Integrated
Circuit
Systems, Inc.

ICS9250-11

Frequency Timing Generator for PENTIUM II/III™ Systems

General Description

The ICS9250-11 is a main clock synthesizer chip for Pentium II based systems using Rambus Interface DRAMs. This chip provides all the clocks required for such a system when used with a Direct Rambus Clock Generator (DRCG) chip such as the ICS9212-01, 02, 03 and a PCI buffer 9112-17.

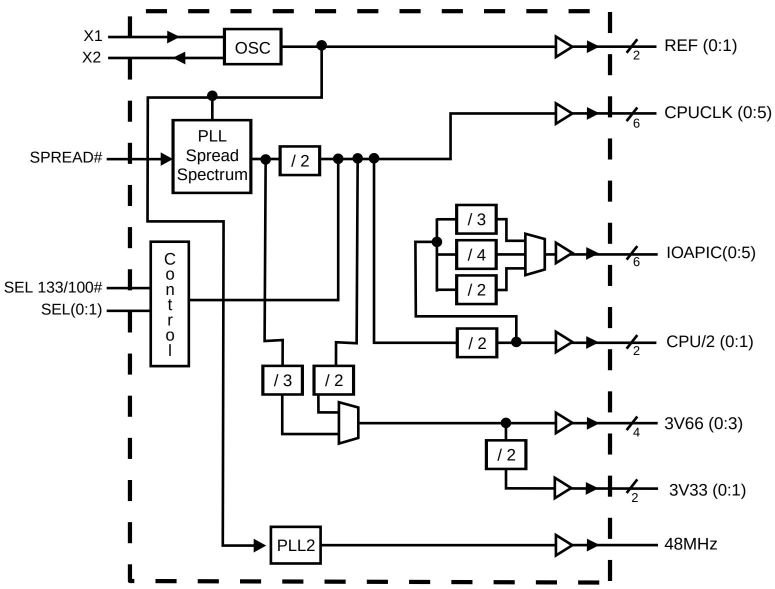
Spread Spectrum may be enabled by driving the SPREAD# pin active. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-11 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

The CPU/2 clocks are inputs to the DRCG.

Features

- Generates the following system clocks:
  - 6 - CPU Clocks 100/133MHz (2.5V).
  - 2 - CPU/2 output for synchronous memory reference (2.5V).
  - 4 - fixed frequency Clocks @ 66.6MHz (3.3V).
  - 2 - fixed frequency Clocks @ 33.3MHz (3.3V).
  - 6 - IOAPIC Clocks @ ¼ of CPUCLK or 16.667MHz, synchronous to CPU Clock (2.5V)
  - 1 - 48MHz Clock (3.3V)
  - 2 - REF Clocks @ 14.31818MHz
- 0.5% typical down spread modulation on CPU, PCI, IOAPIC, 3V66 and CPU/2 output clocks.
- Uses external 14.318MHz crystal.

Block Diagram



Pin Configuration

Pin name	Pin	Pin	Pin name
GNDLAPIC	1	56	VDDLAPIC
APIC1	2	55	APIC2
APIC0	3	54	APIC3
VDDLAPIC	4	53	GNDLAPIC
VDDREF	5	52	GNDLAPIC
X1	6	51	APIC4
X2	7	50	APIC5
GNDREF	8	49	VDDLAPIC
REF0/FREQ_APIC#	9	48	VDDLCPU
REF1/TEST#	10	47	CPUCLK0
VDDREF	11	46	CPUCLK1
VDD66	12	45	GNDLCPU
3V66_0	13	44	GNDLCPU
3V66_1	14	43	CPUCLK2
GND66	15	42	CPUCLK3
GND66	16	41	VDDLCPU
3V66_2	17	40	VDDLCPU
3V66_3	18	39	CPUCLK4
VDD66	19	38	CPUCLK5
VDD33	20	37	GNDLCPU
3V33_0	21	36	GNDLCPU/2
3V33_1	22	35	CPU/2-0
GND3V33	23	34	CPU/2-1
GNDCOR	24	33	VDDLCPU/2
VDDCOR	25	32	SPREAD#
GND48	26	31	SEL1
48MHz	27	30	SEL0
VDD48	28	29	SEL133/100#

ICS9250-11

56-pin SSOP

Power Groups:

VDDREF, GNDREF = REF, X1, X2
VDD66, GND66 = 3V66
VDD33, GND33 = 3V33
VDD48, GND48 = 48MHz
VDDCOR, GNDCOR = PLL Core
VDDLCPU, GNDLCPU = CPUCLK
VDDLCPU/2 , GNDLCPU/2 = CPU/2
VDDLAPIC, GNDAPIC = IOAPIC

9250-11 Rev C 3/20/00

Pin Descriptions

Pin number	Pin name	Type	Description
1, 52, 53	GNDLAPIC	PWR	Ground pin for the IOAPIC outputs.
2, 3, 50, 51, 54, 55	IOAPIC (0:5)	OUT	2.5V clock outputs running divide synchronous with the CPU (Host bus) clock frequency. The default APIC is running at ¼ of CPUCLK frequency. When FREQ_APIC is strapped low, the APIC is running at fixed 16.67 MHz. If CPU = 133 MHz, APIC = CPU/8 If CPU = 100 MHz, APIC = CPU/6
4, 49, 56	VDDLAPIC	PWR	Power pin for the IOAPIC outputs. 2.5V.
5, 11	VDDREF	PWR	Power pin for REF clocks
6	X1	IN	XTAL_IN 14.318MHz crystal input
7	X2	OUT	XTAL_OUT Crystal output
9	REF0	OUT	3.3V 14.318 MHz clock output. APIC clock strapping option for fixed 16.67 MHz APIC clock outputs.
	FREQ_APIC#	OUT	If FREQ_APIC# = 0, APIC Clock = 16.67 MHz If FREQ_APIC# = Open, APIC Clock = CPU/4
10	REF1	OUT	3.3V 14.318MHz clock output.
	TEST#	OUT	TEST# is sampled low (external with 10k pulldown). All clock outputs are Tri-State.
12, 19	VDD66	PWR	power pin for the 3V66 clocks.
13, 14, 17, 18	3V66[0:3]	OUT	66MHz outputs at 3.3V. These outputs are stopped when CPU_STOP# is driven active..
8, 15, 16, 23, 24	GND	PWR	Ground pin for 3V outputs.
21, 22	3V33MHz	OUT	3.3V Fixed 33MHz clock output.
25	VDDCOR	PWR	3.3V power for PLL core.
26	GND48	PWR	Ground pin for the 48MHz output
27	48MHz	OUT	Fixed 48MHz clock output. 3.3V
28	VDD48	PWR	Power pin for the 48MHz output.
29	SEL 133/100#	IN	This selects the frequency for the CPU and CPU/2 outputs. High = 133MHz, Low=100MHz
30, 31	SEL[0:1]	IN	Function select pins. See truth table for details.
32	SPREAD#	IN	Enables spread spectrum when active(Low). modulates all the CPU, PCI, IOAPIC, 3V66 and CPU/2 clocks. Does not affect the REF and 48MHz clocks. 0.5% down spread modulation.
33	VDDLCPU/2	PWR	Power pin for the CPU/2 clocks. 2.5V
34, 35	CPU/2[0:1]	OUT	2.5V clock outputs at 1/2 CPU frequency. 66MHz or50MHz depending on the state of the SEL 133/100# input pin.
36	GNDLCPU/2	PWR	Ground pin for the CPU/2 clocks.
37, 44, 45	GNDLCPU	PWR	Ground pin for the CPUCLKs
38, 39, 42, 43, 46, 47	CPUCLK[0:5]	OUT	Host bus clock output at 2.5V. 133MHz or 100MHz depending on the state of the SEL 133/100MHz.
40, 41, 48	VDDLCPU	PWR	Power pin for the CPUCLKs. 2.5V

Frequency Select:

SEL 133/100#	SEL1	SEL0	CPU MHz	CPU/2 MHz	3V66 MHz	3V33 MHz	48 MHz	REF MHz	IOAPIC MHz
0	0	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
0	0	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0	1	0	100	50.00	66.6	33.3	OFF	14.318	¼ CPUCLK/16.67
0	1	1	100	50.00	66.6	33.3	48	14.318	¼ CPUCLK/16.67
1	0	0	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16
1	0	1	N/A	N/A	N/A	N/A	NA	N/A	N/A
1	1	0	133.3	66.6	66.6	33.3	OFF	14.318	¼ CPUCLK/16.67
1	1	1	133.3	66.6	66.6	33.3	48	14.318	¼ CPUCLK/16.67

Power Management Features:

SEL 133/100#	SEL1	SEL0	Function
0	0	0	All outputs Tri-State
0	00	1	Reserved
0	1	0	Active 100 MHz, 48 MHz PLL inactive
0	1	1	Active 100 MHz, 48 MHz PLL active
1	0	0	Test Mode
1	0	1	Reserved
1	1	0	Active 133 MHz, 48 MHz PLL inactive
1	1	1	Active 133 MHz, 48 MHz PLL active

Absolute Maximum Ratings

Supply Voltage . . . . 7.0 V
Logic Inputs . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . 0°C to +70°C
Storage Temperature . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = Max loads; Select @ 100 MHz			160	mA
		C_L = Max loads; Select @ 133 MHz			160	
	$I_{DD.25OP}$	C_L = Max loads; Select @ 100 MHz			75	mA
		C_L = Max loads; Select @ 133 MHz			90	
Powerdown Current	$I_{DD3.3PD}$	C_L = Max loads			200	µA
	$I_{DD.25PD}$	Input address VDD or GND			100	
Input Frequency	F_i	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance[1]	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	13.5	18	22.5	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		8	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		8	ns
Skew[1]	$T_{CPU\text{-}3V66}$	CPU @ 1.25V, 3V66 @ 1.5V	0		1.5	ns
	$T_{3V66\text{-}3V33}$	3V66 @ 1.5V, 3V33 @ 1.5V	1.5		3.5	ns
	$T_{CPU\text{-}IOAPIC}$	CPU @ 1.25V, IOAPIC @ 1.25V	1.0		3.0	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH\ @\ MIN}$ = 1.0 V	-27			mA
		$V_{OH\ @\ MAX}$ = 2.375 V			-27	
Output Low Current	I_{OL2B}	$V_{OL\ @\ MIN}$ = 1.2 V	27			mA
		$V_{OL\ @\ MAX}$ = 0.3 V			30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45		55	%
Skew window[1]	t_{sk2B}	V_T = 1.25 V			175	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V			150	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU/2

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH\ @\ MIN}$ = 1.0 V	-27			mA
		$V_{OH\ @\ MAX}$ = 2.375 V			-27	
Output Low Current	I_{OL2B}	$V_{OL\ @\ MIN}$ = 1.2 V	27			mA
		$V_{OL\ @\ MAX}$ = 0.3 V			30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45		55	%
Skew window[1]	t_{sk2B}	V_T = 1.25 V			175	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V			250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V33

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -14.5 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	$V_{OH\ @\ MIN}$ = 1.0 V	-33			mA
		$V_{OH\ @\ MAX}$ = 3.135 V			-33	
Output Low Current	I_{OL1}	$V_{OL\ @\ MIN}$ = 1.95 V	30			mA
		$V_{OL\ @\ MAX}$ = 0.4 V			38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2.0	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2.0	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45		55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V			250	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc\text{-}cyc1}$	V_T = 1.5 V			250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -14.5 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} =9 mA			0.4	V
Output High Current	I_{OH1}	$V_{OH\ @\ MIN}$ = 1.0 V	-33			mA
		$V_{OH\ @\ MAX}$ = 3.135 V			-33	
Output Low Current	I_{OL1}	$V_{OL\ @\ MIN}$ = 1.95 V	30			mA
		$V_{OL\ @\ MAX}$ = 0.4 V			38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2.0	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2.0	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45		55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V			250	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc\text{-}cyc1}$	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	$V_{OH\ @\ MIN}$ = 1.0 V	-29			mA
		$V_{OH\ @\ MAX}$ = 3.135 V			-23	
Output Low Current	I_{OL5}	$V_{OL\ @\ MIN}$ = 1.95 V	29			mA
		$V_{OL\ @\ MAX}$ = 0.4 V			27	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1.0		4.0	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1.0		4.0	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter, cycle-to-cycle[1]	$t_{jcyc\text{-}cyc5}$	V_T = 1.5 V, Fixed clocks			500	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc\text{-}cyc5}$	V_T = 1.5 V, Ref clocks			1000	ps

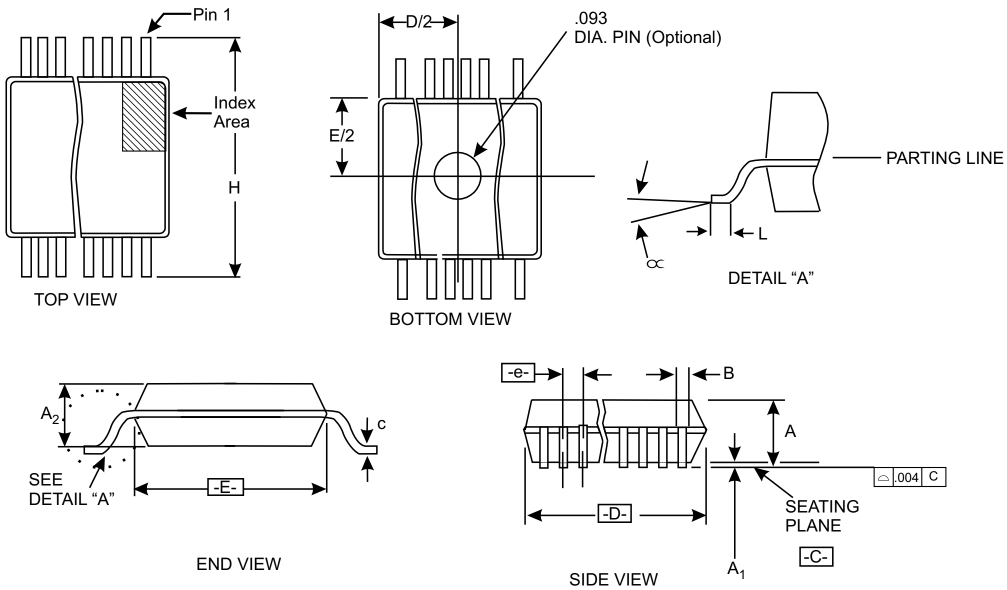
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH\ @\ MIN}$ = 1.0 V	-27			mA
		$V_{OH\ @\ MAX}$ = 2.375 V			-27	
Output Low Current	I_{OL2B}	$V_{OL\ @\ MIN}$ = 1.2 V	27			mA
		$V_{OL\ @\ MAX}$ = 0.3 V			30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45		55	%
Skew window[1]	t_{sk2B}	V_T = 1.25 V			250	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc\text{-}cyc2B}$	V_T = 1.25 V			250	ps

[1]Guaranteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AD	.720	.725	.730	56
A1	.008	.012	.016					
A2	.087	.090	.094					
B	.008	-	.0135					
c	.005	-	.010					
D	See Variations							
E	.291	.295	.299	"For current dimensional specifications, see JEDEC 95."				
e	0.025 BSC							
H	.395	-	.420					
h	.010	.013	.016	Dimensions in inches				
L	.020	-	.040					
N	See Variations							
∝	0°	-	8°					

56 Pin 300 mil SSOP Package

Ordering Information

ICS9250yF-11-T

Example:

ICS XXXX y F - PPP - T

- T — **Designation for tape and reel packaging**
- PPP — **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- F — **Package Type**
  F=SSOP
- y — **Revision Designator** (will not correlate with datasheet revision)
- XXXX — **Device Type (consists of 3 or 4 digit numbers)**
- ICS — **Prefix**
  ICS, AV = Standard Device