Integrated Circuit Systems, Inc.

ICS9250-14

Preliminary Product Preview

Frequency Timing Generator for Pentium II Systems

General Description

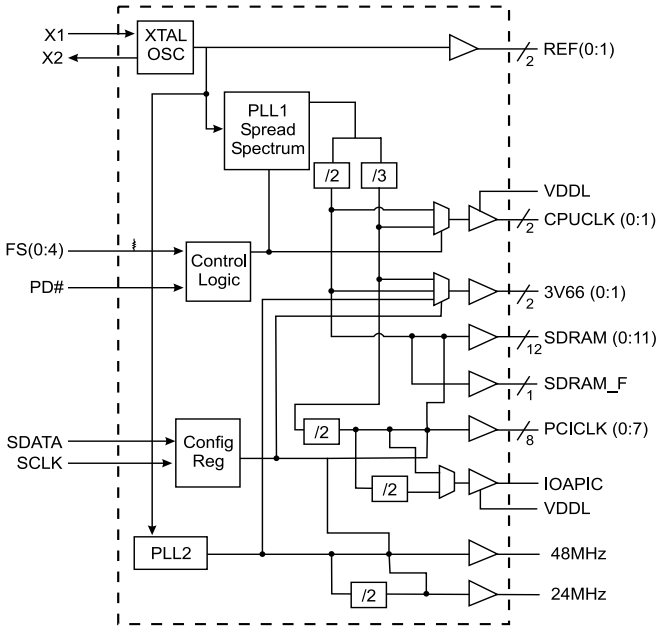
The **ICS9250-14** is a single chip clock for Intel Pentium II. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-14 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Features

- Generates the following system clocks:
  - 2 - CPUs @ 2.5V, up to 150MHz.
  - 1 - IOAPIC @ 2.5V, PCI or PCI/2MHz.
  - 13 SDRAMs (3.3V) @ 150MHz.
  - 2 - 3V66 @ 3.3V, 2x PCIMHz.
  - 8 - PCIs @ 3.3V.
  - 1 - 48MHz, @ 3.3V fixed.
  - 2 - REF @ 3.3V, 14.318Hz.
  - 1 - 24MHz, @ 3.3V fixed.
- Supports spread spectrum modulation , ± .25% center spread.
- I^2C support for power management
- Efficient power management scheme through PD#
- Uses external 14.138 MHz crystal

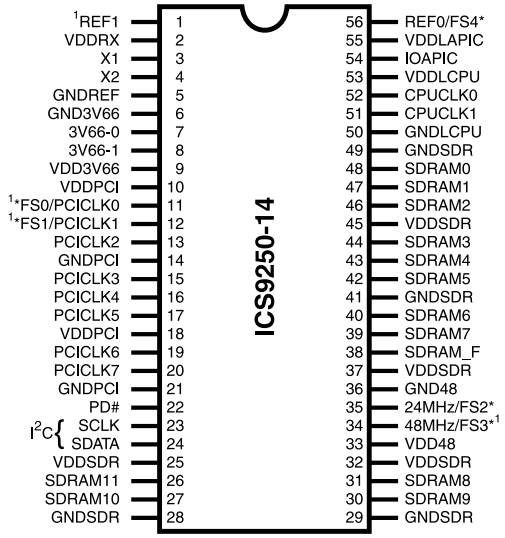
Block Diagram



Skew Specifications

- CPU – CPU: <175ps
- SDRAM - SDRAM: < 250ps
- 3V66 – 3V66: <250ps
- PCI – PCI: <500ps
- CPU-SDRAM<500ps
- CPU(early)-PCI: MIN=1.0ns,TYP=2.0,MAX=4.0
- CPU-3V66<500ps
- 3V66(early)-PCI: MIN=1.5ns,TYP=2.0,MAX=4.0
- IOAPIC-PCI<500ps

Pin Configuration



56-Pin 300 mil SSOP

1. These pins will have 2X drive strength.

* 120K ohm pull-up to VDD on indicated inputs.

Power Groups

GNDREF, VDDREF = REF, Crystal
GND3V66, VDD3V66 = 3V66
GNDPCI, VDDPCI = PCICLKs
GNDCOR, VDDCOR = PLLCORE
GND48, VDD48 = 48
GNDSDR, VDDSDR = SDRAM
GNDLCPU, VDDLCPU = CPUCLK
GNDLPCI, VDDLAPIC = IOAPIC

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I^2C is a trademark of Philips Corporation

PRODUCT PREVIEW documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF1	OUT	3.3V, 14.318MHz reference clock output.
2, 9, 10, 18, 25, 32, 37, 45	VDD	PWR	3.3V power supply
3	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
5, 6, 14, 21, 28, 29, 36, 41, 49	GND	PWR	Ground pins for 3.3V supply
7, 8	3V66 (0;1)	OUT	3.3V Fixed 66MHz clock outputs for HUB
11	PCICLK0[1]	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
	FS0	IN	Logic input frequency select bit. Input latched at power on.
12	PCICLK1[1]	IN	3.3V PCI clock outputs, with Synchronous CPUCLKS
	FS1	IN	Logic input frequency select bit. Input latched at power on.
13, 15, 16, 17, 19, 20	PCICLK (2:7)	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
22	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
23	SCLK	IN	Clock input of I^2C input
24	SDATA	IN	Data input for I^2C serial input.
34	48MHz	OUT	3.3V Fixed 48MHz clock output for USB
	FS3	IN	Logic input frequency select bit. Input latched at power on.
35	FS2	IN	Logic input frequency select bit. Input latched at power on.
	24MHz	OUT	3.3V fixed 24MHz output
38	SDRAM_F	OUT	3.3V free running 100MHz SDRAM not affected by I^2C
26, 27, 30, 31, 39, 40, 42, 43, 44, 47, 48	SDRAM (11:0)	OUT	3.3V output running 100MHz. All SDRAM outputs can be turned off through I^2C
50	GNDL	PWR	Ground for 2.5V power supply for CPU & APIC
51, 52	CPUCLK (0:1)	OUT	2.5V Host bus clock output. 66MHz or 100MHz depending on FS (0:1) pins Refer page 3.
53, 55	VDDL	PWR	2.5V power suypply for CPU, IOAPIC
54	IOAPIC	OUT	2.5V clock outputs running at 16.67MHz.
56	FS4	IN	Logic input frequency select bit. Input latched at power on.
	REF0[1]	OUT	3.3V, 14.318MHz reference clock output.

Note:
1. These pins will have 2X drive strength.

Frequency Selection

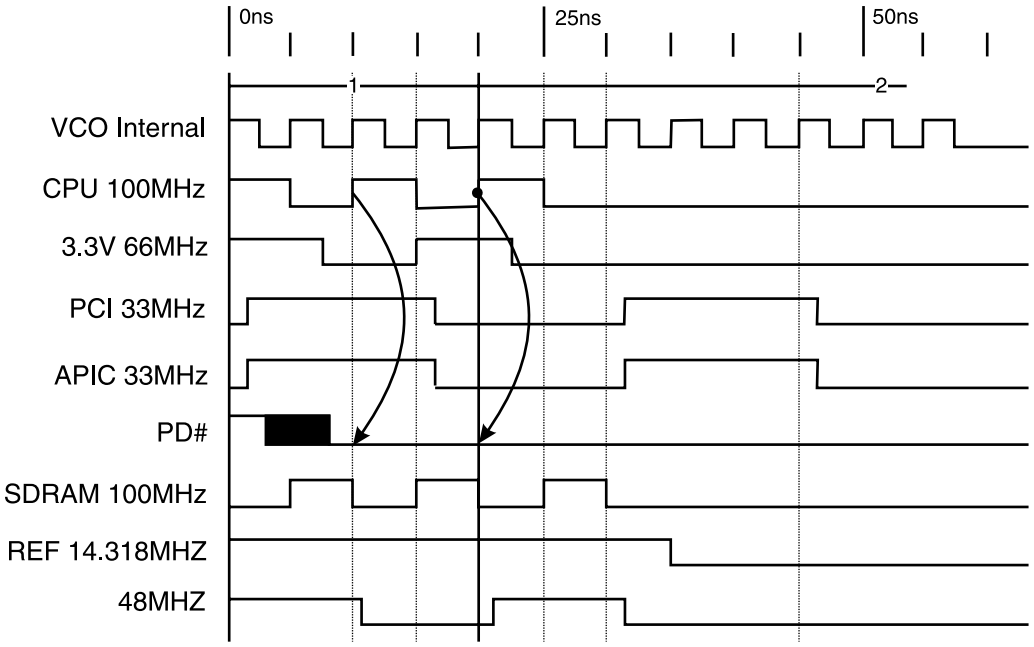
FS4	FS3	FS2	FS1	FS0	CPU MHz	SDRAM MHz	3V66 MHz	PCI MHz	IOAPIC MHz
0	0	0	0	0	67.81	101.71	67.81	33.90	16.95
0	0	0	0	1	70.00	105.00	70.00	35.00	17.50
0	0	0	1	0	72.01	108.01	72.01	36.00	18.00
0	0	0	1	1	66.67	100.00	66.67	33.33	16.67
0	0	1	0	0	73.01	109.51	73.01	36.50	18.25
0	0	1	0	1	75.00	112.50	75.00	37.50	18.75
0	0	1	1	0	77.00	115.50	77.00	38.50	19.25
0	0	1	1	1	78.01	117.01	78.01	39.00	19.50
0	1	0	0	0	80.00	120.00	80.00	40.00	20.00
0	1	0	0	1	83.00	124.51	83.00	41.50	20.75
0	1	0	1	0	84.49	126.74	84.49	42.25	21.12
0	1	0	1	1	100.00	150.00	100.00	50.00	25.00
0	1	1	0	0	86.08	129.12	86.08	43.04	21.52
0	1	1	0	1	88.00	132.00	88.00	44.00	22.00
0	1	1	1	0	90.00	135.00	90.00	45.00	22.50
0	1	1	1	1	95.00	142.50	95.00	47.50	23.75
1	0	0	0	0	49.90	49.90	33.26	16.63	8.32
1	0	0	0	1	100.00	100.00	66.66	33.33	16.67
1	0	0	1	0	74.85	74.85	49.90	24.95	12.47
1	0	0	1	1	66.58	66.58	44.39	22.19	11.10
1	0	1	0	0	82.84	82.84	55.23	27.61	13.81
1	0	1	0	1	89.81	89.81	59.88	29.94	14.97
1	0	1	1	0	94.80	94.80	63.20	31.60	15.80
1	0	1	1	1	100.50	100.50	67.00	33.50	16.75
1	1	0	0	0	104.78	104.78	69.86	34.93	17.46
1	1	0	0	1	111.77	111.77	74.52	37.26	18.63
1	1	0	1	0	114.77	114.77	76.51	38.26	19.13
1	1	0	1	1	100.00	100.00	66.66	33.33	16.67
1	1	1	0	0	123.75	123.75	82.50	41.25	20.62
1	1	1	0	1	132.74	132.74	88.49	44.25	22.12
1	1	1	1	0	139.75	139.75	93.16	46.58	23.29
1	1	1	1	1	149.69	149.69	99.79	49.90	24.95

Note:
* These output frequencies are not synchronous to CPUCLK and do not have spread spectrum modulation.

Clock Enable Configuration

PD#	CPUCLK	SDRAM	IOAPIC	66MHz	PCICLK	REF, 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Byte 0: Functionality and frequency select register (Default=0)
(1 = enable, 0 = disable)

Bit	Description										PWD
Bit (2, 7:4)	Bit (2,7:4)					CPUCLK MHz	SDRAM MHz	3V66 MHz	PCICLK	IOAPIC MHz	XXXX Note 1
	0	0	0	0	0	67.81	101.71	67.81	33.90	16.95	
	0	0	0	0	1	70.00	105.00	70.00	35.00	17.50	
	0	0	0	1	0	72.01	108.01	72.01	36.00	18.00	
	0	0	0	1	1	66.67	100.00	66.67	33.33	16.67	
	0	0	1	0	0	73.01	109.51	73.01	36.50	18.25	
	0	0	1	0	1	75.00	112.50	75.00	37.50	18.75	
	0	0	1	1	0	77.00	115.50	77.00	38.50	19.25	
	0	0	1	1	1	78.01	117.01	78.01	39.00	19.50	
	0	1	0	0	0	80.00	120.00	80.00	40.00	20.00	
	0	1	0	0	1	83.00	124.51	83.00	41.50	20.75	
	0	1	0	1	0	84.49	126.74	84.49	42.25	21.12	
	0	1	0	1	1	100.00	150.00	100.00	50.00	25.00	
	0	1	1	0	0	86.08	129.12	86.08	43.04	21.52	
	0	1	1	0	1	88.00	132.00	88.00	44.00	22.00	
	0	1	1	1	0	90.00	135.00	90.00	45.00	22.50	
	0	1	1	1	1	95.00	142.50	95.00	47.50	23.75	
	1	0	0	0	0	49.90	49.90	33.26	16.63	8.32	
	1	0	0	0	1	100.00	100.00	66.66	33.33	16.67	
	1	0	0	1	0	74.85	74.85	49.90	24.95	12.47	
	1	0	0	1	1	66.58	66.58	44.39	22.19	11.10	
	1	0	1	0	0	82.84	82.84	55.23	27.61	13.81	
	1	0	1	0	1	89.81	89.81	59.88	29.94	14.97	
	1	0	1	1	0	94.80	94.80	63.20	31.60	15.80	
	1	0	1	1	1	100.50	100.50	67.00	33.50	16.75	
	1	1	0	0	0	104.78	104.78	69.86	34.93	17.46	
	1	1	0	0	1	111.77	111.77	74.52	37.26	18.63	
	1	1	0	1	0	114.77	114.77	76.51	38.26	19.13	
	1	1	0	1	1	100.00	100.00	66.66	33.33	16.67	
	1	1	1	0	0	123.75	123.75	82.50	41.25	20.62	
	1	1	1	0	1	132.74	132.74	88.49	44.25	22.12	
	1	1	1	1	0	139.75	139.75	93.16	46.58	23.29	
	1	1	1	1	1	149.69	149.69	99.79	49.90	24.95	
Bit 3	0-Frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,6:4										0
Bit 1	0- Normal 1- Spread spectrum enable ± 0.25% Center Spread										1
Bit 0	0- Running 1- Tristate all outputs										0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as diplayed by Bit 3.

Byte 1: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	X	FS3#
Bit 6	-	X	FS0#
Bit 5	-	X	FS2#
Bit 4	35	1	24_48MHz
Bit 3	-	1	(Reserved)
Bit 2	34	1	48MHz
Bit 1	-	1	(Reserved)
Bit 0	38	1	SDRAM_F

Byte 2: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	39	1	SDRAM7
Bit 6	40	1	SDRAM6
Bit 5	42	1	SDRAM5
Bit 4	43	1	SDRAM4
Bit 3	44	1	SDRAM3
Bit 2	46	1	SDRAM2
Bit 1	47	1	SDRAM1
Bit 0	48	1	SDRAM0

Byte 3: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	20	1	PCICLK7
Bit 6	19	1	PCICLK6
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	15	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	12	1	PCICLK1
Bit 0	11	1	PCICLK0

Byte 4: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	7	1	3V66_0
Bit 5	8	1	3V66_0
Bit 4	-	X	FS4#
Bit 3	54	1	IOAPIC
Bit 2	-	X	FS1#
Bit 1	51	1	CPUCLK1
Bit 0	52	1	CPUCLK0

Byte 5: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	26	1	SDRAM11
Bit 2	27	1	SDRAM10
Bit 1	30	1	SDRAM9
Bit 0	31	1	SDRAM8

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%, VDDL=2.5 V± 5%(unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M		60	100	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND		400	600	µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Pin Inductance	L_{pin}			7		nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance		6		pF
	C_{INX}	X1 & X2 pins	13.5		22.5	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.				mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guarenteed by design, not 100% tested in production.

SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O2}		66		100	MHz
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$= 1.0V , $V_{OH@MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$= 1.2V , $V_{OL@MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	ns
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4		1.6	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			175	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O4}			16.67		MHz
Output Frequency	F_{O5}			33		MHz
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output High Voltage	$V_{OH4\B}$	I_{OH} = -5.5 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 9.0 mA			0.4	V
Output High Current	I_{OH4B}	$V_{OH@\,min}$ = 1.4 V, $V_{OH@\,MAX}$ = 2.5 V	-36		-21	mA
Output Low Current	I_{OL4B}	$V_{OL@\,MIN}$ = 1.0 V, $V_{OL@\,MAX=}$ 0.2	36		31	mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	nS
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4		1.6	nS
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	45		55	%
Jitter	$t_{jcyc-cyc}$	V_T = 1.25 V			500	pS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O3}			100		MHz
Output Impedance	R_{DSP3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output Impedance	R_{DSN3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH3}	$V_{OH\,@MIN}$= 2.0 V, $V_{OH@\,MAX}$=3.135 V	-54		-46	mA
Output Low Current	I_{OL3}	$V_{OL@\,MIN}$= 1.0 V, $V_{OL@\,MAX}$=0.4 V	54		53	mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4		1.6	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45		55	%
Skew	T_{sk3}[1]	V_T = 1.5 V			250	ps
Jitter	tjcyc-cyc	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			33		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

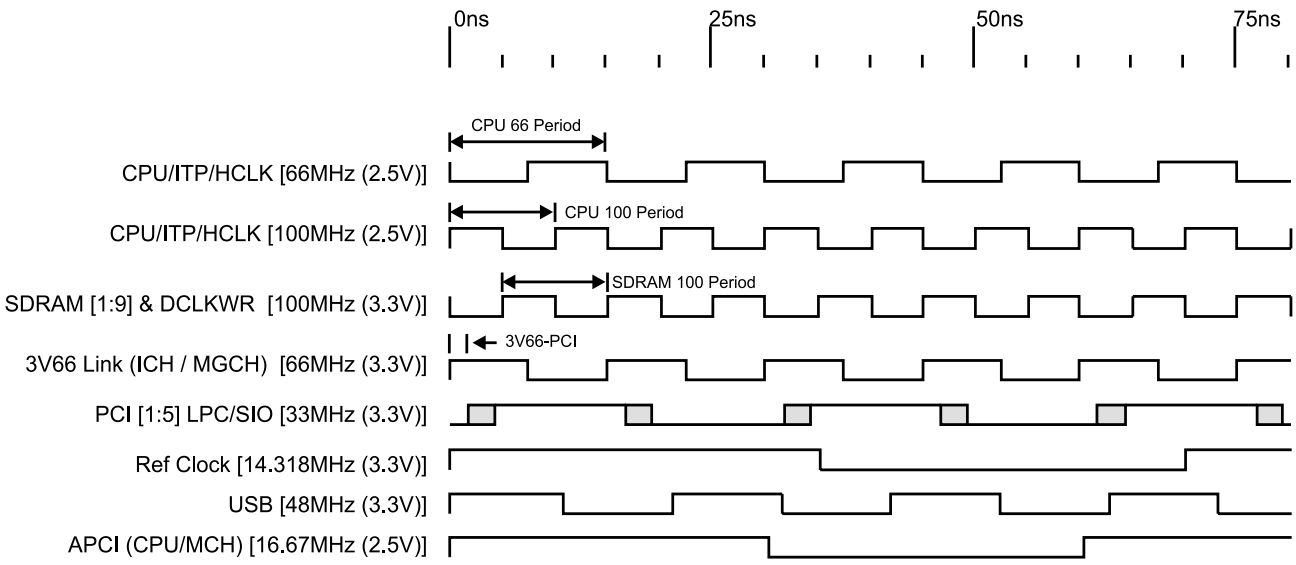
Electrical Characteristics - 48M, REF

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 10 -20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O48M}			48		MHz
Output Frequency	F_{OREF}			14.318		MHz
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = 1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = -1 mA			0.4	V
Output High Current	I_{OH5}	$V_{OH@MIN}$=1 V, $V_{OH@MAX}$= 3.135 V	-29		-23	mA
Output Low Current	I_{OL5}	$V_{OL@MIN}$=1.95 V, $V_{OL@MIN}$=0.4 V	29		27	mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	4	nS
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.7	4	nS
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Fixed Clocks			500	pS
	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Ref Clocks			1000	pS
Skew	T_{sk}	V_T = 1.5 V			250	pS

[1]Guarenteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

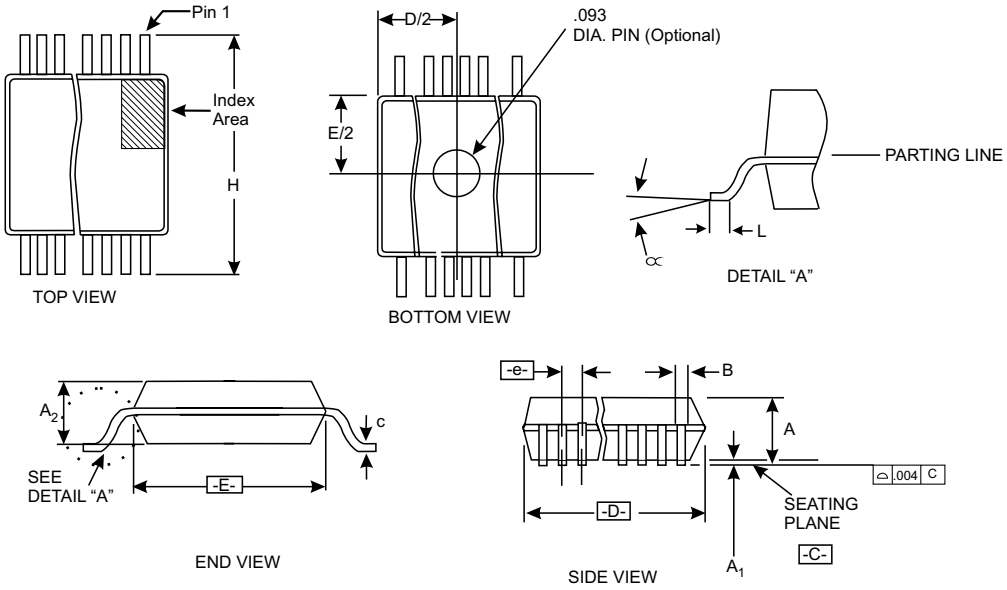


Group Offset Waveforms

Group Skews at Common Transition Edges:

CPU & IOAPIC load (lumped) = 20pf; PCI, SDRAM, 3V66 LOAD (LUMPED) = 30pf.

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CPU (at 66MHz) to 3V66	$S_{CPU1-3V66}$	CPU @ 1.25V, 3V66 @ 1.5V (Note: 180° offset between CPU & 3V66	0		500	ps
CPU (at 100MHz) to SDRAM	$S_{CPU2-SDRAM}$	CPU @ 1.25V, SDRAM @ 1.5V (Note: 180° offset between CPU & SDRAM	0		500	ps
3V66 to PCI	$S_{3V66-PCI}$	3V66 @ 1.5V, PCI @ 1.5V	1.5	2.1	4	ns
IOAPIC to PCI	$S_{IOAPIC-PCI}$	IOAPIC @ 1.25V, PCI @1.5V	0		500	ps



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AD	.720	.725	.730	56
A1	.008	.012	.016	"For current dimensional specifications, see JEDEC 95."				
A2	.087	.090	.094					
B	.008	-	.0135					
c	.005	-	.010					
D	See Variations							
E	.291	.295	.299					
e	0.025 BSC							
H	.395	-	.420					
h	.010	.013	.016	Dimensions in inches				
L	.020	-	.040					
N	See Variations							
∝	0°	-	8°					

56 Pin 300 mil SSOP Package

Ordering Information

ICS9250yF-14-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

PRODUCT PREVIEW documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.