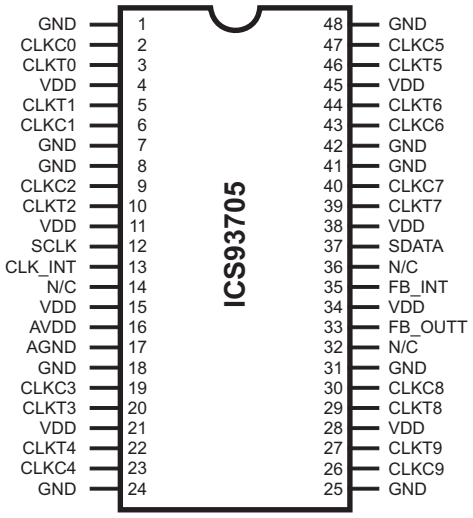
DDR Phase Lock Loop Zero Delay Clock Buffer

Recommended Application:
DDR Zero Delay Clock Buffer

Product Description/Features:
- Low skew, low jitter PLL clock driver
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- 3.3V tolerant CLK_INT input

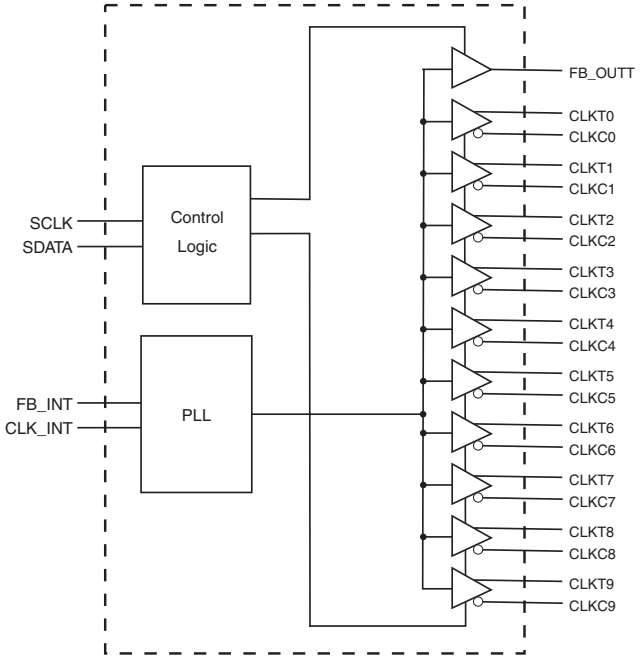
Switching Characteristics:
- PEAK - PEAK jitter (66MHz): <120ps
- PEAK - PEAK jitter (>100MHz): <75ps
- CYCLE - CYCLE jitter (66MHz):<120ps
- CYCLE - CYCLE jitter (>100MHz):<65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 450ps - 950ps
- DUTY CYCLE: 49% - 51%

Pin Configuration



48-Pin SSOP

Block Diagram



Functionality

INPUTS		OUTPUTS			PLL State
AVDD	CLK_INT	CLKT	CLKC	FB_OUTT	
2.5V (nom)	L	L	H	L	on
2.5V (nom)	H	H	L	H	on
2.5V (nom)	<20MHz(1)	Z	Z	Z	off
GND	L	L	H	L	Bypassed/off
GND	H	H	L	H	Bypassed/off

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementary" clocks of differential pair outputs.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
4, 11, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V
12	SCLK	IN	Clock input of I^2C input, 5V tolerant input
13	CLK_INT	IN	"True" reference clock input, 3.3V tolerant input
14, 32, 36	N/C	-	Not connected
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground.
33	FB_OUTT	OUT	"True" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
35	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
37	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant

Byte 0: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 1: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 2: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 3: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 4: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 5: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	3,2	1	CLK0 (T&C)
Bit6	-	1	-
Bit5	10, 9	1	CLK2 (T&C)
Bit4	20, 19	1	CLK3 (T&C)
Bit3	22, 23	1	CLK4 (T&C)
Bit2	27, 26	1	CLK9 (T&C)
Bit1	-	1	Reserved
Bit0	-	1	Reserved

Byte 6: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	29, 30	1	CLK8 (T&C)
Bit3	39, 40	1	CLK7 (T&C)
Bit2	44, 43	1	CLK6 (T&C)
Bit1	46, 47	1	CLK5 (T&C)
Bit0	-	1	Reserved

Note: Don't write into these registers (7:5), writing into these registers can cause malfunction.

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input / Supply / Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND				µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND				µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0 pF at 133 MHz		245	300	mA
	I_{DDPD}	C_L = 0 pF			100	µA
Output High Current	I_{OH}	V_{DD} = 2.3V, V_{OUT} = 1V		-43	-18	mA
Output High Current	I_{OL}	V_{DD} = 2.3V, V_{OUT} = 1.2V	26	43		mA
High Impedance Output Current	I_{OZ}	V_{DD} = 2.7V, $V_{OUT} = V_{DD}$ or GND			10	µA
Input Clamp Voltage	V_{IK}	Iin = -18 mA;				V
High-level Output Voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1mA	2.1	2.42		V
		V_{DD} = 2.3V, I_{OH} = -12mA		1.87		V
Low-level Output Voltage	V_{OL}	V_{DD} = min to max, I_{OH} = 1mA		0.04	0.1	V
		V_{DD} = 2.3V, I_{OH} = 12mA		0.35	0.6	V
Input Capacitance[1]	C_{IN}	$V_I = V_{DD}$ or GND				pF
Output Capacitance[1]	C_{OUT}	$V_I = V_{DD}$ or GND		3		pF

[1] Guaranteed by design, not 100% tested in production.

Recommended Operating Condition

T_A = 0 - 70°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog/core supply voltage	V_{DD}, A_{VDD}		2.3	2.5	2.7	V
Input voltage level	V_{IL}		-		VDD/2 - 0.5V	V
	V_{IH}		VDD/2 + 0.5V		-	V
Input duty cycle	I_{DC}		40		60	%
Input max jitter	I_{TCYC}				500	ps

Timing Requirements

T_A = 0 - 70C; Supply Voltage AV_{DD}, V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Clock Frequency[1]	$freq_{op}$		66		170	MHz
Input Clock Duty Cycle[1]	d_{tin}		40		60	%
Clock Stabilization[1]	t_{STAB}	from V_{DD} = 2.5V to 1% target frequency			100	µs

1. Guaranteed by design, not 100% tested in production.

Switching Characteristics

T_A = 0 - 70C; Supply Voltage V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Jitter[1]	t_{jabs}	66 MHz			120	ps
		100 / 125 / 133 / 167 MHz			75	
Cycle to cycle Jitter[1,2]	t_{c-c}	66 MHz		50	110	ps
		100 / 125 / 133 / 167 MHz		35	65	
Phase Error[1]	t_{pe}	with input clock 0-2.5V 0.8ns rise/fall	-150	50	150	ps
Output to output Skew[1]	T_{skew}	with input clock 0-2.5V 0.8ns rise/fall		40	100	ps
Low-to-high level Propagation Delay Time, Bypass Mode[1]	t_{PLH}	CLK_IN to any output, Load = 120W / 12 pF	4	4.5	6	ns
Pulse Skew[1]	T_{skewp}				100	ps
Duty Cycle (differential)[1,3]	D_C	no loads, 66 MHz to 167 MHz	49	50	51	%
Rise Time, Fall Time[1]	t_R, t_F	Single-ended 20 - 80 %; Load = 120Ω / 12 pF	450	550	950	ps

1. Guaranteed by design, not 100% tested in production.
2. Refers to transistion on non-inverting period.
3. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{wH} / t_C, where the cycle time (t_C) decreases as the frequency increases.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D4(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

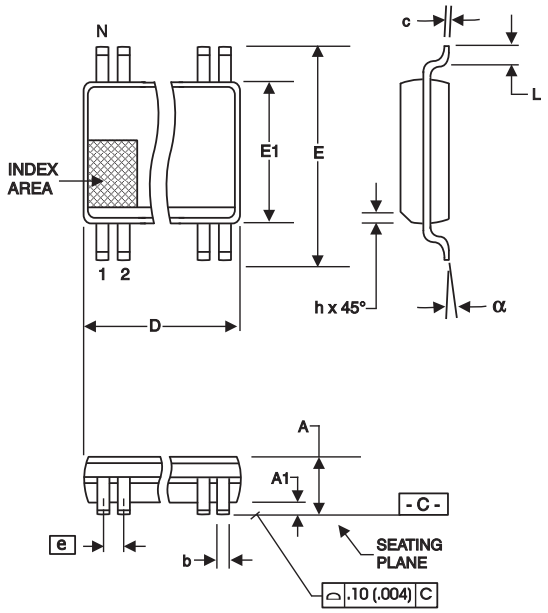
- Controller (host) will send start bit.
- Controller (host) sends the read address D5 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D5(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

0418D—04/28/05



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.748	16.002	.620	.630

JEDEC MO-118 6/1/00
DOC# 10-0034 REV B

Ordering Information

ICS93705yFLF-T

Example:

ICS XXXX y F - PPP LF - T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

0418D—04/28/05

Revision History

Rev.	Issue Date	Description	Page #
D	4/28/2005	Added Lead Free Ordering Information	7

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