



Programmable System Frequency Generator for PII/III™

Recommended Application:

810/810E and Solano (815) type chipset

Output Features:

- 2 - CPUs @ 2.5V
- 13 - SDRAM @ 3.3V
- 3 - 3V66 @ 3.3V
- 7 - PCI @ 3.3V
- 1 - 24/48MHz @ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 1 - REF @ 3.3V, 14.318MHz

Features:

- Programmable output frequency
- Gear ratio change detection
- Real time system reset output
- Spread spectrum for EMI control with programmable spread percentage
- Watchdog timer technology to reset system if over-clocking causes malfunction.
- Support power management through PD#.
- Uses external 14.318MHz crystal
- FS pins for frequency select

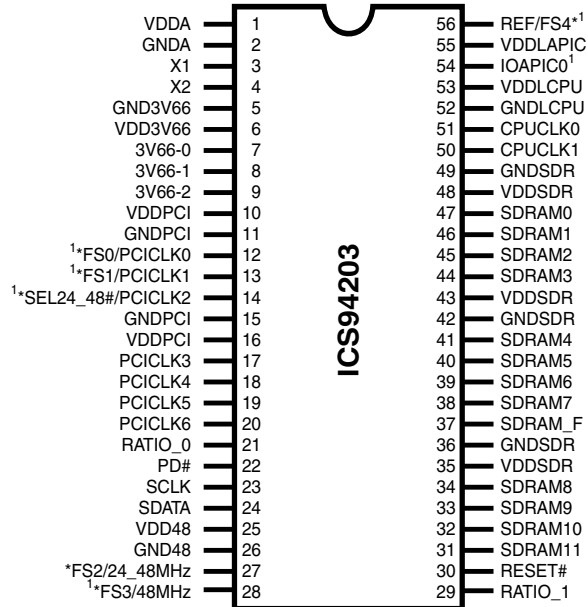
Key Specifications:

- CPU Output Jitter: <250ps
- IOAPIC Output Jitter: <500ps
- 48MHz, 3V66, PCI Output Jitter: <500ps
- CPU Output Skew: <175ps
- PCI Output Skew: <500ps
- 3V66 Output Skew <175ps
- For group skew timing, please refer to the Group Timing Relationship Table.

Power Groups

VDDA, GNDA = Core PLL, Xtal
VDD48, GND48 = 48MHz, Fixed PLL

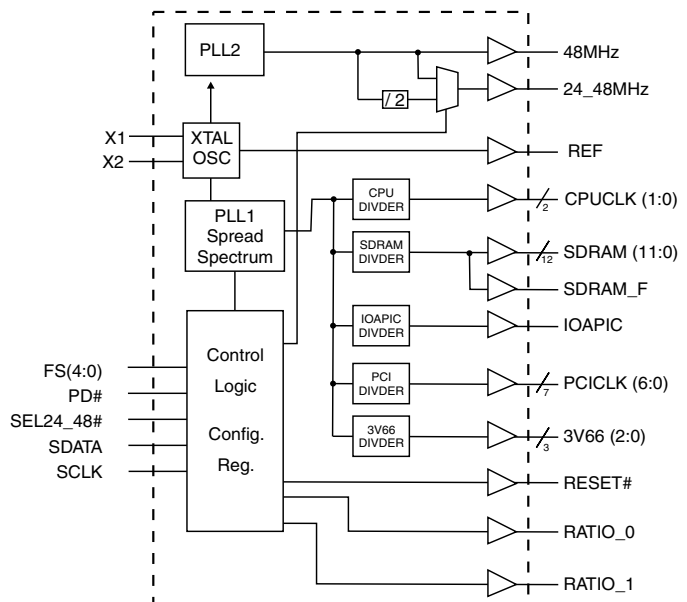
Pin Configuration



56-Pin 300 mil SSOP

1. These pins will have 1.5 to 2X drive strength.
* 120K ohm pull-up to VDD on indicated inputs.

Block Diagram



ICS94203



General Description

The **ICS94203** is a single chip clock solution for desktop designs using the 810/810E and Solano style chipset. It provides all necessary clock signals for such a system.

The **ICS94203** belongs to ICS new generation of programmable system clock generators. It employs serial programming I²C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

Spread spectrum typically reduces system EMI by 7dB to 8dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 6, 10, 16, 25, 35, 43, 48	VDD	PWR	3.3V power supply
3	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
2, 5, 11, 15, 26, 36, 42, 49	GND	PWR	Ground pins for 3.3V supply
9, 8, 7	3V66 [2:0]	OUT	3.3V Fixed 66MHz clock outputs for HUB
12	PCICLK0 ¹	OUT	3.3V PCI clock output, with Synchronous CPUCLKS
	FS0	IN	Logic input frequency select bit. Input latched at power on.
13	PCICLK1 ¹	OUT	3.3V PCI clock output, with Synchronous CPUCLKS
	FS1	IN	Logic input frequency select bit. Input latched at power on.
14	SEL24_48#	IN	24/48MHz frequency select pin for pin 27
	PCICLK2	OUT	3.3V PCI clock output, with Synchronous CPUCLKS
20, 19, 18, 17	PCICLK [6:3]	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
21	RATIO_0	OUT	Output to chipset, replacing the BSEL0 signals originally from the processor.
22	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
23	SCLK	IN	Clock input of I ² C input
24	SDATA	I/O	Data input for I ² C serial input.
27	FS2	IN	Logic input frequency select bit. Input latched at power on.
	24_48MHz	OUT	3.3V 24_48MHz output Default is 24MHz.
28	FS3	IN	Logic input frequency select bit. Input latched at power on.
	48MHz	OUT	3.3V Fixed 48MHz clock output for USB.
29	RATIO_1	OUT	Output to chipset, replacing the BSEL1 signals originally from the processor.
30	RESET	OUT	Real time system reset signal for frequency ratio change or watchdog timer timeout. This signal is active low.
37	SDRAM_F	OUT	3.3V SDRAM output can be turned off through I ² C
31, 32, 33, 34, 38, 39, 40, 41, 44, 45, 46, 47	SDRAM [11:0]	OUT	3.3V output. All SDRAM outputs can be turned off through I ² C
50, 51	CPUCLK [1:0]	OUT	2.5V Host bus clock output. Output frequency derived from FS pins.
52	GNDL	PWR	Ground for 2.5V power supply for CPU & APIC
53, 55	VDDL	PWR	2.5V power supply for CPU, IOAPIC
54	IOAPIC	OUT	2.5V clock outputs running at 16.67MHz.
56	FS4	IN	Logic input frequency select bit. Input latched at power on.
	REF ¹	OUT	3.3V, 14.318MHz reference clock output.



General I²C serial interface information for the ICS94203

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte 0 through Byte 28** (see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 _(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 26	
	ACK
Byte 27	
	ACK
Byte 28	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends **Byte 0 through byte 6 (default)**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 6)**.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 _(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7 _H has been written to B6	Byte 7
ACK	
○	○
○	○
○	○
If 1A _H has been written to B6	Byte 26
ACK	
If 1B _H has been written to B6	Byte 27
ACK	
If 1C _H has been written to B6	Byte 28
ACK	
Stop Bit	

*See notes on the following page.



Brief I²C registers description for ICS94203 Programmable System Frequency Generator

Register Name	Byte	Description	Pwd Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I ² C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-5	Active / inactive output control registers.	See individual byte description
Byte Count Read Back Register	6	Writing to this register will configure byte count and how many byte will be read back. Do not write 00 _H to this byte.	06 _H
Latched Inputs Read Back Register	7	The inverse of the latched inputs level could be read back from this register.	See individual byte description
Watchdog Control Registers	8 Bit[6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	8 Bit[7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 14&15 programming.	0
Watchdog Timer Count Register	9	Writing to this register will configure the number of seconds for the watchdog timer to reset.	FF _H
ICS Reserved Register	10	This is an unused register. Writing to this register will not affect device functionality.	00 _H
Device ID, Vendor ID & Revision ID Registers	11-12	Byte 11 bit[3:0] is ICS vendor id - 0001. Other bits in these 2 registers designate device revision ID of this part.	See individual byte description
ICS Reserved Register	13	Don't write into this register, writing 1's will cause malfunction.	00 _H
VCO Frequency Control Registers	14-15	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	16-17	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Output Dividers Control Registers	18-20	Changing bits in these registers result in frequency divider ratio changes. Incorrect configuration of group output divider ratio can cause system malfunction.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	21	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	22	These register will control the group rise and fall time.	See individual byte description

Notes:

- The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 6.**
- When writing to byte 14 - 15, byte 16 - 17 and byte 18 - 20, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
- The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
- The input is operating at 3.3V logic levels.
- The data byte format is 8 bit bytes.
- To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
- At power-on, all registers are set to a default condition, as shown.



Byte 0: Functionality and frequency select register (Default=0)

Bit	Description													PWD
Bit (2,7:4)	Bit2	Bit7	Bit6	Bit5	Bit4	VCO/REF	VCO	VCO/	CPUCLK	SDRAM	3V66	PCICLK	IOAPIC	Note 1
	FS4	FS3	FS2	FS1	FS0	Divider	MHz	CPU	MHz	MHz	MHz	MHz	MHz	
	0	0	0	0	0	362/13	398.71	6	66.45	99.65	66.43	33.21	16.61	
	0	0	0	0	1	352/14	360.00	6	60.00	90.00	60.00	30.00	15.00	
	0	0	0	1	0	504/18	400.91	6	66.80	100.20	66.80	33.40	16.70	
	0	0	0	1	1	315/11	410.02	6	68.33	102.50	68.33	34.17	17.08	
	0	0	1	0	0	440/15	420.00	6	70.00	105.00	70.00	35.00	17.50	
	0	0	1	0	1	440/14	450.00	6	75.00	112.50	75.00	37.50	18.75	
	0	0	1	1	0	503/15	480.14	6	80.00	120.00	80.00	40.00	20.00	
	0	0	1	1	1	313/9	497.95	6	83.00	124.50	83.00	41.50	20.75	
	0	1	0	0	0	515/37	199.29	2	99.65	99.65	66.43	33.21	16.61	
	0	1	0	0	1	447/40	160.29	2	80.00	80.00	53.33	26.67	13.33	
	0	1	0	1	0	518/37	200.45	2	100.23	100.23	66.84	33.41	16.70	
	0	1	0	1	1	446/31	206.00	2	103.00	103.00	68.67	34.33	17.17	
	0	1	1	0	0	484/33	210.00	2	105.00	105.00	70.00	35.00	17.50	
	0	1	1	0	1	507/33	219.98	2	110.00	110.00	73.33	36.67	18.33	
	0	1	1	1	0	514/32	229.99	2	115.00	115.00	76.67	38.33	19.17	
	0	1	1	1	1	461/11	600.06	2	200.00	200.00	100.00	50.00	25.00	
	1	0	0	0	0	362/13	398.71	3	132.86	132.86	66.43	33.21	16.61	
	1	0	0	0	1	503/15	480.14	3	160.00	160.00	80.00	40.00	20.00	
	1	0	0	1	0	504/18	400.91	3	133.64	133.64	66.82	33.41	16.70	
	1	0	0	1	1	488/17	411.02	3	137.00	137.00	68.50	34.25	17.13	
	1	0	1	0	0	440/15	420.00	3	140.00	140.00	70.00	35.00	17.50	
	1	0	1	0	1	395/13	435.05	3	145.00	145.00	72.50	36.25	18.13	
	1	0	1	1	0	440/14	450.00	3	150.00	150.00	75.00	37.50	18.75	
	1	0	1	1	1	503/15	480.14	3	160.00	160.00	80.00	40.00	20.00	
	1	1	0	0	0	362/13	398.71	3	132.90	99.65	66.93	33.21	16.61	
	1	1	0	0	1	503/15	480.14	3	160.00	100.00	80.00	40.00	20.00	
	1	1	0	1	0	504/18	400.91	3	133.64	100.23	66.82	33.41	16.7	
	1	1	0	1	1	488/17	411.02	3	137.00	102.75	68.50	34.25	17.13	
	1	1	1	0	0	440/15	420.00	3	140.00	105.00	70.00	35.00	17.50	
	1	1	1	0	1	395/13	435.05	3	145.00	108.75	72.50	36.25	18.13	
1	1	1	1	0	440/14	450.00	3	150.00	112.50	75.00	37.50	18.75		
1	1	1	1	1	503/15	480.14	3	160.00	120.00	80.00	40.00	20.00		
Bit 3	0-Frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,7:4													0
Bit 1	0- Normal 1- Spread spectrum enable ± 0.35% Center Spread													1
Bit 0	0- Running 1- Tristate all outputs													0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.



Byte 1: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	27	1	24_48MHz
Bit 3	-	1	(Reserved)
Bit 2	28	1	48MHz
Bit 1	-	1	(Reserved)
Bit 0	37	1	SDRAM_F

Byte 2: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	38	1	SDRAM7
Bit 6	39	1	SDRAM6
Bit 5	40	1	SDRAM5
Bit 4	41	1	SDRAM4
Bit 3	44	1	SDRAM3
Bit 2	45	1	SDRAM2
Bit 1	46	1	SDRAM1
Bit 0	47	1	SDRAM0

Byte 3: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	0	Reserved
Bit 6	20	1	PCICLK6
Bit 5	19	1	PCICLK5
Bit 4	18	1	PCICLK4
Bit 3	17	1	PCICLK3
Bit 2	14	1	PCICLK2
Bit 1	13	1	PCICLK1
Bit 0	12	1	PCICLK0

Byte 4: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	9	1	3V66_2
Bit 6	7	1	3V66_0
Bit 5	8	1	3V66_1
Bit 4	56	1	REF
Bit 3	54	1	IOAPIC0
Bit 2	-	X	Reserved
Bit 1	50	1	CPUCLK1
Bit 0	51	1	CPUCLK0

Byte 5: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	31	1	SDRAM11
Bit 2	32	1	SDRAM10
Bit 1	33	1	SDRAM9
Bit 0	34	1	SDRAM8

Byte 6: Byte Count Read Back Register

Bit	Pin#	PWD	Description
Bit 7	-	0	Reserved (Note)
Bit 6	-	0	Reserved (Note)
Bit 5	-	0	Reserved (Note)
Bit 4	-	0	Reserved (Note)
Bit 3	-	0	Reserved (Note)
Bit 2	-	1	Reserved (Note)
Bit 1	-	1	Reserved (Note)
Bit 0	-	0	Reserved (Note)

Note: Writing to this register will configure byte count and how many bytes will be read back, default is 6 bytes.

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default



Byte 7: Latch Inputs Readback Register

Bit	PWD	Description
Bit 7	0	(Reserved)
Bit 6	0	(Reserved)
Bit 5	X	(SEL24_48#)#
Bit 4	X	FS4#
Bit 3	X	FS3#
Bit 2	X	FS2#
Bit 1	X	FS1#
Bit 0	X	FS0#

Byte 8: VCO Control Selection Bit & Watchdog Timer Control Register

Bit	PWD	Description
Bit 7	0	0=Hw/B0 freq / 1=B14&15 freq
Bit 6	0	WD Enable 0=disable / 1=enable
Bit 5	0	WD Status 0=normal / 1=alarm
Bit 4	0	WD Safe Frequency, FS4
Bit 3	0	WD Safe Frequency, FS3
Bit 2	0	WD Safe Frequency, FS2
Bit 1	0	WD Safe Frequency, FS1
Bit 0	0	WD Safe Frequency, FS0

Note: FS values in bit [0:4] will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

Byte 9: Watchdog Timer Count Register

Bit	PWD	Description
Bit 7	0	The decimal representation of these 8 bits correspond to 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 15 X 290ms = 4.4 seconds. Note, this timer does not control the RESET# signal (pin 30) in case of the frequency ratio change.
Bit 6	0	
Bit 5	0	
Bit 4	0	
Bit 3	1	
Bit 2	1	
Bit 1	1	
Bit 0	1	

Byte 10: ICS Reserved Register

Bit	PWD	Description
Bit 7	0	(Reserved)
Bit 6	0	(Reserved)
Bit 5	0	(Reserved)
Bit 4	0	(Reserved)
Bit 3	0	(Reserved)
Bit 2	0	(Reserved)
Bit 1	0	(Reserved)
Bit 0	0	(Reserved)

Note: This is an unused register. Writing to this register will not affect device performance or functionality.

Byte 11: Vender ID & Device ID Register

Bit	PWD	Description
Bit 7	0	Device ID
Bit 6	0	Device ID
Bit 5	1	Device ID
Bit 4	1	Device ID
Bit 3	0	Vendor ID
Bit 2	0	Vendor ID
Bit 1	0	Vendor ID
Bit 0	1	Vendor ID

Note: ICS Vendor ID is 0001 as in Number 1 in frequency generation.

Byte 12: Revision ID Register

Bit	PWD	Description
Bit 7	X	Revision ID
Bit 6	X	Revision ID
Bit 5	X	Revision ID
Bit 4	X	Revision ID
Bit 3	X	Revision ID
Bit 2	X	Revision ID
Bit 1	X	Revision ID
Bit 0	X	Revision ID

Note: Device ID and Revision ID values will be based on individual device and its revision.

Notes:

1. PWD = Power on Default



Byte 13: ICS Reserved Register

Bit	PWD	Description
Bit 7	0	(Reserved)
Bit 6	0	(Reserved)
Bit 5	0	(Reserved)
Bit 4	0	W0 timer base select 0=290ms 1=0.5ms
Bit 3	0	(Reserved)
Bit 2	0	(Reserved)
Bit 1	0	(Reserved)
Bit 0	0	(Reserved)

Note: DON'T write a '1' into this register, it will cause malfunction.

Byte 14: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit0
Bit 6	X	REF Divider Bit6
Bit 5	X	REF Divider Bit5
Bit 4	X	REF Divider Bit4
Bit 3	X	REF Divider Bit3
Bit 2	X	REF Divider Bit2
Bit 1	X	REF Divider Bit1
Bit 0	X	REF Divider Bit0

Note: The decimal representation of these 7 bits (Byte 14 [6:0]) + 2 is equal to the REF divider value .

Byte 15: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit8
Bit 6	X	VCO Divider Bit7
Bit 5	X	VCO Divider Bit6
Bit 4	X	VCO Divider Bit5
Bit 3	X	VCO Divider Bit4
Bit 2	X	VCO Divider Bit3
Bit 1	X	VCO Divider Bit2
Bit 0	X	VCO Divider Bit1

Note: The decimal representation of these 9 bits (Byte 15 bit [7:0] & Byte 14 bit [7]) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program $36 - 8 = 28$, namely, 0, 00011100 into byte 15 bit & byte 14 bit 7.

VCO Programming Constrains

VCO Frequency 150MHz to 500MHz

VCO Divider Range 8 to 519

REF Divider Range 2 to 129

Phase Detector Stability 0.3536 to 1.4142

Useful Formula

VCO Frequency = $14.31818 \times \text{VCO/REF divider value}$

Phase Detector Stabiliy = $14.038 \times (\text{VCO divider value})^{-0.5}$

To program the VCO frequency for over-clocking.

0. Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.
1. Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.
2. Write 0001, 0111 (17H) to byte 6 for readback of 23 bytes (byte 0-22).
3. Read back byte 16-24 and copy values in these registers.
4. Re-initialize the write sequence.
5. Write a '1' to byte 8 bit 7 indicating you want to use byte 14 and 15 to control the VCO frequency.
6. Write to byte 14 & 15 with the desired VCO & REF divider values.
7. Write to byte 16 to 22 with the values you copy from step 3. This maintains the output divider mux controls the same gear ratio.
8. The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 14 and 15 unless the system is to reboot.



Note:

1. User needs to ensure step 3 & 7 is carried out. Systems with wrong spread percentage and/or group to group divider ratio programmed into bytes 16-20 could be unstable. Step 3 & 7 assure the correct spread and gear ratio.
2. If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.
3. Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use $14.31818\text{MHz} \times \text{VCO/REF divider values}$ to calculate the VCO frequency (MHz).
4. Users can also utilize software utility provided to program VCO frequency from ICS Application Engineering.
5. Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spread amount desired. See Application note for software support.

Byte 16: Spread Spectrum Control Register

Bit	PWD	Description
Bit 7	X	Spread Spectrum Bit7
Bit 6	X	Spread Spectrum Bit6
Bit 5	X	Spread Spectrum Bit5
Bit 4	X	Spread Spectrum Bit4
Bit 3	X	Spread Spectrum Bit3
Bit 2	X	Spread Spectrum Bit2
Bit 1	X	Spread Spectrum Bit1
Bit 0	X	Spread Spectrum Bit0

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 17: Spread Spectrum Control Register

Bit	PWD	Description
Bit 7	X	Divider control Bit26
Bit 6	0	Divider control Bit25
Bit 5	X	Divider control Bit24
Bit 4	X	Spread Spectrum Bit12
Bit 3	X	Spread Spectrum Bit11
Bit 2	X	Spread Spectrum Bit10
Bit 1	X	Spread Spectrum Bit9
Bit 0	X	Spread Spectrum Bit8

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 18: Output Dividers Control Register

Bit	PWD	Description
Bit 7	X	Output Divider MUX Control Bit7
Bit 6	X	Output Divider MUX Control Bit6
Bit 5	X	Output Divider MUX Control Bit5
Bit 4	X	Output Divider MUX Control Bit4
Bit 3	X	Output Divider MUX Control Bit3
Bit 2	X	Output Divider MUX Control Bit2
Bit 1	X	Output Divider MUX Control Bit1
Bit 0	X	Output Divider MUX Control Bit0

Note: Changing bits in these registers results in frequency divider ratio changes. Incorrect configuration of group gear ratio can cause system malfunction.

Byte 19: Output Dividers Control Register

Bit	PWD	Description
Bit 7	X	Output Divider MUX Control Bit15
Bit 6	X	Output Divider MUX Control Bit14
Bit 5	X	Output Divider MUX Control Bit13
Bit 4	X	Output Divider MUX Control Bit12
Bit 3	X	Output Divider MUX Control Bit11
Bit 2	X	Output Divider MUX Control Bit10
Bit 1	X	Output Divider MUX Control Bit9
Bit 0	X	Output Divider MUX Control Bit8

Note: Changing bits in these registers results in frequency divider ratio changes. Incorrect configuration of group gear ratio can cause system malfunction.

Notes:

1. PWD = Power on Default
2. The power on default for byte 16-20 depends on the hardware (latch inputs FS[0:4]) or IIC (Byte 0 bit [1:7]) setting. Be sure to read back and re-write the values of these 5 registers when VCO frequency change is desired for the first pass.



Byte 20: Output Dividers Control Register

Bit	PWD	Description
Bit 7	X	Output Divider MUX Control Bit23
Bit 6	X	Output Divider MUX Control Bit22
Bit 5	X	Output Divider MUX Control Bit21
Bit 4	X	Output Divider MUX Control Bit20
Bit 3	X	Output Divider MUX Control Bit19
Bit 2	X	Output Divider MUX Control Bit18
Bit 1	X	Output Divider MUX Control Bit17
Bit 0	X	Output Divider MUX Control Bit16

Note: Changing bits in these registers results in frequency divider ratio changes. Incorrect configuration of group gear ratio can cause system malfunction.

Byte 22: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	0	24,48MHz 0=Normal, 1=Weak
Bit 6	0	IOAPIC/REF 0=Normal, 1=Weak
Bit 5	0	PCI 0=Normal, 1=Weak
Bit 4	0	SDRAM_F 0=Normal, 1=Weak
Bit 3	0	SDRAM [0:11] 0=Normal, 1=Weak
Bit 2	0	3V66 0=Normal, 1=Weak
Bit 1	0	CPU1 0=Normal, 1=Weak
Bit 0	0	CPU0 0=Normal, 1=Weak

Notes:

1. PWD = Power on Default

Byte 21: ICS Reserved Register

Bit	PWD	Description
Bit 7	1	3V66 to PCI Skew Bit3
Bit 6	0	3V66 to PCI Skew Bit2
Bit 5	1	3V66 to PCI Skew Bit1
Bit 4	1	3V66 to PCI Skew Bit0
Bit 3	0	3V66 to IOAPIC Skew Bit 3
Bit 2	1	3V66 to IOAPIC Skew Bit 2
Bit 1	1	3V66 to IOAPIC Skew Bit 1
Bit 0	0	3V66 to IOAPIC Skew Bit 0

Note: Each increment or decrement of bit 4 to 7 will introduce 100ps delay or advance on all of the above clocks.

Notes:

1. PWD = Power on Default
2. The power on default for byte 16-20 depends on the hardware (latch inputs FS[0:4]) or I²C (Byte 0 bit [1:7]) setting. Be sure to read back and re-write the values of these 5 registers when VCO frequency change is desired for the first pass.
3. If Byte 8 bit 7 is driven to "1" meaning programming is intended, Byte 21-22 will lose their default power up value.



Absolute Maximum Ratings

Core Supply Voltage	4.6 V
I/O Supply Voltage	3.6V
Logic Inputs	GND -0.5 V to V _{DD} +0.5 V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Case Temperature	115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Timing Relationship Table¹

Group	CPU 66MHz SDRAM 100MHz		CPU 100MHz SDRAM 100MHz		CPU 133MHz SDRAM 100MHz		CPU 133MHz SDRAM 133MHz	
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM	2.5ns	500ps	5.0ns	500ps	0.0ns	500ps	3.75ns	500ps
CPU to 3V66	7.5ns	500ps	5.0ns	500ps	0.0ns	500ps	0.0ns	500ps
SDRAM to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps	3.75ns	500ps
3V66 to PCI	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5 -3.5ns	500ps
PCI to PCI	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns
USB & DOT	Asynch	N/A	Asynch	N/A	Asynch	N/A	Asynch	N/A

Electrical Characteristics - Input/Supply/Common Output Parameters

TA = 0 - 70° C; Supply Volt age VDD = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V _{IH}		2		V _{DD} +0.3	V
Input Low Voltage	V _{IL}		V _{SS} -0.3		0.8	V
Input High Current	I _{IH}	V _{IN} = VDD			5	A
Input Low Current	I _{IL1}	V _{IN} =0 V;Inputs with no pull-up resistors	-5			uA
Input Low Current	I _{IL2}	V _{IN} =0 V; Inputs with pull-up resistors	-200			uA
Supply Current	I _{DD3.3OP100}	C _L =30 pF		346	400	mA
Power Down	PD			4.3	600	mA
Input frequency	F _i	V _{DD} = 3.3 V;	12	14.318	16	MHz
	C _{IN}	Logic Inputs			5	pF
Input Capacitance ¹	C _{IN}	Logic Inputs			5	pF
	C _{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization ¹	T _{STAB}	From V _{DD} = 3.3 V to 1% target Freq.			3	ms

¹ Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$; $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance ¹	R_{DSP2B}	$V_O = V_{DD}^*(0.5)$	13.5	20	45	Ω
Output Impedance ¹	R_{DSN2B}	$V_O = V_{DD}^*(0.5)$	13.5	27	45	Ω
Output High Voltage	V_{OH2B}	$I_{OH} = -1 \text{ mA}$	2	2.5		V
Output Low Voltage	V_{OL2B}	$I_{OL} = 1 \text{ mA}$		0.18	0.4	V
Output High Current	I_{OH2B}	$V_{OH @ MIN} = 1.0 \text{ V}$		-51	-27	mA
		$V_{OH @ MAX} = 2.375 \text{ V}$	-27	-11		
Output Low Current	I_{OL2B}	$V_{OL @ MIN} = 1.2 \text{ V}$	27	41		mA
		$V_{OL @ MAX} = 0.3 \text{ V}$		15	30	
Rise Time ¹	t_{r2B}	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.0 \text{ V}$	0.4	1	1.6	ns
Fall Time ¹	t_{f2B}	$V_{OH} = 2.0 \text{ V}, V_{OL} = 0.4 \text{ V}$	0.4	1	1.6	ns
Duty Cycle ¹	d_{t2B}	$V_T = 1.25 \text{ V}$	45	49	55	%
Skew window ¹	t_{sk2B}	$V_T = 1.25 \text{ V}$		40	175	ps
Jitter, Cycle-to-cycle ¹	$t_{jyc-cyc}$	$V_T = 1.25 \text{ V}, \text{CPU}=66 \text{ MHz}$		245	250	ps
		$V_T = 1.25 \text{ V}, \text{CPU}=100 \text{ MHz}$		160	250	
		$V_T = 1.25 \text{ V}, \text{CPU}=133 \text{ MHz}$		290	250	

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1B} ¹	$V_O = V_{DD}^*(0.5)$	12	17.4	55	Ω
Output Impedance	R_{DSN1B} ¹	$V_O = V_{DD}^*(0.5)$	12	22.4	55	Ω
Output High Voltage	V_{OH1}	$I_{OH} = -1 \text{ mA}$	2.4	3.3		V
Output Low Voltage	V_{OL1}	$I_{OL} = 1 \text{ mA}$		0.009	0.55	V
Output High Current	I_{OH1}	$V_{OH @ MIN} = 1.0 \text{ V}$		-68	-29	mA
		$V_{OH @ MAX} = 3.135 \text{ V}$	-27	-14		
Output Low Current	I_{OL1}	$V_{OL @ MIN} = 1.95 \text{ V}$	29	77		mA
		$V_{OL @ MAX} = 0.4 \text{ V}$		24	27	
Rise Time ¹	t_{r1}	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$	0.5	1.4	2	ns
Fall Time ¹	t_{f1}	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$	0.5	1.7	2	ns
Duty Cycle ¹	d_{t1}	$V_T = 1.5 \text{ V}$	45	49	55	%
Skew window ¹	t_{sk1}	$V_T = 1.5 \text{ V}$		35	175	ps
Jitter, Cycle-to-cycle ¹	$t_{jyc-cyc1}$	$V_T = 1.5 \text{ V}$		292	500	ps

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - IOAPIC

T_A = 0 - 70°C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R _{DSP4B} ¹	V _O = V _{DD} *(0.5)	9	28	30	Ω
Output Impedance	R _{DNS4B} ¹	V _O = V _{DD} *(0.5)	9	28	30	Ω
Output High Voltage	V _{OH4B}	I _{OH} = -1 mA	2	2.4		V
Output Low Voltage	V _{OL4B}	I _{OL} = 1 mA		0.25	0.4	V
Output High Current	I _{OH4B}	V _{OH @ MIN} = 1.0 V		-62	-27	mA
		V _{OH @ MAX} = 2.375 V	-27	-12		
Output Low Current	I _{OL4B}	V _{OL @ MIN} = 1.2 V	27	35		mA
		V _{OL @ MAX} = 0.3 V		8	30	
Rise Time ¹	t _{r4B}	V _{OL} = 0.4 V, V _{OH} = 2.0 V	0.4	1.45	1.6	ns
Fall Time ¹	t _{f4B}	V _{OH} = 2.0 V, V _{OL} = 0.4 V	0.4	0.97	1.6	ns
Duty Cycle ¹	d _{t4B}	V _T = 1.25 V	45	49.3	55	%
Jitter, Cycle-to-cycle ¹	t _{jcc-cyc4B}	V _T = 1.25 V		130	500	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 20-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R _{DSP3B} ¹	V _O = V _{DD} *(0.5)	10	16	24	Ω
Output Impedance	R _{DNS3B} ¹	V _O = V _{DD} *(0.5)	10	17.5	24	Ω
Output High Voltage	V _{OH3}	I _{OH} = -1 mA	2.4	3.3		V
Output Low Voltage	V _{OL3}	I _{OL} = 1 mA		0.01	0.4	V
Output High Current	I _{OH3}	V _{OH @ MIN} = 2.0 V		-70	-46	mA
		V _{OH @ MAX} = 3.135 V	-54	-29		
Output Low Current	I _{OL3}	V _{OL @ MIN} = 1.0 V	54	90		mA
		V _{OL @ MAX} = 0.4 V		28	53	
Rise Time ¹	t _{r3}	V _{OL} = 0.4 V, V _{OH} = 2.4 V	0.4	0.9	1.6	ns
Fall Time ¹	t _{f3}	V _{OH} = 2.4 V, V _{OL} = 0.4 V	0.4	0.8	1.6	ns
Duty Cycle ¹	d ₃	V _T = 1.5 V	45	49.2	55	%
Skew window ¹	t _{sk3}	V _T = 1.5 V		83	250	ps
Jitter, Cycle-to-cycle ¹	t _{jcc-cyc3}	V _T = 1.5 V, CPU=66,100,133 MHz		214	250	ps

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 10\text{-}30 \text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1B}^1	$V_O = V_{DD} \cdot (0.5)$	12	17.4	55	Ω
Output Impedance	R_{DSN1B}^1	$V_O = V_{DD} \cdot (0.5)$	12	22.4	55	Ω
Output High Voltage	V_{OH1}	$I_{OH} = -1 \text{ mA}$	2.4	3.3		V
Output Low Voltage	V_{OL1}	$I_{OL} = 1 \text{ mA}$		0.009	0.55	V
Output High Current	I_{OH1}	$V_{OH @ MIN} = 1.0 \text{ V}$		-67	-29	mA
		$V_{OH @ MAX} = 3.135 \text{ V}$	-27	-14		
Output Low Current	I_{OL1}	$V_{OL @ MIN} = 1.95 \text{ V}$	29	77		mA
		$V_{OL @ MAX} = 0.4 \text{ V}$		24	27	
Rise Time ¹	t_{r1}	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$	0.5	1.7	2.5	ns
Fall Time ¹	t_{f1}	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$	0.5	1.9	2.5	ns
Duty Cycle ¹	d_{t1}	$V_T = 1.5 \text{ V}$	45	51	55	%
Skew window ¹	t_{sk1}	$V_T = 1.5 \text{ V}$		213	500	ps
Jitter, Cycle-to-cycle ¹	$t_{jyc-cyc1}$	$V_T = 1.5 \text{ V}$		285	500	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5B}^1	$V_O = V_{DD} \cdot (0.5)$	15	18	60	Ω
Output Impedance	R_{DSN5B}^1	$V_O = V_{DD} \cdot (0.5)$	15	18.75	60	Ω
Output High Voltage	V_{OH15}	$I_{OH} = -1 \text{ mA}$	2.4	3.27		V
Output Low Voltage	V_{OL5}	$I_{OL} = 1 \text{ mA}$		0.025	0.4	V
Output High Current	I_{OH5}	$V_{OH @ MIN} = 1.0 \text{ V}$		-76	-33	mA
		$V_{OH @ MAX} = 3.135 \text{ V}$	-33	-12		
Output Low Current	I_{OL5}	$V_{OL @ MIN} = 1.95 \text{ V}$		71	29	mA
		$V_{OL @ MAX} = 0.4 \text{ V}$	27	22		
Rise Time ¹	t_{r5}	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$	0.4	1	4	ns
Fall Time ¹	t_{f5}	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$	0.4	1.7	4	ns
Duty Cycle ¹	d_{t5}	$V_T = 1.5 \text{ V}$	45	54.1	55	%

¹Guaranteed by design, not 100% tested in production.



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS94203 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

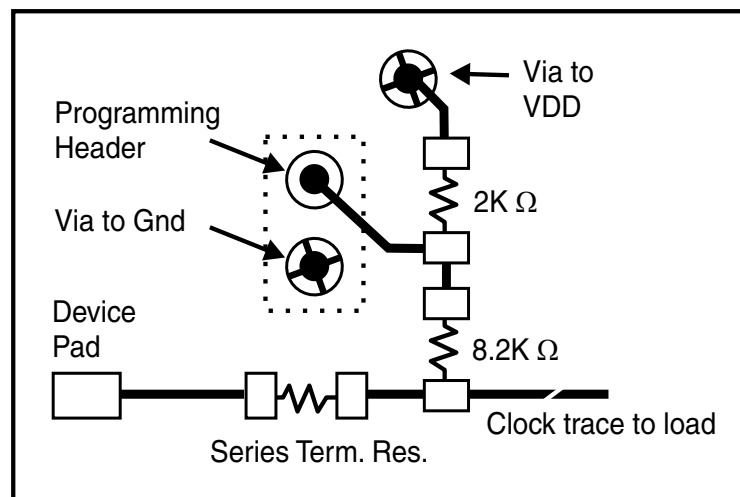
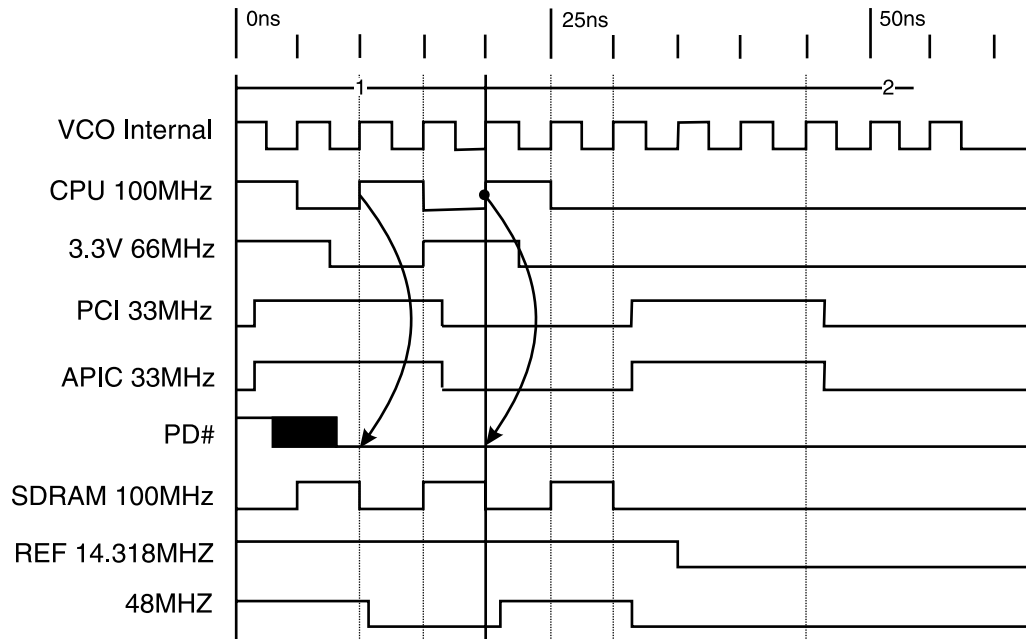


Fig. 1

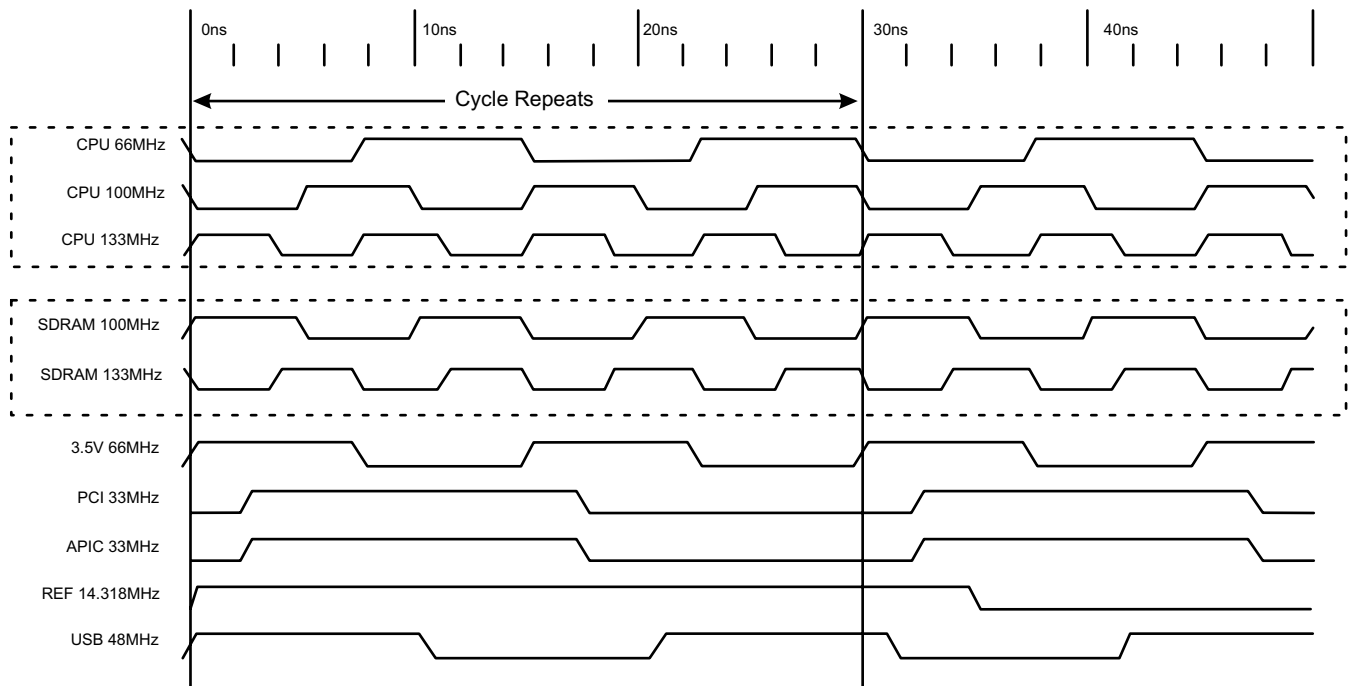


Power Down Waveform

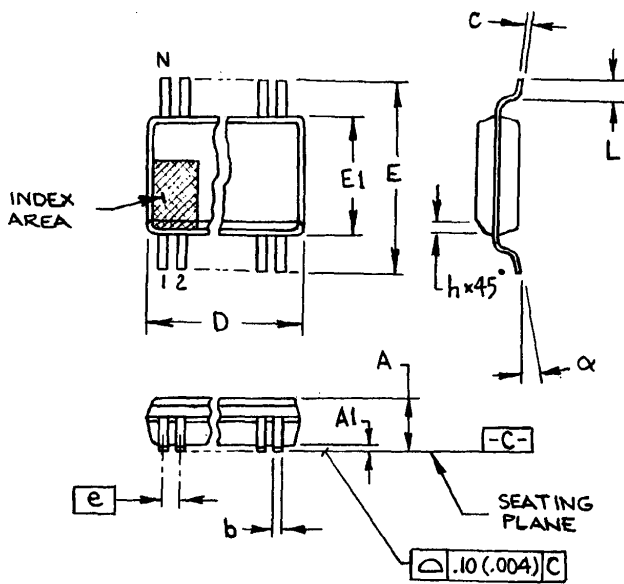


Note

1. After PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low transition.
2. Power-up latency <3ms.
3. Waveform shown for 100MHz



Group Offset Waveforms



300 mil SSOP

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.398	9.652	.370	.380
34	11.303	11.557	.445	.455
48	15.748	16.002	.620	.630
56	18.288	18.542	.720	.730
64	20.828	21.082	.820	.830

Ordering Information

ICS94203yF-T

Example:

ICS XXXX y F - T

