



# AMD-K7™ System Clock Chip

**Recommended Application:**  
AMD 750/760 style chipset

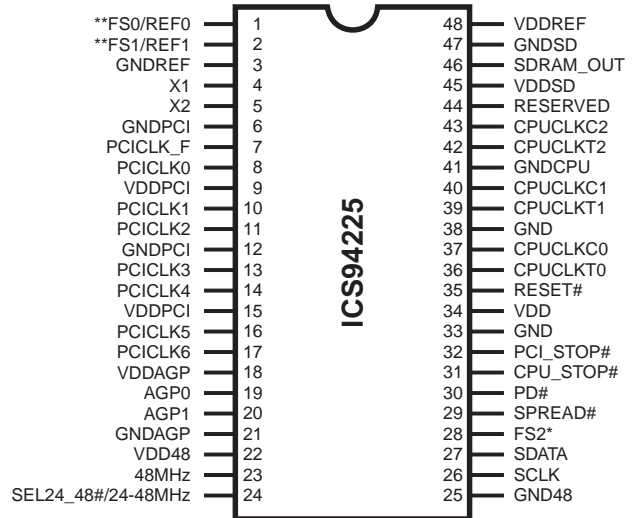
**Output Features:**

- 3 differential pair open drain CPU clocks (1.5V external pull-up; up to 150MHz achievable through I<sup>2</sup>C)
- 2 - AGPCLK @ 3.3V
- 8 - PCI @3.3V, including 1 free running
- 1 - 48MHz @ 3.3V
- 1 - 24/48MHz @ 3.3V
- 2- REF @3.3V, 14.318MHz.

**Features:**

- Programmable output frequency
- Programmable output rise/fall time
- Programmable group skew
- Real time system reset output
- Spread spectrum for EMI control typically by 7dB to 8dB, with programmable spread percentage
- Watchdog timer technology to reset system if over-clocking causes malfunction
- Uses external 14.318MHz crystal

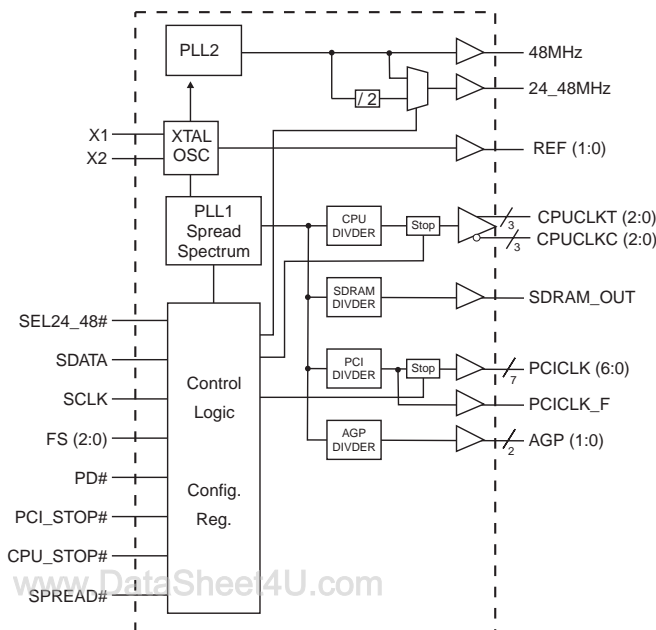
**Pin Configuration**



**48-Pin 300mil SSOP**

\* Internal 120K pullup resistor on indicated inputs  
\*\* Internal 240K pullup resistor on indicated inputs

**Block Diagram**



**Functionality**

FS2	FS1	FS0	CPU, SDRAM	PCI	AGP
0	0	0	133.33	33.33	66.67
0	0	1	95	31.67	63.33
0	1	0	100.99	33.66	67.33
0	1	1	115	38.33	76.67
1	0	0	100.7	33.57	67.13
1	0	1	103	34.33	68.67
1	1	0	105	35.00	70.00
1	1	1	110	36.67	73.33

**Power Groups**

VDD48, GND48 = 48MHz, PLL2  
VDDREF, GNDREF= REF, X1, X2  
VDD, GND = PLL Core



## General Description

The **ICS94225** is a main clock synthesizer chip for AMD-K7 based systems with AMD 750/760 style chipsets. This provides all clocks required for such a system.

The **ICS94225** belongs to ICS new generation of programmable system clock generators. It employs serial programming I<sup>2</sup>C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

## Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2,1	FS (1:0)	IN	Frequency Select pins, has pull-up to VDD
	REF (1:0)	OUT	14.318MHz clock output
3, 6, 21, 25, 33, 38, 41, 47	GND	PWR	Ground
4	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
5	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
7	PCICLK_F	OUT	Free Running PCI output. Not affected by the PCI_STOP# input.
17, 16, 14, 13, 11, 10, 8	PCICLK (6:0)	OUT	PCI clock outputs. TTL compatible 3.3V
9, 15	VDDPCI	PWR	Power for PCICLK outputs, nominally 3.3V
18	VDDAGP	PWR	Power for AGP outputs, nominally 3.3V
20, 19	AGP (1:0)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
34	VDD	PWR	Isolated power for core, nominally 3.3V
22	VDD48	PWR	Power for 48MHz and 24MHz outputs nominally 3.3V
23	48MHz	OUT	48MHz output
24	SEL24-48#	IN	Selects 24 or 48MHz output for pin 24 Low = 48MHz High = 24MHz
	24-48MHz	OUT	Fixed clock out selectable through SEL24-48#
26	SCLK	IN	Clock pin of I <sup>2</sup> C circuitry 5V tolerant
27	SDATA	I/O	Data pin for I <sup>2</sup> C circuitry 5V tolerant
28	FS2	IN	Frequency Select pin, has pull-up to VDD
29	SPREAD#	IN	Enables Spread Spectrum feature when LOW. Down Spread 0.5% modulation frequency =50KHz
30	PD#	IN	Powers down chip, active low. Internal PLL & all outputs are disabled.
31	CPU_STOP#	IN	Halts CPUCLKs. CPUCLKT is driven LOW whereas CPUCLKC is driven HIGH when this pin is asserted (Active LOW).
32	PCI_STOP#	IN	Halts PCI Bus at logic "0" level when driven low. PCICLK_F is not affected by this pin
35	RESET#	OUT	Real time system reset signal for watchdog timer timeout. This signal is active low.
46	SDRAM_OUT	OUT	Reference clock for SDRAM zero delay buffer
44	RESERVED	N/C	Future CPU power rail
42, 39, 36	CPUCLKT (2:0)	OUT	"True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
43, 40, 37	CPUCLKC (2:0)	OUT	"Complementary" clocks of differential pair CPU output. These open drain outputs need an external 1.5V pull_up.
45	VDDSD	PWR	Power for SDRAM_OUT pin. Nornally 3.3V
48	VDDREF	PWR	Power for REF, X1, X2, nominally 3.3V



**Byte 1: Reserved Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	-	1	(Reserved)
Bit 0	-	1	(Reserved)

**Byte 2: Reserved, Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	-	1	(Reserved)
Bit 0	-	1	(Reserved)

**Byte 3: Reserved Active/Inactive Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	-	1	(Reserved)
Bit 0	-	1	(Reserved)

**Byte 4: Clock Control Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
7	1	1	REF0
6	23	1	24MHz/48MHz
5	22	1	USB0
4	20	1	AGP1
3	19	1	AGP0
2	42, 43	1	CPUCLKC/T2
1	39, 40	1	CPUCLKC/T1
0	36, 37	1	CPUCLKC/T0

**Byte 5: PCI Clock Control Register  
(1= enable, 0 = disable)**

BIT	PIN#	PWD	DESCRIPTION
7	2	1	REF1
6	17	1	PCICLK6
5	16	1	PCICLK5
4	14	1	PCICLK4
3	13	1	PCICLK3
2	11	1	PCICLK2
1	10	1	PCICLK1
0	8	1	PCICLK0

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.



## Byte 6: SDRAM Clock & Generator Mode Control Register

Bit	Description								PWD
7	Spread Spectrum enable (+/- 0.25% center spread) 0=OFF 1=ON								0
6:2	Bit 3	Bit 2	FS2 Bit 6	FS1 Bit 5	FS0 Bit 4	CPU, SDRAM	PCI	AGP	0010 Note1
	0	0	0	0	0	133.33	33.33	66.67	
	0	0	0	0	1	95	31.67	63.33	
	0	0	0	1	0	100.99	33.66	67.33	
	0	0	0	1	1	115	38.33	76.67	
	0	0	1	0	0	100.7	33.57	67.13	
	0	0	1	0	1	103	34.33	68.67	
	0	0	1	1	0	105	35.00	70.00	
	0	0	1	1	1	110	36.67	73.33	
	0	1	0	0	0	102	34.00	68.00	
	0	1	0	0	1	104	34.67	69.33	
	0	1	0	1	0	106	35.33	70.67	
	0	1	0	1	1	107	35.67	71.33	
	0	1	1	0	0	108	36.00	72.00	
	0	1	1	0	1	109	36.33	72.67	
	0	1	1	1	0	90	30.00	60.00	
	0	1	1	1	1	111	37.00	74.00	
	1	0	0	0	0	112	37.33	74.67	
	1	0	0	0	1	113	37.67	75.33	
	1	0	0	1	0	114	38.00	76.00	
	1	0	0	1	1	116	38.67	77.33	
	1	0	1	0	0	117	39.00	78.00	
	1	0	1	0	1	118	39.33	78.67	
	1	0	1	1	0	119	39.67	79.33	
	1	0	1	1	1	120	30.00	60.00	
1	1	0	0	0	142	35.50	71.00		
1	1	0	0	1	144	36.00	72.00		
1	1	0	1	0	146	36.50	73.00		
1	1	0	1	1	138	34.50	69.00		
1	1	1	0	0	136	34.00	68.00		
1	1	1	0	1	135	33.75	67.50		
1	1	1	1	0	140	35.00	70.00		
1	1	1	1	1	150	37.50	75.00		
1	0 - Frequency is selected by hardware select, latched input; Spread controlled by pin 29 1 - Frequency is selected by Bit (6:2); Spread controlled by Bit								0
0	0 - SDRAM_OUT Disable 1 - SDRAM_OUT Enable								1

### Notes:

1. Default at power-up will be latched logic inputs to define frequency, as displayed by Bit 1.
2. PWD = Power-Up Default



**Byte 7: Vendor ID and Revision ID Register**

Bit	PWD	Description
Bit 7	0	Vendor ID
Bit 6	0	Vendor ID
Bit 5	1	Vendor ID
Bit 4	X	Revision ID
Bit 3	X	Revision ID
Bit 2	X	Revision ID
Bit 1	X	Revision ID
Bit 0	X	Revision ID

**Byte 8: Byte Count and Read Back Register**

Bit	PWD	Description
Bit 7	0	Reserved
Bit 6	0	Reserved
Bit 5	0	Reserved
Bit 4	0	Reserved
Bit 3	1	Reserved
Bit 2	0	Reserved
Bit 1	0	Reserved
Bit 0	0	Reserved

**Byte 9: Watchdog Timer Count Register**

Bit	PWD	Description
Bit 7	0	The decimal representation of these 8 bits correspond to 290ms or 1ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 290ms.
Bit 6	0	
Bit 5	0	
Bit 4	0	
Bit 3	0	
Bit 2	0	
Bit 1	0	
Bit 0	0	

**Byte 10: VCO Control Selection Bit & Watchdog Timer Control Register**

Bit	PWD	Description
Bit 7	0	0=Hw/B0 freq / 1=B11 & 12 freq
Bit 6	0	WD Enable 0=disable / 1=enable
Bit 5	0	WD Status 0=normal / 1=alarm
Bit 4	1	WD Safe Frequency, Byte 0 bit 2
Bit 3	0	WD Safe Frequency, FS3
Bit 2	0	WD Safe Frequency, FS2
Bit 1	0	WD Safe Frequency, FS1
Bit 0	0	WD Safe Frequency, FS0

Note: FS values in bit [0:4] will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

**Byte 11: VCO Frequency Control Register**

Bit	PWD	Description
Bit 7	X	VCO Divider Bit0
Bit 6	X	REF Divider Bit6
Bit 5	X	REF Divider Bit5
Bit 4	X	REF Divider Bit4
Bit 3	X	REF Divider Bit3
Bit 2	X	REF Divider Bit2
Bit 1	X	REF Divider Bit1
Bit 0	X	REF Divider Bit0

Note: The decimal representation of these 7 bits (Byte 11 [6:0]) + 2 is equal to the REF divider value .

**Notes:**

1. PWD = Power on Default

**Byte 12: VCO Frequency Control Register**

Bit	PWD	Description
Bit 7	X	VCO Divider Bit8
Bit 6	X	VCO Divider Bit7
Bit 5	X	VCO Divider Bit6
Bit 4	X	VCO Divider Bit5
Bit 3	X	VCO Divider Bit4
Bit 2	X	VCO Divider Bit3
Bit 1	X	VCO Divider Bit2
Bit 0	X	VCO Divider Bit1

Note: The decimal representation of these 9 bits (Byte 12 bit [7:0] & Byte 11 bit [7] ) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program 36 - 8 = 28, namely, 0, 00011100 into byte 12 bit & byte 11 bit 7.



### Byte 13: Spread Spectrum Control Register

Bit	PWD	Description
Bit 7	X	Spread Spectrum Bit7
Bit 6	X	Spread Spectrum Bit6
Bit 5	X	Spread Spectrum Bit5
Bit 4	X	Spread Spectrum Bit4
Bit 3	X	Spread Spectrum Bit3
Bit 2	X	Spread Spectrum Bit2
Bit 1	X	Spread Spectrum Bit1
Bit 0	X	Spread Spectrum Bit0

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

### Byte 14: Spread Spectrum Control Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Spread Spectrum Bit12
Bit 3	X	Spread Spectrum Bit11
Bit 2	X	Spread Spectrum Bit10
Bit 1	X	Spread Spectrum Bit9
Bit 0	X	Spread Spectrum Bit8

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

### Byte 15: Output Skew Control

Bit	PWD	Description
Bit 7	X	CPUCLKC2/T2 Skew Control
Bit 6	X	
Bit 5	X	
Bit 4	X	
Bit 3	X	PCICLK_F Skew Control
Bit 2	X	
Bit 1	X	
Bit 0	X	

### Byte 16: Output Skew Control

Bit	PWD	Description
Bit 7	X	PCICLK (6:0) Skew Control
Bit 6	X	
Bit 5	X	
Bit 4	X	
Bit 3	X	AGP (3:0) Skew Control
Bit 2	X	
Bit 1	X	
Bit 0	X	

### Byte 17: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	X	CPUCLKT0
Bit 6	X	CPUCLKC0
Bit 5	X	CPUCLKT1
Bit 4	X	CPUCLKC1
Bit 3	X	AGP (2:0) Slew Rate Control
Bit 2	X	
Bit 1	X	3V66 (1:0) Slew Rate Control
Bit 0	X	

### Byte 18: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	X	PCI (3:0): Slew Rate Control
Bit 6	X	
Bit 5	X	PCI (6:4): Slew Rate Control
Bit 4	X	
Bit 3	X	48MHz: Slew Rate Control
Bit 2	X	
Bit 1	X	24MHz: Slew Rate Control
Bit 0	X	

#### Notes:

1. PWD = Power on Default
2. The power on default for byte 13-20 depends on the hardware (latch inputs FS[0:4]) or I<sup>2</sup>C (Byte 0 bit [1:7]) setting. Be sure to read back and re-write the values of these 8 registers when VCO frequency change is desired for the first pass.
3. If Byte 8 bit 7 is driven to "1" meaning programming is intended, Byte 21-24 will lose their default power up value.



Byte 19: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Byte 20: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Note: Byte 19 and 20 are reserved registers, these are unused registers writing to these registers will not affect device performance or functionality.

VCO Programming Constrains

- VCO Frequency ..... 150MHz to 500MHz
- VCO Divider Range ..... 8 to 519
- REF Divider Range ..... 2 to 129
- Phase Detector Stability ..... 0.3536 to 1.4142

Useful Formula

- VCO Frequency = 14.31818 x VCO/REF divider value
- Phase Detector Stabiliy = 14.038 x (VCO divider value)<sup>-0.5</sup>

To program the VCO frequency for over-clocking.

- Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.
- Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.
- Write 0001, 1001 (19H) to byte 8 for readback of 21 bytes (byte 0-20).
- Read back byte 11-20 and copy values in these registers.
- Re-initialize the write sequence.
- Write a '1' to byte 9 bit 7 and write to byte 11 & 12 with the desired VCO & REF divider values.
- Write to byte 13 to 20 with the values you copy from step 3. This maintains the output spread, skew and slew rate.
- The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 11 and 12 unless the system is to reboot.

Note:

- User needs to ensure step 3 & 7 is carried out. Systems with wrong spread percentage and/or group to group skew relation programmed into bytes 13-16 could be unstable. Step 3 & 7 assure the correct spread and skew relationship.
- If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.
- Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use 14.31818MHz x VCO/REF divider values to calculate the VCO frequency (MHz).
- ICS recommends users, to utilize the software utility provided by ICS Application Engineering to program the VCO frequency.
- Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spread amount desired. See Application note for software support.



## Absolute Maximum Ratings

Supply Voltage . . . . .	5.5 V
Logic Inputs . . . . .	GND –0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature . . . . .	0°C to +70°C
Storage Temperature . . . . .	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	$V_{IH}$		2		$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$		$V_{SS} - 0.3$		0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$			5	A
Input Low Current	$I_{IL1}$	$V_{IN} = 0$ V; Inputs with no pull-up resistors	-5			mA
Input Low Current	$I_{IL2}$	$V_{IN} = 0$ V; Inputs with pull-up resistors	-200			
Supply Current	$I_{DD3.30P66}$	$C_L = 0$ pF; Select@ 66MHz		87	180	mA
	$I_{DD3.30P100}$	$C_L = 0$ pF; Select@ 100MHz		91		
	$I_{DD3.30P133}$	$C_L = 0$ pF; Select@ 133MHz		104		
Power Down	PD			3.25	5	mA
Input frequency	$F_i$	$V_{DD} = 3.3$ V	12	14.318	16	MHz
Input Capacitance <sup>1</sup>	$C_{IN}$	Logic Inputs			5	pF
	$C_{INX}$	X1 & X2 pins	27		45	pF
	$T_{STAB}$	From $V_{DD} = 3.3$ V to 1% target Freq.			3	ms
	$t_{CPU-PCI}$	$V_T = 50\%$ to 1.5V	1	2.85	4	ns

<sup>1</sup> Guaranteed by design, not 100% tested in production.





**Electrical Characteristics - USB, REF(1:0)**

TA = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH5</sub>	I <sub>OH</sub> = -12 mA	2.4			V
Output Low Voltage	V <sub>OL5</sub>	I <sub>OL</sub> = 9 mA			0.4	V
Output High Current	I <sub>OH5</sub>	V <sub>OH</sub> = 2.0 V			-22	mA
Output Low Current	I <sub>OL5</sub>	V <sub>OL</sub> = 0.8 V	16			mA
Rise Time <sup>1</sup>	t <sub>r5</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V		0.98	4	ns
Fall Time <sup>1</sup>	t <sub>f5</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V		0.77	4	ns
Duty Cycle <sup>1</sup>	d <sub>t5</sub>	V <sub>T</sub> = 1.5V	45	54	57	%
Jitter, Cycle-to-cycle <sup>1</sup>	t <sub>jcy-cyc2B</sub>	V <sub>T</sub> = 1.5V		471	1100	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - CPUCLK (Open Drain)**

TA = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z <sub>0</sub>	V <sub>O</sub> = V <sub>X</sub>				
Output High Voltage	V <sub>OH2B</sub>	Termination to V <sub>pull-up</sub> (external)	1		1.2	V
Output Low Voltage	V <sub>OL2B</sub>				0.4	V
Output Low Current	I <sub>OL2B</sub>	V <sub>OL</sub> = 0.3 V	18			mA
Rise Time <sup>1</sup>	t <sub>r2B</sub>	V <sub>OL</sub> = 0.3 V, V <sub>OH</sub> = 1.2 V			0.9	ns
Fall Time <sup>1</sup>	t <sub>f2B</sub>	V <sub>OH</sub> = 1.2 V, V <sub>OL</sub> = 0.3 V			0.9	ns
Differential voltage-AC <sup>1</sup>	V <sub>DIF</sub>	Note 2	0.4		V <sub>pu</sub>	V
Differential voltage-DC <sup>1</sup>	V <sub>DIF</sub>	Note 2	0.2		+0.6	V
Differential Crossover	V <sub>X</sub>	Note 3	550		1100	mV
Duty Cycle <sup>1</sup>	d <sub>t2B</sub>	V <sub>T</sub> = 50%	45	51	55	%
Skew <sup>1</sup>	t <sub>sk2B</sub>	V <sub>T</sub> = 50%		46	200	ps
Jitter, Cycle-to-cycle <sup>1</sup>	t <sub>jcy-cyc2B</sub>	V <sub>T</sub> = V <sub>X</sub>		86	250	ps
Jitter, Absolute <sup>1</sup>	t <sub>jabs2B</sub>	V <sub>T</sub> = 50%	-250		250	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V<sub>DIF</sub> specifies the minimum input differential voltages (V<sub>TR</sub>-V<sub>CP</sub>) required for switching, where V<sub>TR</sub> is the "true" input level and V<sub>CP</sub> is the "complement" input level.

3 - V<sub>pullup</sub>(external) = 1.5V, Min = V<sub>pullup</sub>(external)/2-150mV; Max=(V<sub>pullup</sub>(external)/2)+150mV



### Electrical Characteristics - PCICLK\_F, PCICLK(6:0)

TA = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH5</sub>	I <sub>OH</sub> = -11 mA	2.6			V
Output Low Voltage	V <sub>OL5</sub>	I <sub>OL</sub> = 9.4 mA			0.4	V
Output High Current	I <sub>OH5</sub>	V <sub>OH</sub> = 2.0 V			-16	mA
Output Low Current	I <sub>OL5</sub>	V <sub>OL</sub> = 0.8 V	19			mA
Rise Time <sup>1</sup>	t <sub>r5</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V		1.8	2	ns
Fall Time <sup>1</sup>	t <sub>f5</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V		1.8	2	ns
Duty Cycle <sup>1</sup>	d <sub>t5</sub>	V <sub>T</sub> = 1.5V	45	51.7	55	%
Skew <sup>1</sup>	t <sub>sk2B</sub>	V <sub>T</sub> = 1.5V		175	200	ps
Jitter, Cycle-to-cycle <sup>1</sup>	t <sub>jcy-cyc2B</sub>	V <sub>T</sub> = 1.5V		122	500	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - PCICLK\_F, PCICLK(6:0)

TA = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH5</sub>	I <sub>OH</sub> = -11 mA	2.6			V
Output Low Voltage	V <sub>OL5</sub>	I <sub>OL</sub> = 9.4 mA			0.4	V
Output High Current	I <sub>OH5</sub>	V <sub>OH</sub> = 2.0 V			-16	mA
Output Low Current	I <sub>OL5</sub>	V <sub>OL</sub> = 0.8 V	19			mA
Rise Time <sup>1</sup>	t <sub>r5</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V		1.8	2	ns
Fall Time <sup>1</sup>	t <sub>f5</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V		1.8	2	ns
Duty Cycle <sup>1</sup>	d <sub>t5</sub>	V <sub>T</sub> = 1.5V	45	51.7	55	%
Skew <sup>1</sup>	t <sub>sk2B</sub>	V <sub>T</sub> = 1.5V		175	200	ps
Jitter, Cycle-to-cycle <sup>1</sup>	t <sub>jcy-cyc2B</sub>	V <sub>T</sub> = 1.5V		122	500	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - AGP(1:0)**

TA = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH5}$	$I_{OH} = -18 \text{ mA}$	2.6			V
Output Low Voltage	$V_{OL5}$	$I_{OL} = 1.8 \text{ mA}$			0.4	V
Output High Current	$I_{OH5}$	$V_{OH} = 2.0 \text{ V}$			-16	mA
Output Low Current	$I_{OL5}$	$V_{OL} = 0.8 \text{ V}$	19			mA
Rise Time <sup>1</sup>	$t_{r5}$	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$		1.05	1.6	ns
Fall Time <sup>1</sup>	$t_{f5}$	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$		1.27	1.6	ns
Duty Cycle <sup>1</sup>	$d_{t5}$	$V_T = 50\%$	45	50.4	55	%
Skew <sup>1</sup> (window)	$T_{sk}^1$	$V_T = 50\%$		12	200	ps
Jitter, Cycle-to-cycle <sup>1</sup>	$t_{jyc-cyc2B}$	$V_T = 50\%$		268	500	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.**Electrical Characteristics - SDRAM\_OUT**

TA = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH3}$	$I_{OH} = -11 \text{ mA}$	2			V
Output Low Voltage	$V_{OL3}$	$I_{OL} = 11 \text{ mA}$			0.4	V
Output High Current	$I_{OH3}$	$V_{OH} = 2.0 \text{ V}$			-12	mA
Output Low Current	$I_{OL3}$	$V_{OL} = 0.8 \text{ V}$	12			mA
Rise Time <sup>1</sup>	$t_{r3}$	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}@100\text{MHz}$		0.83	1.6	ns
Fall Time <sup>1</sup>	$t_{f3}$	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}@100\text{MHz}$		0.71	1.6	ns
Duty Cycle <sup>1</sup>	$d_{t3}$	$V_T = 50\%$	45	50.8	55	%
Jitter, Cycle-to-cycle <sup>1</sup>	$t_{jyc-cyc3B}$	$V_T = 50\% @ 100\text{MHz}$		240	250	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## General I<sup>2</sup>C serial interface information for the ICS94225

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending *Byte 0 through Byte 20* (see Note)
- ICS clock will *acknowledge* each byte *one at a time*
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 <sub>(H)</sub>	
	<b>ACK</b>
Dummy Command Code	
	<b>ACK</b>
Dummy Byte Count	
	<b>ACK</b>
Byte 0	
	<b>ACK</b>
Byte 1	
	<b>ACK</b>
Byte 2	
	<b>ACK</b>
Byte 3	
	<b>ACK</b>
Byte 4	
	<b>ACK</b>
Byte 5	
	<b>ACK</b>
Byte 6	
	<b>ACK</b>
○	
○	○
○	○
	○
Byte 18	
	<b>ACK</b>
Byte 19	
	<b>ACK</b>
Byte 20	
	<b>ACK</b>
Stop Bit	

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends *Byte 0 through byte 8 (default)*
- ICS clock sends *Byte 0 through byte X (if X<sub>(H)</sub> was written to byte 8)*.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 <sub>(H)</sub>	
	<b>ACK</b>
	<b>Byte Count</b>
ACK	
	<b>Byte 0</b>
ACK	
	<b>Byte 1</b>
ACK	
	<b>Byte 2</b>
ACK	
	<b>Byte 3</b>
ACK	
	<b>Byte 4</b>
ACK	
	<b>Byte 5</b>
ACK	
	<b>Byte 6</b>
ACK	
If 7 <sub>H</sub> has been written to B6	<b>Byte 7</b>
ACK	
○	○
○	○
○	○
If 12 <sub>H</sub> has been written to B6	<b>Byte 18</b>
ACK	
If 13 <sub>H</sub> has been written to B6	<b>Byte 19</b>
ACK	
If 14 <sub>H</sub> has been written to B6	<b>Byte 20</b>
ACK	
Stop Bit	

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\*See notes on the following page.

0445B—08/01/03



## Brief I<sup>2</sup>C registers description for ICS94225 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I <sup>2</sup> C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-6	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	7	Byte 11 bit[7:4] is ICS vendor id - 1001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00 <sub>H</sub> to this byte.	08 <sub>H</sub>
Watchdog Timer Count Register	9	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10 <sub>H</sub>
Watchdog Control Registers	10 Bit [6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	10 Bit [7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
VCO Frequency Control Registers	11-12	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	13-14	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	15-16	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	17-20	These registers will control the output rise and fall time.	See individual byte description

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

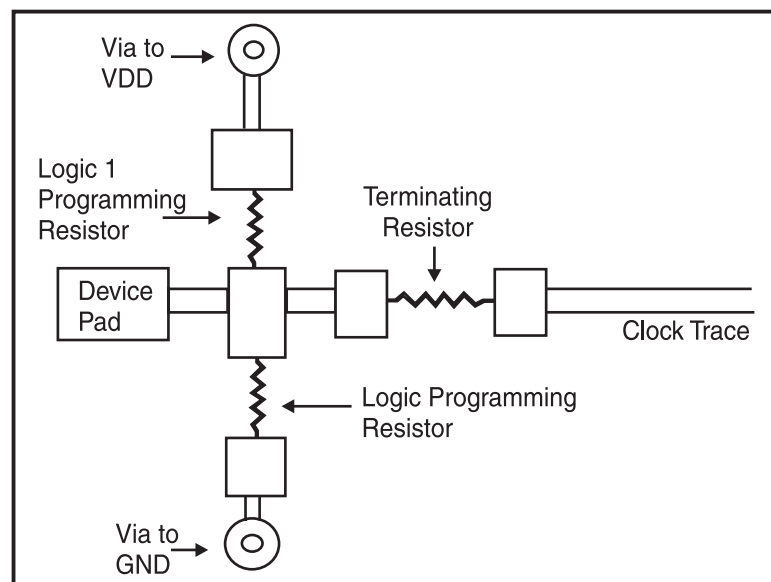


## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

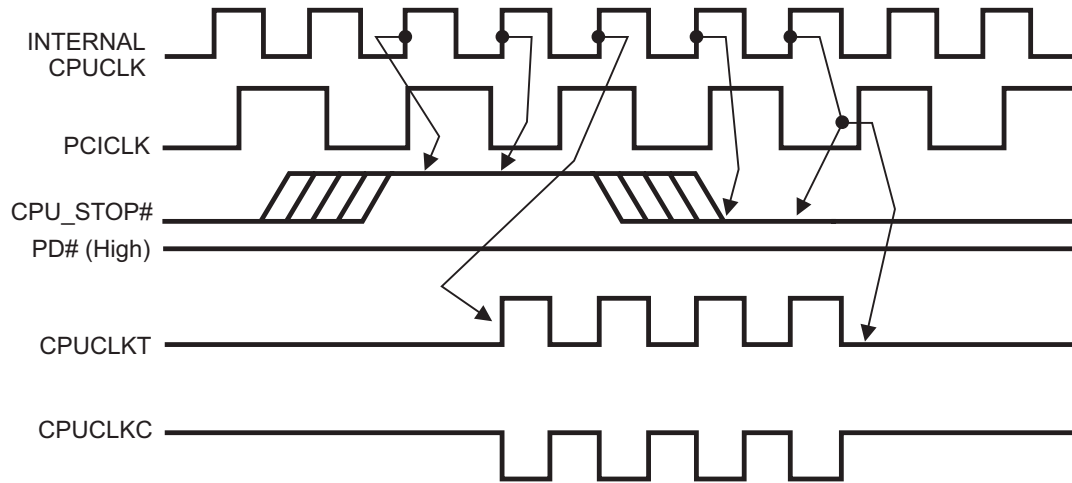


**Fig. 1**



### CPU\_STOP# Timing Diagram

CPU\_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU\_STOP# is synchronized by the **ICS94225**. All other clocks will continue to run while the CPUCLKs clocks are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



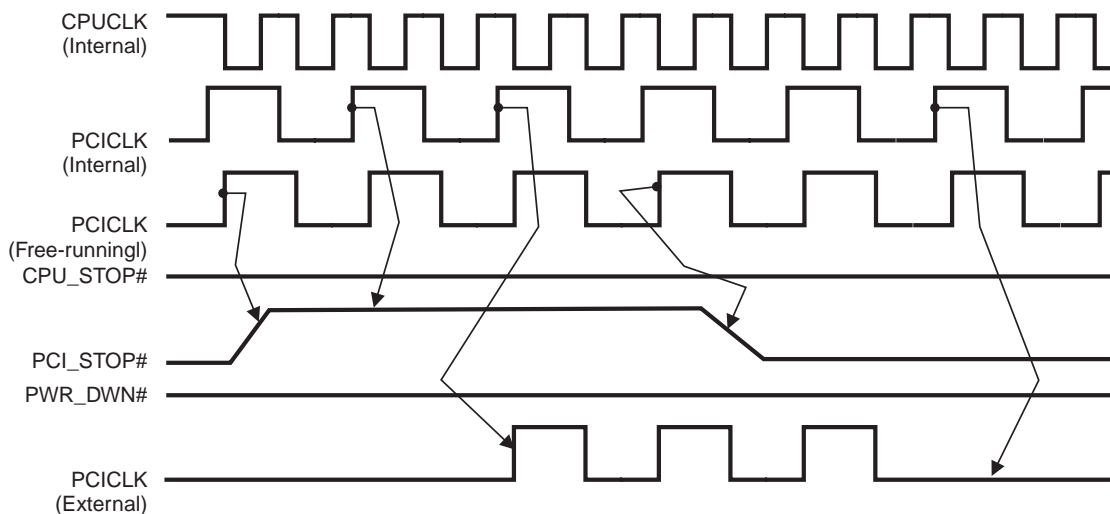
**Notes:**

- 1. All timing is referenced to the internal CPUCLK.
- 2. CPU\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS94225**.
- 3. All other clocks continue to run undisturbed.
- 4. PD# and PCI\_STOP# are shown in a high (true) state.



## PCI\_STOP# Timing Diagram

PCI\_STOP# is an asynchronous input to the **ICS94225**. It is used to turn off the PCICLK clocks for low power operation. PCI\_STOP# is synchronized by the **ICS94225** internally. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94225 device.)
2. PCI\_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS94225.
3. All other clocks continue to run undisturbed.
4. PD# and CPU\_STOP# are shown in a high (true) state.

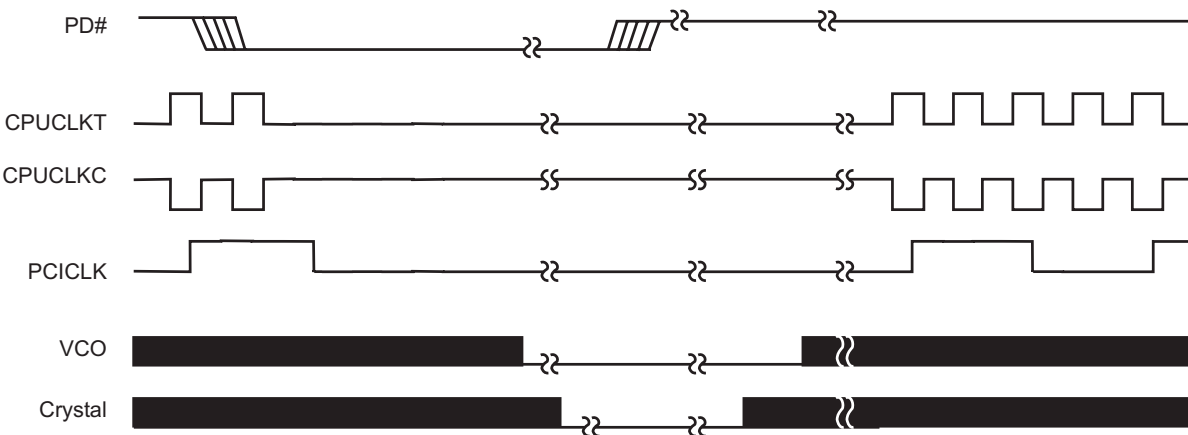




## PD# Timing Diagram

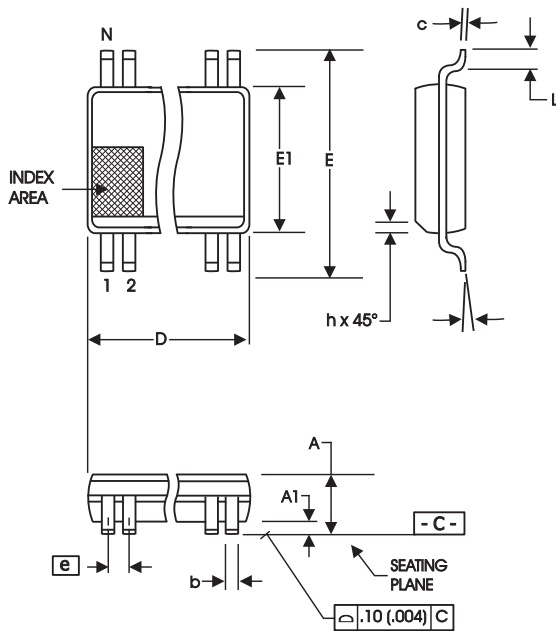
The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI\_STOP# and CPU\_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94225 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



**300 mil SSOP Package**

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
$\alpha$	0°	8°	0°	8°

N	VARIATIONS			
	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

**ICS94225yF-T**

Example:

**ICS XXXX y F - PPP - T**

- Designation for tape and reel packaging
- Pattern Number (2 or 3 digit number for parts with ROM code patterns)
- Package Type  
F=SSOP
- Revision Designator (will not correlate with datasheet revision)
- Device Type
- Prefix  
ICS, AV = Standard Device

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