Integrated Circuit Systems, Inc.

ICS94235

Programmable System Clock Chip for AMD - K7™ processor

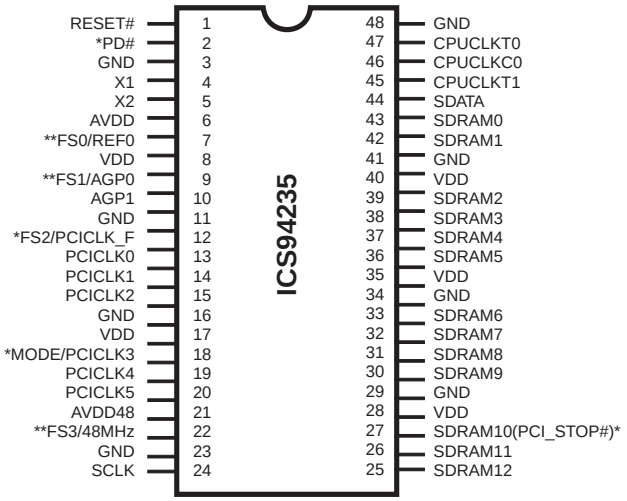
Recommended Application:
ALI 1647 style chipset

Output Features:
- 1 - Differential pair open drain CPU clocks
- 1 - Single-ended open drain CPU clock
- 13 - SDRAM @ 3.3V
- 7 - PCI @ 3.3V
- 2 - AGP @ 3.3V
- 1 - 48MHz, @3.3V
- 1 - REF @ 3.3V, (selectable strength) through I^2C

Features:
- Programmable ouput frequency
- Programmable ouput rise/fall time
- Programmable CPU, SDRAM, PCI and AGP skew
- Real time system reset output
- Spread spectrum for EMI control typically by 7dB to 8dB, with programmable spread percentage
- Watchdog timer technology to reset system if over-clocking causes malfunction
- Uses external 14.318MHz crystal

Skew Specifications:
- CPUT - CPUC: <250ps
- PCI - PCI: <500ps
- CPU - SDRAM: <350ps
- SDRAM - SDRAM: <250ps
- AGP - AGP: <250ps
- AGP - PCI: <750ps
- CPU - PCI: <3ns

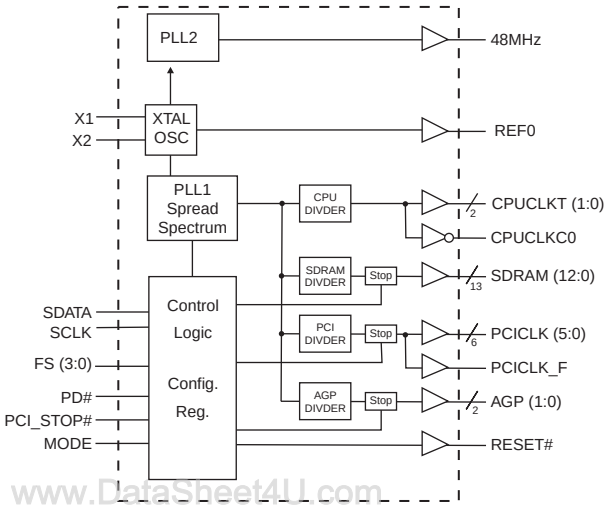
Pin Configuration



48-Pin 300mil SSOP &
240mil TSSOP package

Notes:
REF0 could be 1X or 2X strength controlled by I^2C.
* Internal Pull-up Resistor of 120K to VDD
** Internal pull-down of 120K to GND.

Block Diagram



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Functionality

FS3	FS2	FS1	FS0	CPU	SDRAM	PCI	AGP
0	0	0	0	66.66	66.66	33.33	66.66
0	0	0	1	66.66	100.00	33.33	66.66
0	0	1	0	100.00	66.66	33.33	66.66
0	0	1	1	100.00	100.00	33.33	66.66
0	1	0	0	100.00	133.33	33.33	66.66
0	1	0	1	120.00	120.00	30.00	60.00
0	1	1	0	133.33	100.00	33.33	66.66
0	1	1	1	133.33	133.33	33.33	66.66
1	0	0	0	90.00	90.00	30.00	60.00
1	0	0	1	100.90	100.90	33.63	67.27
1	0	1	0	100.00	66.66	33.33	66.66
1	0	1	1	100.00	100.00	33.33	66.66
1	1	0	0	100.00	133.33	33.33	66.66
0	1	0	1	126.00	126.00	31.50	63.00
1	1	1	0	133.33	100.00	33.33	66.66
1	1	1	1	133.33	133.33	33.33	66.66

Power Groups

AVDD = Xtal, Core PLL
AVDD48 = 48MHz, Fixed PLL

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	RESET#	OUT	Real time system reset signal for frequency value or watchdog timmer timeout. This signal is active low.
2	PD#[1]	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
4	X1	IN	Crystal input,nominally 14.318MHz.
5	X2	OUT	Crystal output, nominally 14.318MHz.
3, 11, 16, 23, 29, 34, 41, 48	GND	PWR	Ground pins
8, 17, 28, 35, 40	VDD	PWR	Power supply pins, nominal 3.3V
6	AVDD	PWR	Analog power supply pin, nominal 3.3V
7	FS0[2, 3]	IN	Frequency select pin.
	REF0	OUT	14.318 MHz reference clock.
9	FS1[2, 3]	IN	Frequency select pin.
	AGP0	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
10	AGP1	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
12	PCICLK_F	OUT	Free running PCICLK not stoped by PCI_STOP#
	FS2[1, 3]	IN	Frequency select pin.
20, 19, 15, 14, 13	PCICLK (5:4) (2:0)	OUT	PCI clock outputs.
18	PCICLK3	OUT	PCI clock output.
	MODE[1, 3]	IN	Function select pin, 1=Desktop Mode, 0=Mobile Mode.
21	AVDD48	PWR	Analog power supply pin, nominal 3.3V
22	FS3[2, 3]	IN	Frequency select pin.
	48MHz	OUT	48MHz output clock
24	SCLK	IN	Clock input of I^2C input, 5V tolerant input
27	PCI_STOP#[1]	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
	SDRAM10	OUT	SDRAM clock output.
25, 26, 30, 31, 32, 33, 36, 37, 38, 39, 42, 43	SDRAM (12:11, 9:0)	OUT	SDRAM clock outputs.
44	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
45, 47	CPUCLKT (1:0)	OUT	"True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
46	CPUCLKC0	OUT	"Complementory" clocks of differential pair CPU outputs. This open drain output need an external 1.5V pull-up.

Notes:
1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs
2: Internal pull-down resistor of 120K to GND.
3: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

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General Description

The **ICS94235** is a main clock synthesizer chip for AMD-K7 based systems with ALI 1647 style chipset. This provides all clocks required for such a system.

The **ICS94235** belongs to ICS new generation of programmable system clock generators. It employs serial programming I^2C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

Mode Pin - Power Management Input Control

MODE, Pin 18 (Latched Input)	Pin 27
0	PCI_STOP# (Input)
1	SDRAM10 (Output)

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General I²C serial interface information for the ICS94235

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte 0 through Byte 20*** (see Note)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2$_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 18	
	ACK
Byte 19	
	ACK
Byte 20	
	ACK
Stop Bit	

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*See notes on the following page.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends ***Byte 0 through byte 8 (default)***
- ICS clock sends ***Byte 0 through byte X (if X$_{(H)}$ was written to byte 8).***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3$_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7$_H$ has been written to B8	***Byte 7***
ACK	
○	○
○	○
○	○
If 12$_H$ has been written to B8	***Byte18***
ACK	
If 13$_H$ has been written to B8	***Byte 19***
ACK	
If 14$_H$ has been written to B8	***Byte 20***
ACK	
Stop Bit	

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Brief I²C registers description for ICS94235 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I²C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-6	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	7	Byte 11 bit[7:4] is ICS vendor id - 1001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00_H to this byte.	08_H
Watchdog Timer Count Register	9	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10_H
Watchdog Control Registers	10 Bit [6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	10 Bit [7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
VCO Frequency Control Registers	11-12	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	13-14	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	15-16	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	17-20	These registers will control the output rise and fall time.	See individual byte description

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

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Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description										PWD
		FS3	FS2	FS1	FS0	CPUCLK	SDRAM	PCICLK	AGP	Spread Precentage	
	Bit2	Bit7	Bit6	Bit5	Bit4	(MHz)	(MHz)	(MHz)	(MHz)		
Bit 2, Bit 7:4	0	0	0	0	0	66.66	66.66	33.33	66.66	+/- 0.25% Center Spread	00000 Note1
	0	0	0	0	1	66.66	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	0	1	0	100.00	66.66	33.33	66.66	+/- 0.25% Center Spread	
	0	0	0	1	1	100.00	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	0	0	100.00	133.33	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	0	1	120.00	120.00	30.00	60.00	+/- 0.25% Center Spread	
	0	0	1	1	0	133.33	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	1	1	133.33	133.33	33.33	66.66	+/- 0.25% Center Spread	
	0	1	0	0	0	90.00	90.00	30.00	60.00	+/- 0.25% Center Spread	
	0	1	0	0	1	100.90	100.90	33.63	67.27	+/- 0.25% Center Spread	
	0	1	0	1	0	100.00	66.66	33.33	66.66	0 to -0.5% Down Spread	
	0	1	0	1	1	100.00	100.00	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	0	0	100.00	133.33	33.33	66.66	0 to -0.5% Down Spread	
	0	0	1	0	1	126.00	126.00	31.50	63.00	+/- 0.25% Center Spread	
	0	1	1	1	0	133.33	100.00	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	1	1	133.33	133.33	33.33	66.66	0 to -0.5% Down Spread	
	1	0	0	0	0	102.00	102.00	34.00	67.99	+/- 0.25% Center Spread	
	1	0	0	0	1	102.00	136.00	34.00	67.99	+/- 0.25% Center Spread	
	1	0	0	1	0	136.00	102.00	34.00	67.99	+/- 0.25% Center Spread	
	1	0	0	1	1	136.00	136.00	34.00	67.99	+/- 0.25% Center Spread	
	1	0	1	0	0	103.00	103.00	34.33	68.66	+/- 0.25% Center Spread	
	1	0	1	0	1	103.00	137.33	34.33	68.66	+/- 0.25% Center Spread	
	1	0	1	1	0	137.33	103.00	34.33	68.66	+/- 0.25% Center Spread	
	1	0	1	1	1	137.33	137.33	34.33	68.66	+/- 0.25% Center Spread	
	1	1	0	0	0	105.00	105.00	35.00	69.99	+/- 0.25% Center Spread	
	1	1	0	0	1	105.00	140.00	35.00	69.99	+/- 0.25% Center Spread	
	1	1	0	1	0	140.00	140.00	35.00	69.99	+/- 0.25% Center Spread	
	1	1	0	1	1	107.00	107.00	35.66	71.33	+/- 0.25% Center Spread	
	1	1	1	0	0	107.00	142.66	35.66	71.33	+/- 0.25% Center Spread	
	1	1	1	0	1	133.90	133.90	33.40	66.95	+/- 0.25% Center Spread	
	1	1	1	1	0	110.00	110.00	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	1	1	146.66	146.66	36.66	73.33	+/- 0.25% Center Spread	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 7:4										0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled										0
Bit 0	0 - Running 1- Tristate all outputs										0

Note1: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.
The I^2C readback of the power up default indicates the revision ID in bits 2, 7:4 as shown.

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Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS3#
Bit 6	10	1	AGP1
Bit 5	9	1	AGP0
Bit 4	22	1	48MHz
Bit 3	43	1	SDRAM0
Bit 2	7	1	REF0 - 1X or 2X default = 1=1X
Bit 1	47, 46	1	CPUCLKT0, CPUCLKC0
Bit 0	45	1	CPUCLKT1

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	MODE#
Bit 6	20	1	PCICLK5
Bit 5	19	1	PCICLK4
Bit 4	18	1	PCICLK3
Bit 3	15	1	PCICLK2
Bit 2	14	1	PCICLK1
Bit 1	13	1	PCICLK0
Bit 0	12	1	PCICLK_F

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS0#
Bit 6	-	X	FS1#
Bit 5	-	X	FS2#
Bit 4	31	1	SDRAM8
Bit 3	30	1	SDRAM9
Bit 2	27	1	SDRAM10
Bit 1	26	1	SDRAM11
Bit 0	25	1	SDRAM12

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	1	Reserved
Bit 5	39	1	SDRAM2
Bit 4	38	1	SDRAM3
Bit 3	37	1	SDRAM4
Bit 2	36	1	SDRAM5
Bit 1	33	1	SDRAM6
Bit 0	32	1	SDRAM7

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	42	1	SDRAM1

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	1	Reserved (Note)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

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Byte 7: Vendor ID and Revision ID Register

Bit	PWD	Description
Bit 7	0	Vendor ID
Bit 6	0	Vendor ID
Bit 5	1	Vendor ID
Bit 4	X	Revision ID
Bit 3	X	Revision ID
Bit 2	X	Revision ID
Bit 1	X	Revision ID
Bit 0	X	Revision ID

Byte 8: Byte Count and Read Back Register

Bit	PWD	Description
Bit 7	0	Reserved
Bit 6	0	Reserved
Bit 5	0	Reserved
Bit 4	0	Reserved
Bit 3	1	Reserved
Bit 2	0	Reserved
Bit 1	0	Reserved
Bit 0	0	Reserved

Byte 9: Watchdog Timer Count Register

Bit	PWD	Description
Bit 7	0	The decimal representation of these 8 bits correspond to how many 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16X 290ms = 4.64 seconds.
Bit 6	0	
Bit 5	0	
Bit 4	1	
Bit 3	0	
Bit 2	0	
Bit 1	0	
Bit 0	0	

Byte 10: VCO Control Selection Bit & Watchdog Timer Control Register

Bit	PWD	Description
Bit 7	0	0=Hw/B0 freq / 1=B11 & 12 freq
Bit 6	0	WD Enable 0=disable / 1=enable
Bit 5	0	WD Status 0=normal / 1=alarm
Bit 4	1	WD Safe Frequency, Byte 0 bit 2
Bit 3	0	WD Safe Frequency, FS3
Bit 2	0	WD Safe Frequency, FS2
Bit 1	0	WD Safe Frequency, FS1
Bit 0	0	WD Safe Frequency, FS0

Note: FS values in bit (0:4) will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

Byte 11: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit0
Bit 6	X	REF Divider Bit6
Bit 5	X	REF Divider Bit5
Bit 4	X	REF Divider Bit4
Bit 3	X	REF Divider Bit3
Bit 2	X	REF Divider Bit2
Bit 1	X	REF Divider Bit1
Bit 0	X	REF Divider Bit0

Note: The decimal representation of these 7 bits (Byte 11 (6:0)) + 2 is equal to the REF divider value .

Notes:

1. PWD = Power on Default

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Byte 12: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit8
Bit 6	X	VCO Divider Bit7
Bit 5	X	VCO Divider Bit6
Bit 4	X	VCO Divider Bit5
Bit 3	X	VCO Divider Bit4
Bit 2	X	VCO Divider Bit3
Bit 1	X	VCO Divider Bit2
Bit 0	X	VCO Divider Bit1

Note: The decimal representation of these 9 bits (Byte 12 bit (7:0) & Byte 11 bit (7)) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program 36 - 8 = 28, namely, 0, 00011100 into byte 12 bit & byte 11 bit 7.

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Byte 13: Spread Spectrum Control Register

Bit	PWD	Description
Bit 7	X	Spread Spectrum Bit7
Bit 6	X	Spread Spectrum Bit6
Bit 5	X	Spread Spectrum Bit5
Bit 4	X	Spread Spectrum Bit4
Bit 3	X	Spread Spectrum Bit3
Bit 2	X	Spread Spectrum Bit2
Bit 1	X	Spread Spectrum Bit1
Bit 0	X	Spread Spectrum Bit0

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 14: Spread Spectrum Control Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Spread Spectrum Bit12
Bit 3	X	Spread Spectrum Bit11
Bit 2	X	Spread Spectrum Bit10
Bit 1	X	Spread Spectrum Bi 9
Bit 0	X	Spread Spectrum Bit8

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 15: Output Skew Control

Bit	PWD	Description
Bit 7	0	CPUCLKT/C0 Skew Control
Bit 6	0	
Bit 5	0	CPUCLKT1
Bit 4	0	
Bit 3	0	SDRAM0 Skew Control
Bit 2	0	
Bit 1	0	SDRAM (12:1) Skew Control
Bit 0	0	

Byte 16: Output Skew Control

Bit	PWD	Description
Bit 7	0	PCICLK (5:0, F) Skew Control
Bit 6	1	
Bit 5	0	
Bit 4	0	
Bit 3	0	AGP (1:0) Skew Control
Bit 2	1	
Bit 1	0	
Bit 0	0	

Byte 17: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	CPUCLKT/C0 Slew Rate Control
Bit 6	0	
Bit 5	1	CPUCLKT1 Slew Rate Control
Bit 4	0	
Bit 3	1	PCICLK_F Slew Rate Control
Bit 2	0	
Bit 1	1	PCICLK (5:0) Slew Rate Control
Bit 0	0	

Byte 18: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	SDRAM0 Skew Control
Bit 6	0	
Bit 5	1	SDRAM (12:1) Skew Control
Bit 4	0	
Bit 3	1	AGP (1:0) Slew Rate Control
Bit 2	0	
Bit 1	1	48MHz Slew Rate Control
Bit 0	0	

Notes:

1. PWD = Power on Default
2. The power on default for byte 13-20 depends on the harware (latch inputs FS(4:0)) or I^2C (Byte 0 bit (1:7)) setting. Be sure to read back and re-write the values of these 8 registers when VCO frequency change is desired for the first pass.
3. If Byte 8 bit 7 is driven to "1" meaning programming is intended, Byte 21-24 will lose their default power up value.

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Byte 19: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Byte 20: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Note: Byte 19 and 20 are reserved registers, these are unused registers writing to these registers will not affect device performance or functinality.

VCO Programming Constrains

VCO Frequency ..... 150MHz to 500MHz

VCO Divider Range ..... 8 to 519

REF Divider Range ..... 2 to 129

Phase Detector Stability ..... 0.3536 to 1.4142

Useful Formula

VCO Frequency = 14.31818 x VCO/REF divider value

Phase Detector Stabiliy = 14.038 x (VCO divider value)$^{-0.5}$

To program the VCO frequency for over-clocking.

0. Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.

1. Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.

2. Write 0001, 1001 (19_H) to byte 8 for readback of 21 bytes (byte 0-20).

3. Read back byte 11-20 and copy values in these registers.

4. Re-initialize the write sequence.

5. Write a '1' to byte 9 bit 7 and write to byte 11 & 12 with the desired VCO & REF divider values.

6. Write to byte 13 to 20 with the values you copy from step 3. This maintains the output spread, skew and slew rate.

7. The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 11 and 12 unless the system is to reboot.

Note:

1. User needs to ensure step 3 & 7 is carried out. Systems with wrong spread percentage and/or group to group skew relation programmed into bytes 13-16 could be unstable. Step 3 & 7 assure the correct spread and skew relationship.

2. If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.

3. Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use 14.31818MHz x VCO/REF divider values to calculate the VCO frequency (MHz).

4. ICS recommends users, to utilize the software utility provided by ICS Application Engineering to program the VCO frequency.

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5. Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spreadamount desired. See Application note for software support.

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Absolute Maximum Ratings

Supply Voltage 5.5V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Ouput Parameters.

TA = 0 - 70º C; Supply Voltage VDD = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		VDD+0.3	V
Input Low Voltage	V_{IL}		VSS-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = VDD			5	uA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA
Operating	$IDD3.3_{OP66}$	CL = 0 pF; Select @ 66MHz				
Supply Current	$IDD3.3_{OP100}$	C_L = 0 pF; Select @ 66MHz			180	mA
	$IDD3.3_{OP133}$	C_L = 0 pF; Select @ 133MHz				
Power Down	P_D				600	uA
Input frequency	Fi	VDD = 3.3 V;	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From VDD = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$t_{AGP-PCI}$	V_T = 50%		300	750	ps
	$t_{CPU-SDRAM}$			200	350	
	$t_{CPU-PCI}$			2.67	3	ns

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - CPUCLK (Open Drain)

TA = 0 - 70º C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O	$V_O = V_X$				Ohms
Output High Voltage	V_{OH2B}	Termination to $V_{pull\text{-}up(external)}$	1		1.2	V
Output Low Voltage	V_{OL2B}	Termination to $V_{pull\text{-}up(external)}$			0.4	V
Output Low Current	I_{OL2B}	VOL = 0.3V	18			mA
Rise Time[1]	tr_{2B}	VOL = 0.3V, V_{OH} = 1.2 V			0.9	ns
Fall Time[1]	tf_{2B}	VOH = 1.2 V, V_{OL} = 0.3 V		**0.913**	0.9	ns
					$V_{pullup(external)}$	
Differential Voltage-$_{AC1}$	V_{DIF}	Note 2	0.4		0.6	V
					$V_{pullup(external)}$	
Differential Voltage-$_{DC1}$	V_{DIF}	Note 2	0.2		0.6	V
Differential Crossover Voltage[1]	V_X	Note 3	550		1100	mV
Duty Cycle[1]	dt_{2B}	V_T = 50%	45	53	55	%
Skew[1]	tsk_{2B}	V_T = 50%			250	ps
Jitter, Cycle-to-cycle[1]	$tjcyc\text{-}cyc_{2B}$	$V_T = V_X$		201	250	ps
Jitter, Absolute[1]	$tjabs_{2B}$	V_T = 50%	-250		250	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - VDIF specifies the minimum input differential voltages (VTR-VCP) required for switching, where VTR is the TRUE input level and VCP is the "complement" input level.

3 - Vpullup(external) = 1.5V, Min = Vpullup(external)/2-150mV; Max = (Vpullup(external)/2)+150mV.

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Electrical Characteristics - PCICLK

TA = 0 - 70º C VDD = 3.3V +/-5%; C = 30pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-16	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	19			mA
Rise Time$_1$	tr_1	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.63	2	ns
Fall Time$_1$	tf_1	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.63	2	ns
Duty Cycle$_1$	dt_1	V_T = 1.5V	45	51.9	55	%
Skew$_1$	Tsk_1	V_T = 1.5V		170	500	ps

$_1$Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK_F

TA = 0 - 70º C; VDD = 3.3V +/-5%; CL = 20 pF (unless otherwise stated).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-12	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	12			mA
Rise Time$_1$	tr_1	V_{OL} = 0.4 V, V_{OH} =2.4 V		1.63	2	ns
Fall Time$_1$	tf_1	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.63	2	ns
Duty Cycle$_1$	dt_1	V_T = 50%	45	49.7	55	%
Skew$_1$(window)	T_{sk1}	V_T = 50%		170	500	ps

$_1$Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - 48MHz, REF0

TA = 0 - 70º C; VDD = 3.3V +/-5%, VDDL = 2.5 V +/-5%; CL = 20pF (otherwise stated).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time$_1$	tr_5	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.23	2	ns
Fall Time$_1$	tf_5	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.21	2	ns
Duty Cycle$_1$	dt_5	V_T = 1.5 V	45	53	55	%
Jitter, One Sigma$_1$	$tj1s_5$	V_T = 1.5 V		595	0.5	ns
Jitter, Absolute$_1$	$tjabs_5$	V_T = 1.5 V	-1		1	ns

$_1$Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM (12:0)

TA = 0 - 70º C; VDD = 3.3 V +/-5%, CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -11 mA	2			V
Output Low Voltage	V_{OL3}	I_{OL} = 11 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V			-12	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	12			mA
Rise Time$_1$	Tr_3	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.88	2.2	ns
Fall Time$_1$	Tf_3	V_{OH} = 2.4 V, V_{OL} = 0.4 V		0.8	2.2	ns
Duty Cycle$_1$	Dt_3	V_T = 50%	45	51.2	55	%
Skew$_1$(window)	Tsk_1	V_T = 50%		205	250	ps

$_1$Guarenteed by design, not 100% tested in production.

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Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

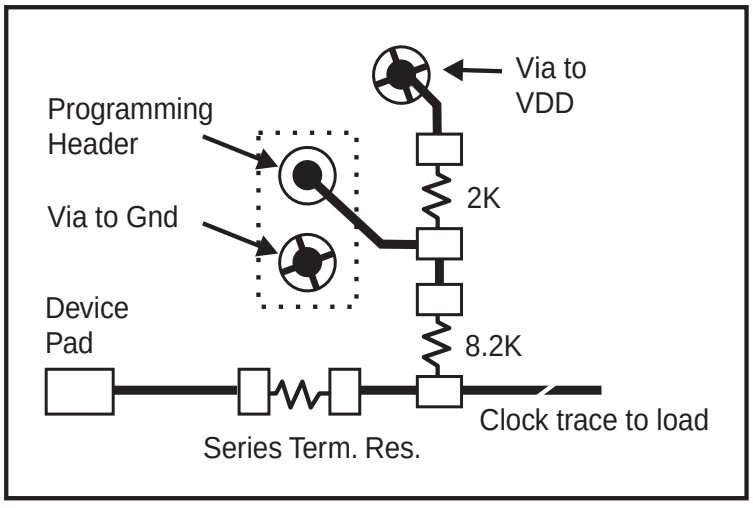

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Fig. 1

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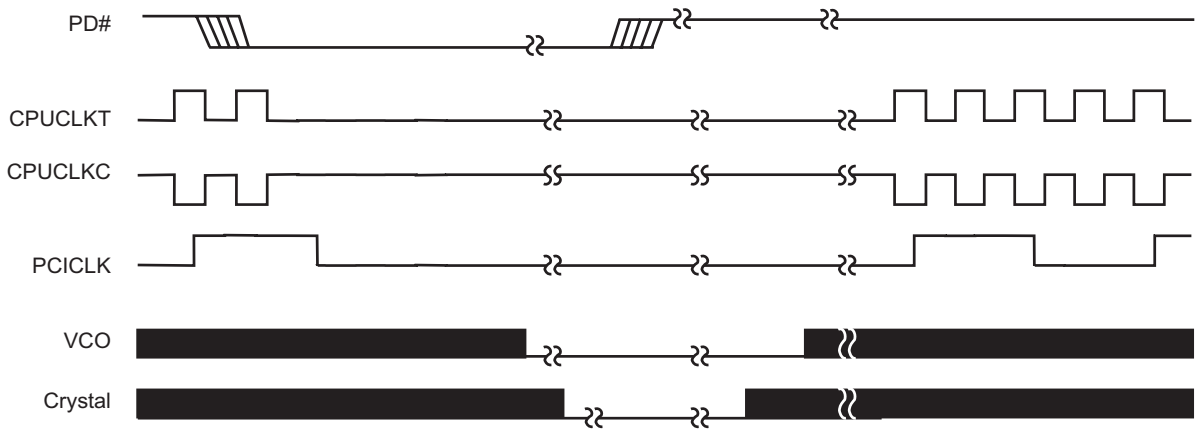
PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. CPU_STOP# is considered to be a don't care during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94235 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

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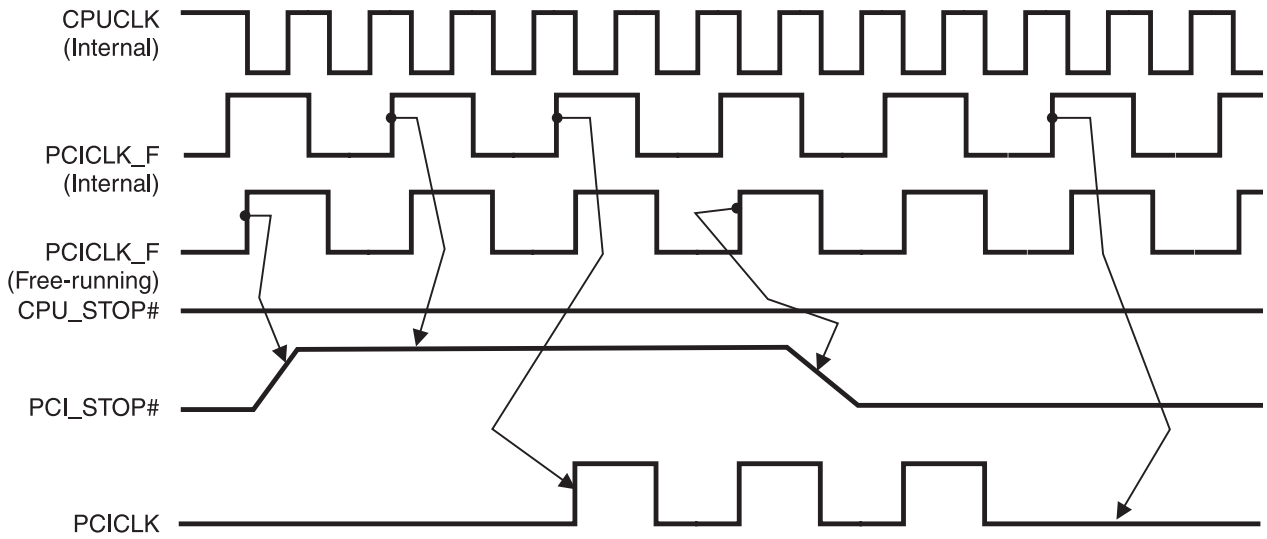
PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS94235**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS94235** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94235 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS94235.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

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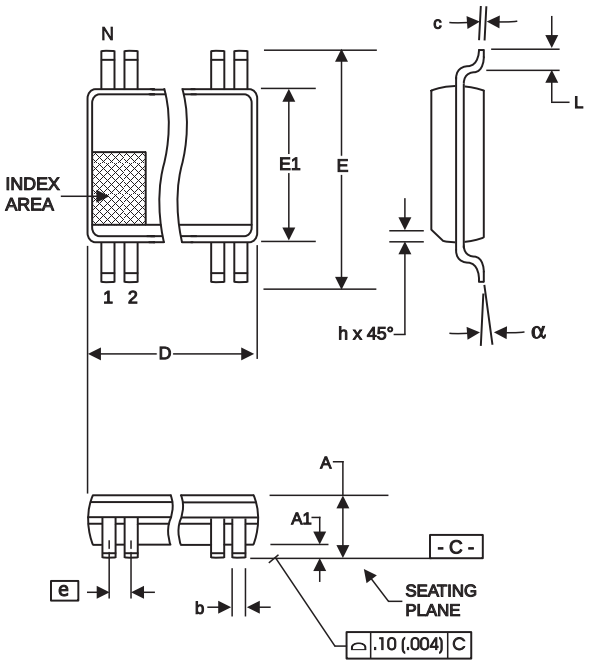

300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.748	16.002	.620	.630

JEDEC MO-118 6/1/00
DOC# 10-0034 REV B

Ordering Information

ICS94235yFT

Example:

ICS XXXX y F - T

Designation for tape and reel packaging

Package Type
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device

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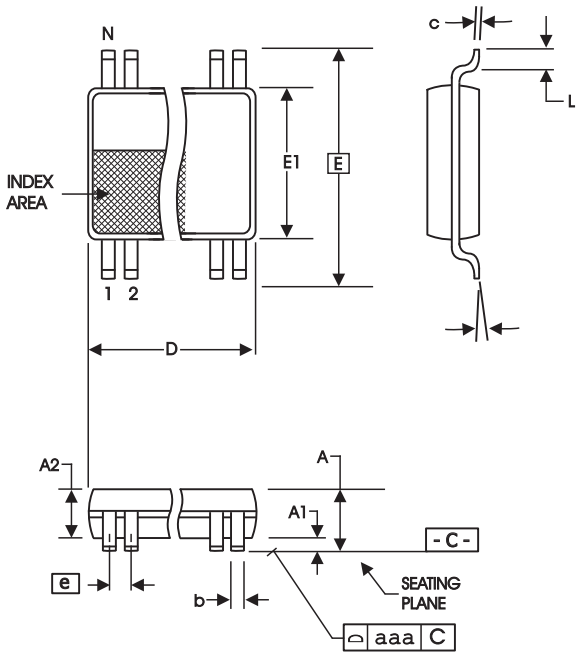

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.30
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

MO-153 JEDEC 7/6/00 Rev B
Doc.# 10-0039

Ordering Information

ICS94235yGT

Example:

ICS XXXX y G - T

Designation for tape and reel packaging

Package Type
G=TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device

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