Programmable Timing Control Hub™ for PII/III™

Recommended Application:

810/810E/815 and 815 B-Step type chipset

Output Features:

- 2 - CPUs @ 2.5V
- 13 - SDRAM @ 3.3V
- 3 - 3V66 @ 3.3V
- 8 - PCI @3.3V
- 1 - 24/48MHz@ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 1 - REF @3.3V, 14.318MHz

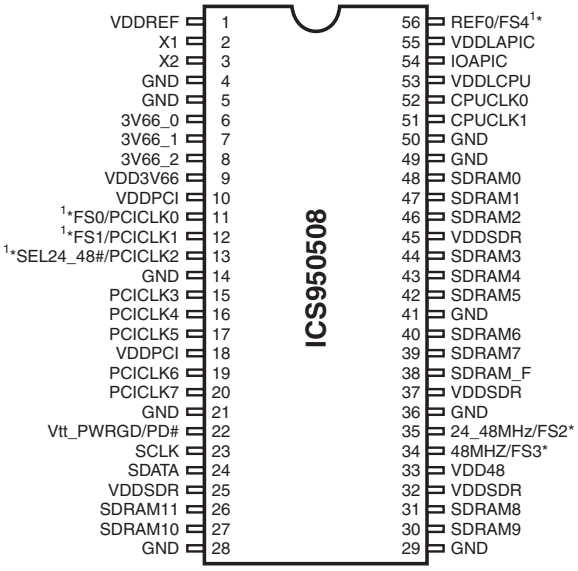
Features/Benefits:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

Key Specifications:

- CPU Output Jitter: <250ps
- IOAPIC Output Jitter: <500ps
- 48MHz, 3V66, PCI Output Jitter: <500ps
- Ref Output Jitter. <1000ps
- CPU Output Skew: <175ps
- PCI Output Skew: <500ps
- 3V66 Output Skew <175ps
- For group skew timing, please refer to the Group Timing Relationship Table.

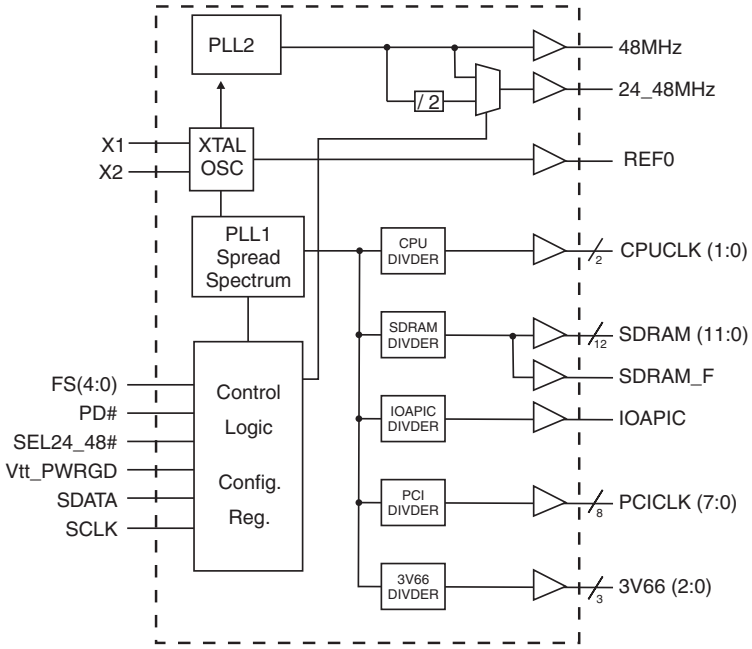
Pin Configuration



56-Pin 300-mil SSOP

1. These pins will have 1.5 to 2X drive strength.
* Internal Pull-up resistor of 120K to VDD

Block Diagram



General Description

The **ICS950508** is a single chip clock solution for desktop designs using the 810/810E, 815 and 815 B-Step style chipset. It provides all necessary clock signals for such a system.

The **ICS950508** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment. With all these programmable features ICS's, TCH makes mother board testing, tuning and improvement very simple.

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 9, 10, 18, 25, 32, 33, 37, 45	VDD	PWR	3.3V power supply
2	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
3	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
4, 5, 14, 21, 28, 29, 36, 41, 49	GND	PWR	Ground pins for 3.3V supply
8, 7, 6	3V66 (2:0)	OUT	3.3V Fixed 66MHz clock outputs for HUB
11	PCICLK0[1]	OUT	3.3V PCI clock output, with Synchronous CPUCLKs
	FS0	IN	Logic input frequency select bit. Input latched at power on.
12	PCICLK1[1]	OUT	3.3V PCI clock output, with Synchronous CPUCLKs
	FS1	IN	Logic input frequency select bit. Input latched at power on.
13	SEL_24_48#	IN	Logic input to select output.
	PCICLK2[1]	OUT	3.3V PCI clock output, with Synchronous CPUCLKs
20, 19, 17, 16, 15	PCICLK (7:3)	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKs
22	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
	Vtt_PWRGD	IN	This pin acts as a dual function input pin for Vtt_PWRGD and PD# signal. When Vtt_PWRGD goes high the frequency select will be latched at power on; thereafter the pin is an asynchronous active low power down pin.
23	SCLK	IN	Clock pin for I^2C circuitry 5V tolerant
24	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
34	FS3	IN	Logic input frequency select bit. Input latched at power on.
	48MHz	OUT	3.3V Fixed 48MHz clock output for USB
35	FS2	IN	Logic input frequency select bit. Input latched at power on.
	24_48MHz	OUT	3.3V 24_48MHz output, selectable through pin 13, default is 24MHz.
38	SDRAM_F	OUT	3.3V SDRAM output can be turned off through I^2C
48, 46, 47, 44, 43, 42, 40, 39, 31, 30, 27, 26	SDRAM (11:0)	OUT	3.3V output. All SDRAM outputs can be turned off through I^2C
50	GNDL	PWR	Ground for 2.5V power supply for CPU & APIC
51, 52	CPUCLK (1:0)	OUT	2.5V Host bus clock output. Output frequency derived from FS pins.
53, 55	VDDL	PWR	2.5V power suypply for CPU, IOAPIC
54	IOAPIC	OUT	2.5V clock outputs running at 16.67MHz.
56	FS4	IN	Logic input frequency select bit. Input latched at power on.
	REF0[1]	OUT	3.3V, 14.318MHz reference clock output.

General I²C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
○		
○		○
○		○
		○
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address D3(H)		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
	X Byte	Beginning Byte N
ACK		
		○
○		○
○		○
○		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

*See notes on the following page.

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Byte 0: Functionality and frequency select register (Default=0)

Bit	Description										PWD
Bit (2,7:4)	Bit2	Bit7	Bit6	Bit5	Bit4	CPUCLK MHz	SDRAM MHz	3V66 MHz	PCICLK MHz	IOAPIC MHz	Note 1
	FS4	FS3	FS2	FS1	FS0						
	0	0	0	0	0	66.43	99.65	66.43	33.21	16.61	
	0	0	0	0	1	60.00	90.00	60.00	30.00	15.00	
	0	0	0	1	0	66.80	100.20	66.80	33.40	16.70	
	0	0	0	1	1	68.33	102.50	68.33	34.17	17.08	
	0	0	1	0	0	70.00	105.00	70.00	35.00	17.50	
	0	0	1	0	1	75.00	112.50	75.00	37.50	18.75	
	0	0	1	1	0	80.00	120.00	80.00	40.00	20.00	
	0	0	1	1	1	83.00	124.50	83.00	41.50	20.75	
	0	1	0	0	0	99.65	99.65	66.43	33.21	16.61	
	0	1	0	0	1	90.00	90.00	60.00	30.00	15.00	
	0	1	0	1	0	100.23	100.23	66.84	33.41	16.70	
	0	1	0	1	1	103.00	103.00	68.67	34.33	17.17	
	0	1	1	0	0	105.00	105.00	70.00	35.00	17.50	
	0	1	1	0	1	110.00	110.00	73.33	36.67	18.33	
	0	1	1	1	0	115.00	115.00	76.67	38.33	19.17	
	0	1	1	1	1	200.00	200.00	133.33	66.66	33.33	
	1	0	0	0	0	132.86	132.86	66.43	33.21	16.61	
	1	0	0	0	1	166.67	166.67	83.34	41.67	20.83	
	1	0	0	1	0	133.64	133.64	66.82	33.41	16.70	
	1	0	0	1	1	137.00	137.00	68.50	34.25	17.13	
	1	0	1	0	0	140.00	140.00	70.00	35.00	17.50	
	1	0	1	0	1	145.00	145.00	72.50	36.25	18.13	
	1	0	1	1	0	150.00	150.00	75.00	37.50	18.75	
	1	0	1	1	1	160.00	160.00	80.00	40.00	20.00	
	1	1	0	0	0	132.86	99.65	66.93	33.21	16.61	
	1	1	0	0	1	166.67	125.00	83.34	41.67	20.83	
	1	1	0	1	0	133.64	100.23	66.82	33.41	16.7	
	1	1	0	1	1	137.00	102.75	68.50	34.25	17.13	
	1	1	1	0	0	140.00	105.00	70.00	35.00	17.50	
	1	1	1	0	1	145.00	108.75	72.50	36.25	18.13	
	1	1	1	1	0	150.00	112.50	75.00	37.50	18.75	
	1	1	1	1	1	160.00	120.00	80.00	40.00	20.00	
Bit 3	0-Frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,7:4										0
Bit 1	0- Normal 1- Spread spectrum enable ± 0.35% Center Spread										1
Bit 0	0- Running 1- Tristate all outputs										0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Byte 1: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	X	Readback FS3#
Bit 6	-	X	Readback FS0#
Bit 5	-	X	Readback FS2#
Bit 4	35	1	24MHz
Bit 3	-	1	(Reserved)
Bit 2	34	1	48MHz
Bit 1	-	1	(Reserved)
Bit 0	38	1	SDRAM_F

Byte 2: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	39	1	SDRAM7
Bit 6	40	1	SDRAM6
Bit 5	42	1	SDRAM5
Bit 4	43	1	SDRAM4
Bit 3	44	1	SDRAM3
Bit 2	46	1	SDRAM2
Bit 1	47	1	SDRAM1
Bit 0	48	1	SDRAM0

Byte 3: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	20	1	PCICLK7
Bit 6	19	1	PCICLK6
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	15	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	12	1	PCICLK1
Bit 0	11	1	PCICLK0

Byte 4: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	8	1	3V66_2
Bit 6	6	1	3V66_0
Bit 5	7	1	3V66_1
Bit 4	-	X	Readback FS4#
Bit 3	54	1	IOAPIC
Bit 2	-	X	Readback FS1#
Bit 1	51	1	CPUCLK1
Bit 0	52	1	CPUCLK0

Byte 5: Output Control Register

Bit	Pin#	PWD	Description
Bit 7	-	X	Readback (SEL24, 48#)#
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	0	(Reserved)
Bit 3	26	1	SDRAM11
Bit 2	27	1	SDRAM10
Bit 1	30	1	SDRAM9
Bit 0	31	1	SDRAM8

Byte 6: Vendor ID Register

Bit	Name	PWD	Description
Bit 7	-	X	(Reserved)
Bit 6	-	X	(Reserved)
Bit 5	-	X	(Reserved)
Bit 4	-	X	(Reserved)
Bit 3	-	X	(Reserved)
Bit 2	Vendor ID2	0	ICS vendor ID is 001 as in number 1 in frequency timing generation.
Bit 1	Vendor ID1	0	
Bit 0	Vendor ID0	1	

Byte 7: Revision ID and Device ID Register

Bit	Name	PWD	Description
Bit 7	Revision ID2	0	Device ID and Revision ID values will be based on individual device and it's revisio, "01h" in this case.
Bit 6	Revision ID1	0	
Bit 5	Revision ID0	0	
Bit 4	Device ID4	0	
Bit 3	Device ID3	0	
Bit 2	Device ID2	0	
Bit 1	Device ID1	0	
Bit 0	Device ID0	1	

Byte 8: Byte Count Read Back Register

Bit	Name	PWD	Description
Bit 7	Byte7	0	Note: Writing to this register will configure byte count and how many bytes will be read back, default is $0F_H$ = 15 bytes.
Bit 6	Byte6	0	
Bit 5	Byte5	0	
Bit 4	Byte4	0	
Bit 3	Byte3	1	
Bit 2	Byte2	0	
Bit 1	Byte1	0	
Bit 0	Byte0	0	

Byte 9: Watchdog Timer Count Register

Bit	Name	PWD	Description
Bit 7	WD7	0	The decimal representation of these 8 bits correspond to X • 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16 • 290ms = 4.6 seconds.
Bit 6	WD6	0	
Bit 5	WD5	0	
Bit 4	WD4	1	
Bit 3	WD3	0	
Bit 2	WD2	0	
Bit 1	WD1	0	
Bit 0	WD0	0	

Byte 10: Programming Enable bit 8 Watchdog Control Register

Bit	Name	PWD	Description
Bit 7	Program Enable	0	Programming Enable bit 0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all I^2C programing.
Bit 6	WD Enable	0	Watchdog Enable bit
Bit 5	WD Alarm	0	Watchdog Alarm Status 0 = normal 1= alarm status
Bit 4	SF4	0	Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corrsponding to Byte 0 Bit 2, 7:4 table
Bit 3	SF3	0	
Bit 2	SF2	0	
Bit 1	SF1	0	
Bit 0	SF0	0	

Byte 11: VCO Frequency M Divider (Reference divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 8	X	N divider bit 8
Bit 6	Mdiv 6	X	The decimal respresentation of Mdiv (6:0) corresposd to the reference divider value. Default at power up is equal to the latched inputs selection.
Bit 5	Mdiv 5	X	
Bit 4	Mdiv 4	X	
Bit 3	Mdiv 3	X	
Bit 2	Mdiv 2	X	
Bit 1	Mdiv 1	X	
Bit 0	Mdiv 0	X	

Byte 12: VCO Frequency N Divider (VCO divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 7	X	The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selecton. Notice Ndiv 8 is located in Byte 11.
Bit 6	Ndiv 6	X	
Bit 5	Ndiv 5	X	
Bit 4	Ndiv 4	X	
Bit 3	Ndiv 3	X	
Bit 2	Ndiv 2	X	
Bit 1	Ndiv 1	X	
Bit 0	Ndiv 0	X	

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Byte 13: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	SS 7	X	The Spread Spectrum (12:0) bit will program the spread precentage. Spread precent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use the ICS spread programming guide for spread programming. Default power on is latched FS divider.
Bit 6	SS 6	X	
Bit 5	SS 5	X	
Bit 4	SS 4	X	
Bit 3	SS 3	X	
Bit 2	SS 2	X	
Bit 1	SS 1	X	
Bit 0	SS 0	X	

Byte 14: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	Reserved
Bit 5	Reserved	X	Reserved
Bit 4	SS 12	X	Spread Spectrum Bit 12
Bit 3	SS 11	X	Spread Spectrum Bit 11
Bit 2	SS 10	X	Spread Spectrum Bit 10
Bit 1	SS 9	X	Spread Spectrum Bit 9
Bit 0	SS 8	X	Spread Spectrum Bit 8

Byte 15: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	SD Div 3	X	SDRAM clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	SD Div 2	X	
Bit 5	SD Div 1	X	
Bit 4	SD Div 0	X	
Bit 3	CPU Div 3	X	CPU clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	CPU Div 2	X	
Bit 1	CPU Div 1	X	
Bit 0	CPU Div 0	X	

Byte 16: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	PCI Div 3	X	PCI clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 2. Default at power up is latched FS divider.
Bit 6	PCI Div 2	X	
Bit 5	PCI Div 1	X	
Bit 4	PCI Div 0	X	
Bit 3	AGP Div 3	X	AGP clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	AGP Div 2	X	
Bit 1	AGP Div 1	X	
Bit 0	AGP Div 0	X	

Byte 17: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	PCI_INV	X	PCICLK Phase Inversion bit
Bit 6	3V66_INV	X	3V66 Phase Inversion bit
Bit 5	SD_INV	X	SDRAM Phase Inversion bit
Bit 4	CPU_INV	X	CPUCLK Phase Inversion bit
Bit 3	APIC Div 3	X	IOAPIC clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to table 2. Default at power up is latched FS divider.
Bit 2	APIC Div 2	X	
Bit 1	APIC Div 1	X	
Bit 0	APIC Div 0	X	

Table 1

Div (3:2) / Div (1:0)	00	01	10	11
00	/2	/4	/8	/16
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

Table 2

Div (3:2) / Div (1:0)	00	01	10	11
00	/4	/8	/16	/32
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/9	/18	/36	/72

Byte 18: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	SD_Skew 0	1	These 2 bits delay the SDRAM with respect to CPUCLK 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps
Bit 6	SD_Skew 1	0	
Bit 5	Reserved	0	Reserved
Bit 4	Reserved	0	Reserved
Bit 3	CPU_Skew 1	1	These 2 bits delay the CPU clock with respect to all other clocks. 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps
Bit 2	CPU_Skew 0	0	
Bit 1	Reserved	0	Reserved
Bit 0	Reserved	0	Reserved

Byte 19: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	PCI_Skew 3	0	These 4 bits can change the 3V66 to PCI skew from 1.4ns - 2.9ns. Each binary increment or decrement of PCI_SKEW (3:0) will increase or decrease the delay of the PCI clocks by 100ps.
Bit 6	PCI_Skew 2	0	
Bit 5	PCI_Skew 1	1	
Bit 4	PCI_Skew 0	0	
Bit 3	3V66_Skew 1	1	These 2 bits delay the 3V66 with respect to CPUCLK 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps
Bit 2	3V66_Skew 0	0	
Bit 1	Reserved	0	Reserved
Bit 0	Reserved	0	Reserved

Byte 20: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	0	Reserved
Bit 6	Reserved	0	Reserved
Bit 5	Reserved	0	Reserved
Bit 4	Reserved	0	Reserved
Bit 3	APIC_Skew 3	0	These 4 bits can change the 3V66 to APIC skew from 1.4ns - 2.9ns. Default at power up is - 2.5ns. Each binary increment or decrement of APIC_SKEW (3:0) will increase or decrease the delay of the PCI clocks by 100ps.
Bit 2	APIC_Skew 2	0	
Bit 1	APIC_Skew 1	1	
Bit 0	APIC_Skew 0	0	

Byte 21: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	24/48_Slew 1	0	24/48 MHz clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 6	24/48_Slew 0	1	
Bit 5	3V66_Slew 1	0	3V66 clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 4	3V66_Slew 0	1	
Bit 3	APIC_Slew 1	0	IOAPIC clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 2	APIC_Slew 0	1	
Bit 1	REF_Slew 1	0	REF clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 0	REF_Slew 0	1	

Byte 22: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	SD_F Slew 1	0	SDRAM_F clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 6	SD_F Slew 0	1	
Bit 5	SD(11:8) Slew 1	0	SDRAM (11:8) clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 4	SD(11:8) Slew 0	1	
Bit 3	SD(7:4) Slew 1	0	SDRAM (7:4) clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 2	SD(7:4) Slew 0	1	
Bit 1	SD(3:0) Slew 1	0	SDRAM (3:0) clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 0	SD(3:0) Slew 0	1	

Byte 23: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	PCI (7:4) Slew 1	0	PCI (7:4) clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 6	PCI (7:4) Slew 0	1	
Bit 5	PCI (3:0) Slew 1	0	PCI (3:0) clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 4	PCI (3:0) Slew 0	1	
Bit 3	CPU 1 Slew 1	0	CPUCLK 1 clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 2	CPU 1 Slew 0	1	
Bit 1	CPU 0 Slew 1	0	CPUCLK 0 clock slew rate control bits. 10 = strong: 11 = normal; 01 = weak
Bit 0	CPU 0 Slew 0	1	

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Timing Relationship Table[1]

Group	CPU 66MHz SDRAM 100MHz		CPU 100MHz SDRAM 100MHz		CPU 133MHz SDRAM 100MHz		CPU 133MHz SDRAM 133MHz	
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM	2.5ns	500ps	5.0ns	500ps	0.0ns	500ps	3.75ns	500ps
CPU to 3V66	7.5ns	500ps	5.0ns	500ps	0.0ns	500ps	0.0ns	500ps
SDRAM to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps	3.75ns	500ps
3V66 to PCI	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5 - 3.5ns	500ps
PCI to PCI	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns
USB & DOT	Asynch	N/A	Asynch	N/A	Asynch	N/A	Asynch	N/A

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V ±5%, VDDL=2.5 V± 5%(unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND			600	mA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guaranteed by design, not 100% tested in production.

0470E—04/06/05

Electrical Characteristics - CPU

T_A = 0 - 70°C; V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	$Vo=V_{DD}*(0.5)$	13.5	15	45	Ω
Output Impedance[1]	R_{DSN2B}	$Vo=V_{DD}*(0.5)$	13.5	16.5	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2	2.48		V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA		0.04	0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$ = 1 V		-60	-27	mA
		$V_{OH@MAX}$ = 2.375V	-27	-7		
Output Low Current	I_{OL2B}	$V_{OL@MIN}$ = 1.2 V	27	63		mA
		$V_{OL@MAX}$ =0.3V		20	30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	0.95	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	0.85	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45	50	55	%
Skew[1]	t_{sk2B}	V_T = 1.25 V		32	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V, CPU 66, SDRAM 100		200	250	ps
		CPU 100, SDRAM 100		165	250	
		CPU 133, SDRAM 100		400	450	
		CPU 133, SDRAM 133		180	250	

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70°C; V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP4B}	$Vo=V_{DD}*(0.5)$	9		30	Ω
Output Impedance[1]	R_{DSN4B}	$Vo=V_{DD}*(0.5)$	9		30	Ω
Output High Voltage	V_{OH4B}	I_{OH} = -5.5 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH4B}	$V_{OH@MIN}$ = 1.4 V			-21	mA
		$V_{OH@MAX}$ = 2.5V	-36			
Output Low Current	I_{OL4B}	$V_{OL@MIN}$ = 1.0 V	36			mA
		$V_{OL@MAX}$ =0.2V			31	
Rise Time[1]	t_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	0.9	1.6	ns
Fall Time[1]	t_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1	1.6	ns
Duty Cycle[1]	d_{t4B}	V_T = 1.25 V	45	50	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc4B}$	V_T = 1.25 V		250	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP3}	Vo=V_{DD}*(0.5)	10		24	Ω
Output Impedance[1]	R_{DSN3}	Vo=V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH3}	$V_{OH@MIN}$ = 2 V			-46	mA
		$V_{OH@MAX}$ = 3.135V	-54			
Output Low Current	I_{OL3}	$V_{OL@MIN}$ = 1 V	54			mA
		$V_{OL@MAX}$ =0.4V			53	
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.2	1.6	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	0.9	1.6	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk3}	V_T = 1.5 V		218	250	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc-cyc3}$	V_T = 1.5 V		225	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP1}	V_O = V_{DD}*(0.5)	12		55	Ω
Output Impedance[1]	R_{DSN1}	V_O = V_{DD}*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	$V_{OH\ @\ MIN}$ = 1.0 V			-33	mA
		$V_{OH\ @\ MAX}$ = 3.135 V	-33			
Output Low Current	I_{OL1}	$V_{OL\ @\ MIN}$ = 1.95 V	30			mA
		$V_{OL\ @\ MAX}$ = 0.4 V			38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.55	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.65	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	53	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		94	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		350	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, C_L = 10 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP1}	$Vo=V_{DD}*(0.5)$	12		55	Ω
Output Impedance[1]	R_{DSN1}	$Vo=V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	$V_{OH@MIN}$ = 1 V			-33	mA
		$V_{OH@MAX}$ = 3.135V	-33			
Output Low Current	I_{OL1}	$V_{OL@MIN}$ = 1.95 V	30			mA
		$V_{OL@MAX}$ =0.4V			38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V, PCI0-2	0.5	1.2	2	ns
		PCI3-7		2.1	2.25	
Fall Time[1]	t_{f1}	V_{OL} = 2.4 V, V_{OH} = 0.4 V, PCI0-2	0.5	1	2	ns
		PCI3-7		2	2.25	
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	51	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		480	500	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		300	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 24_48MHz, 48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP5}	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance[1]	R_{DSN5}	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH5}	$V_{OH\ @\ MIN}$ = 1.0 V			-23	mA
		$V_{OH\ @\ MAX}$ = 3.135 V	-29			
Output Low Current	I_{OL5}	$V_{OL\ @\ MIN}$ = 1.95 V	29			mA
		$V_{OL\ @\ MAX}$ = 0.4 V			27	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	53	55	%
Jitter, cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, 24, 48 MHz		250	500	ps
		V_T = 1.5 V, Ref clocks		2000	3000	

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

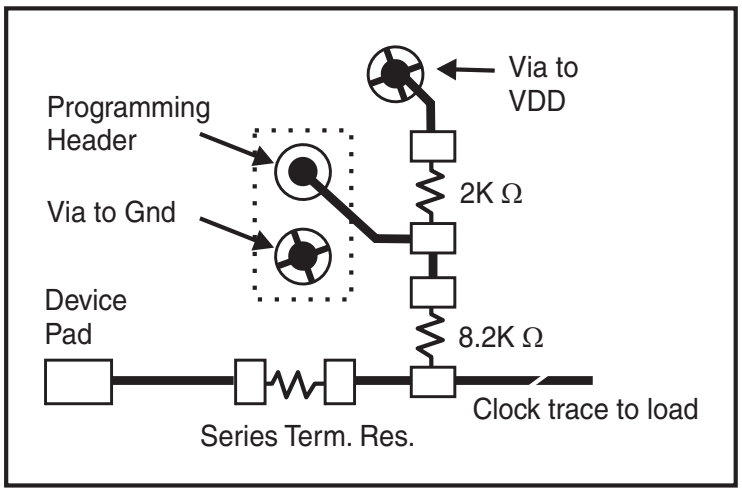
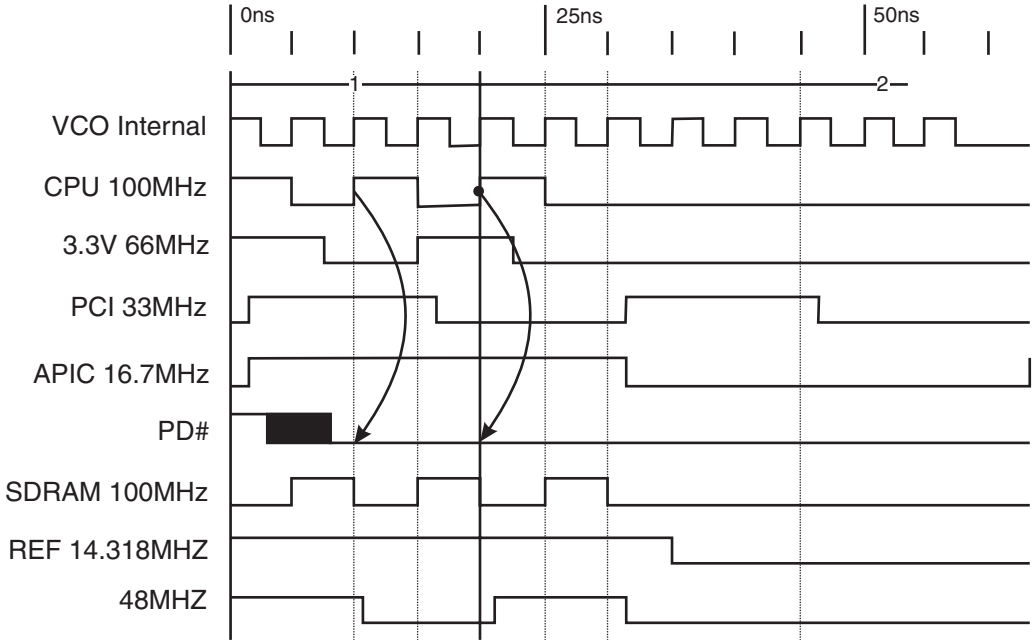


Fig. 1

Power Down Waveform

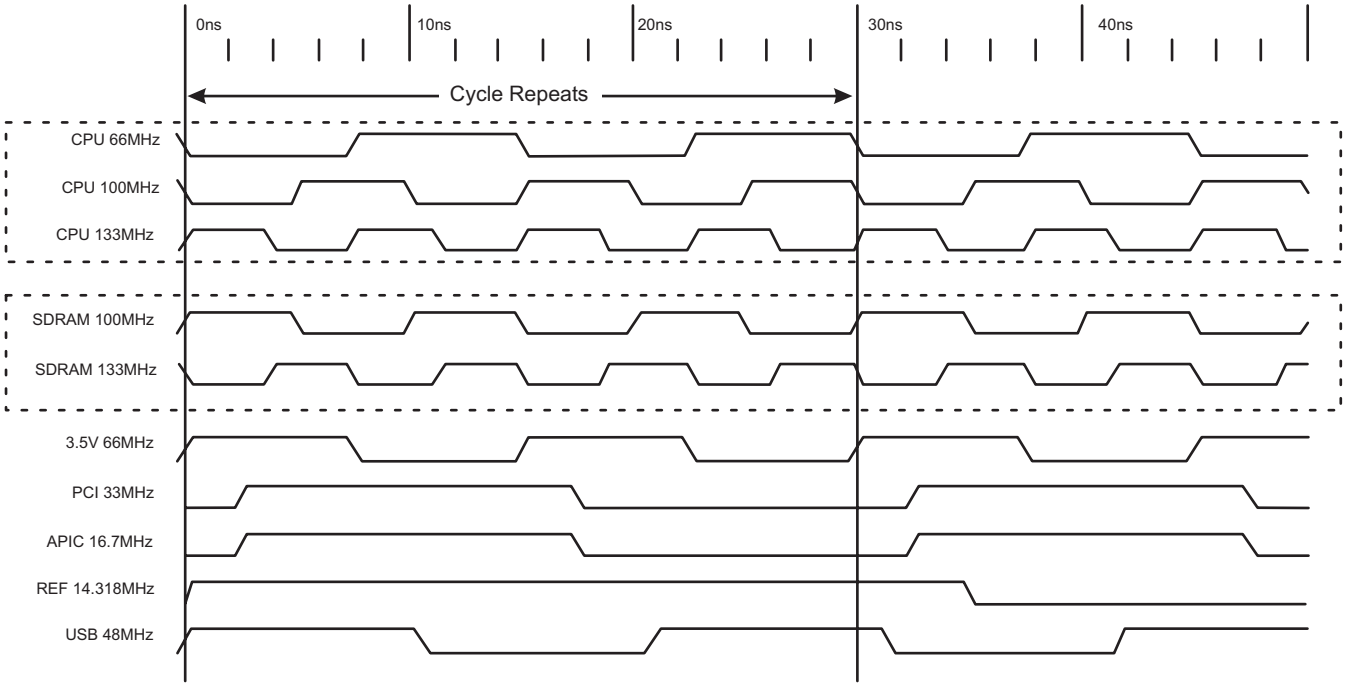


Note

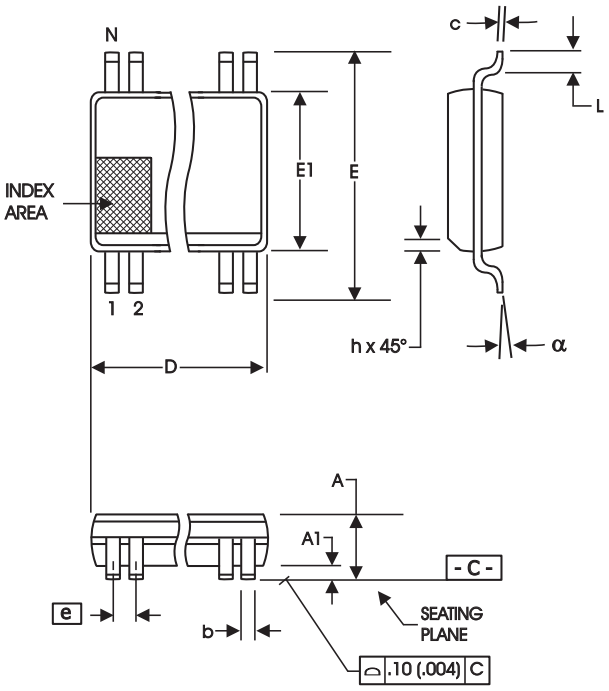
1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz



Group Offset Waveforms



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950508yFLF-T

Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0470E—04/06/05

Revision History

Rev.	Issue Date	Description	Page #
D	3/15/2005	Update default values of Bytes 18-20	9-10
E	4/6/2005	Update Byte 13 spread programming information	8

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