Integrated Circuit Systems, Inc.

ICS952011

Programmable Timing Control Hub™ for P4™ processor

Recommended Application:

SIS 645/645DX/648/650 style chipsets.

Output Features:

- 2 - Pairs of differential CPUCLKs (differential current mode)
- 1 - SDRAM @ 3.3V
- 9 - PCI @3.3V (including 2 free-running)
- 2 - AGP @ 3.3V
- 2 - ZCLKs @ 3.3V
- 1- 12/48MHZ @ 3.3V
- 1- 24/48MHz, @3.3V selectable by I^2C
- 3- REF @3.3V, 14.318MHz.

Key Specifications:

- PCI - PCI output skew: < 500ps
- CPU - SDRAM output skew: < 1ns
- AGP - AGP output skew: <150ps

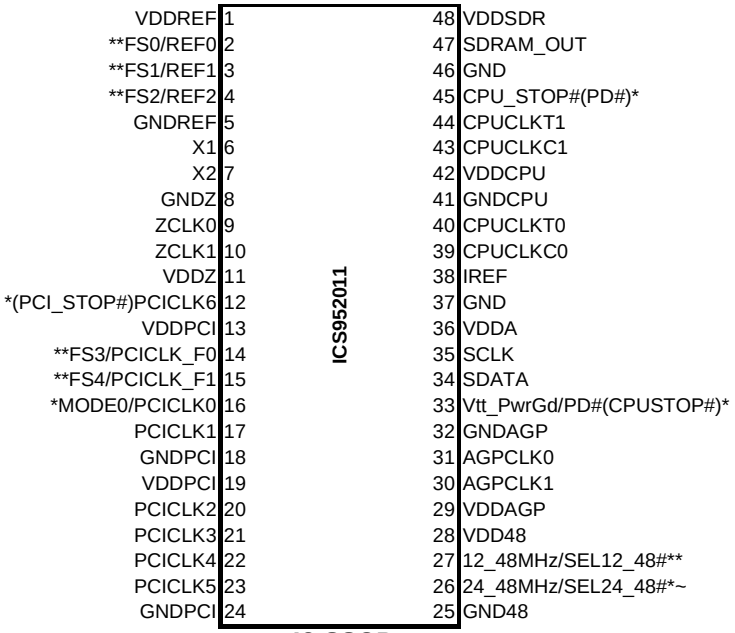
Features/Benefits:

- Selectable asynchronous/synchronous AGP, ZCLK and PCI outputs
- Supports DDR333 OEM frequencies
- Programmable output frequency, divider ratios, output rise/falltime, output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- For PC133 SDRAM system use the ICS9179-16 as the memory buffer.
- For DDR SDRAM system use the ICS93735 or ICS93732 as the memory buffer.
- Uses external 14.318MHz crystal.

Functionality

Bit2	Bit7	Bit6	Bit5	Bit4	CPU	SDR	AGP	PCI	ZCLK
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	0	0	0	0	100.20	100.20	66.80	33.40	66.80
0	0	0	0	1	100.20	133.60	66.80	33.40	66.80
0	0	0	1	0	100.20	200.40	66.80	33.40	66.80
0	0	0	1	1	100.20	167.00	66.80	33.40	66.80
0	0	1	0	0	133.60	100.20	66.80	33.40	66.80
0	0	1	0	1	133.60	133.60	66.80	33.40	66.80
0	0	1	1	0	133.60	200.40	66.80	33.40	66.80
0	0	1	1	1	133.60	167.00	66.80	33.40	66.80
0	1	0	0	0	200.05	100.03	66.68	33.34	66.68
0	1	0	0	1	200.05	133.37	66.68	33.34	66.68
0	1	0	1	0	200.05	200.05	66.68	33.34	66.68
0	1	0	1	1	200.05	160.04	66.68	33.34	66.68
0	1	1	0	0	166.70	100.20	66.68	33.40	66.68
0	1	1	0	1	166.70	133.36	66.80	33.40	66.80
0	1	1	1	0	160.04	200.05	66.68	33.34	66.68
0	1	1	1	1	166.70	166.70	66.68	33.34	66.68
1	0	0	0	0	100.20	100.20	66.80	33.40	133.60
1	0	0	0	1	100.20	133.60	66.80	33.40	133.60
1	0	0	1	0	100.20	200.40	66.80	33.40	133.60
1	0	0	1	1	100.20	167.00	66.80	33.40	133.60
1	0	1	0	0	133.60	100.20	66.80	33.40	133.60
1	0	1	0	1	133.60	133.60	66.80	33.40	133.60
1	0	1	1	0	133.60	200.40	66.80	33.40	133.60
1	0	1	1	1	133.60	167.00	66.80	33.40	133.60
1	1	0	0	0	200.05	100.03	66.68	33.34	133.37
1	1	0	0	1	200.05	133.37	66.68	33.34	133.37
1	1	0	1	0	200.05	200.05	66.68	33.34	133.37
1	1	0	1	1	200.05	160.04	66.68	33.34	133.37
1	1	1	0	0	166.70	100.20	66.68	33.40	133.60
1	1	1	0	1	166.70	133.36	66.80	33.40	133.60
1	1	1	1	0	160.04	200.05	66.68	33.34	133.37
1	1	1	1	1	166.70	166.70	66.68	33.34	133.37

Pin Configuration



48-SSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

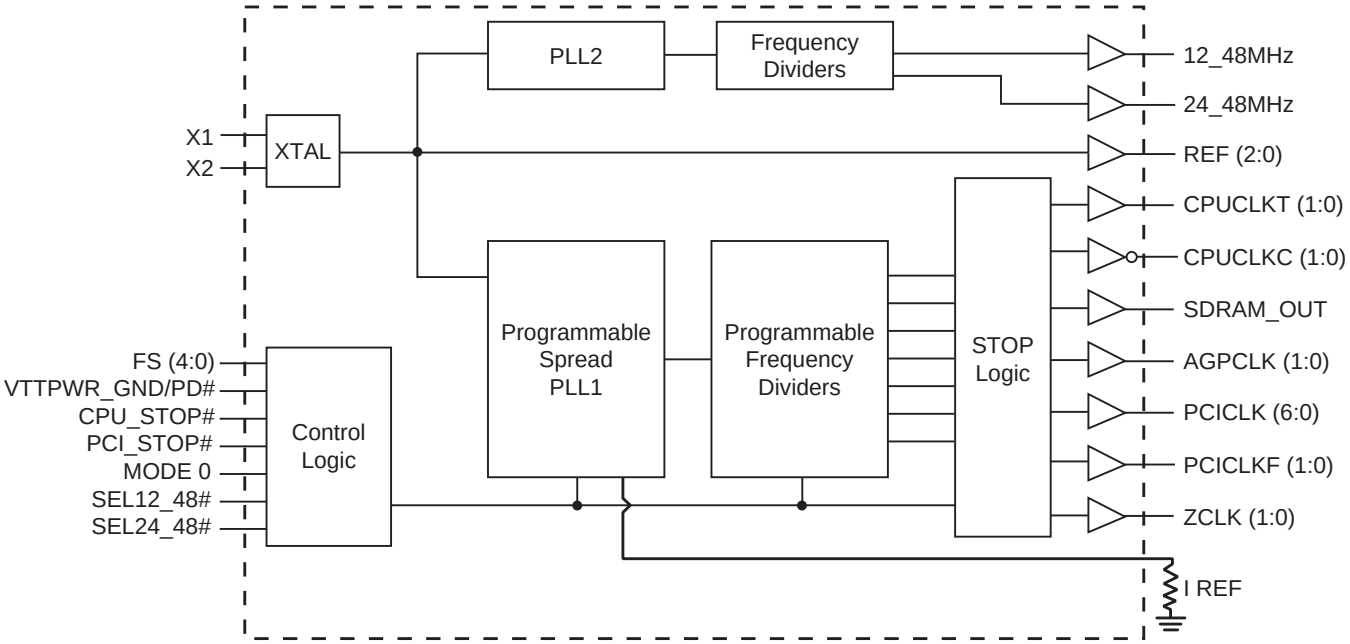
~ This output has 1.5X drive strength

General Description

The **ICS952011** is a two chip clock solution for desktop designs using SIS 645/645DX/648/650 style chipsets. When used with a zero delay buffer such as the ICS9179-16 for PC133 or the ICS93735 for DDR applications it provides all the necessary clocks signals for such a system.

The **ICS952011** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
1	5	REF Output, Crystal
11	8	Hyper ZCLK outputs
28	25	12/24/48MHz, Fix Analog, Fix Digital
29	32	AGP outputs
36	37	CPU PLL, CPU Analog, MCLK
42	41	CPU_T/C outputs
48	46	SDRAM_Out

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	**FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
3	**FS1/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
4	**FS2/REF2	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
5	GNDREF	PWR	Ground pin for the REF outputs.
6	X1	IN	Crystal input, Nominally 14.318MHz.
7	X2	OUT	Crystal output, Nominally 14.318MHz
8	GNDZ	PWR	Ground pin for the ZCLK outputs
9	ZCLK0	OUT	3.3V Hyperzip clock output.
10	ZCLK1	OUT	3.3V Hyperzip clock output.
11	VDDZ	PWR	Power supply for ZCLK clocks, nominal 3.3V
12	*(PCI_STOP#)PCICLK6	I/O	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low. This input is activated by the MODE selection pin / PCI clock output.
13	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
14	**FS3/PCICLK_F0	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
15	**FS4/PCICLK_F1	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
16	*MODE0/PCICLK0	I/O	Function select latch input pin, 1=Desktop Mode, 0=Mobile Mode / PCI clock output.
17	PCICLK1	OUT	PCI clock output.
18	GNDPCI	PWR	Ground pin for the PCI outputs
19	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
20	PCICLK2	OUT	PCI clock output.
21	PCICLK3	OUT	PCI clock output.
22	PCICLK4	OUT	PCI clock output.
23	PCICLK5	OUT	PCI clock output.
24	GNDPCI	PWR	Ground pin for the PCI outputs
25	GND48	PWR	Ground pin for the 48MHz outputs
26	24_48MHz/SEL24_48#*~	I/O	24MHz/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 24MHz.
27	12_48MHz/SEL12_48#**	I/O	12MHz/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 12MHz.
28	VDD48	PWR	Power pin for the 48MHz output.3.3V
29	VDDAGP	PWR	Power supply for AGP clocks, nominal 3.3V
30	AGPCLK1	OUT	AGP clock output
31	AGPCLK0	OUT	AGP clock output
32	GNDAGP	PWR	Ground pin for the AGP outputs
33	Vtt_PwrGd/PD#(CPUSTOP#)*	I/O	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. Active low Power Down input or active low CPU_STOP depend on B24b3 IIC selection. Default is PD#.
34	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
35	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
36	VDDA	PWR	3.3V power for the PLL core.
37	GND	PWR	Ground pin.
38	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
39	CPUCLKC0	OUT	"Complimentary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
40	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
41	GNDCPU	PWR	Ground pin for the CPU outputs
42	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
43	CPUCLKC1	OUT	"Complimentary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
44	CPUCLKT1	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	CPU_STOP#(PD#)*	IN	Active low CPU_STOP or Active low Power Down input depend on B24b3 IIC selection. Default is CPU_STOP#.
46	GND	PWR	Ground pin.
47	SDRAM_OUT	OUT	SDRAM seed clock output for external buffer
48	VDDSDR	PWR	Supply for SDRAM clocks, nominal 3.3V.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor

Table 6: CPUCLK Swing Select Functions

Byte 24 Bit 0 MULTSEL0	Byte 23 Bit 7 MULTSEL1	Board Target Trace/Term Z	Reference R, Iref = Vdd/(3*Rr)	Output Current	Voh @ Z, Iref=2.32mA
0	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.71V @ 60
0	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
0	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
1	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.85V /2 60
1	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.71V @ 50
1	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.60 @ 20
0	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.5V @ 20
1	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.90V @ 30
1	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.75V @ 20
1	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	0.84V @ 20

General I²C serial interface information for the ICS952011

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address D3(H)		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
	X Byte	Beginning Byte N
ACK		
		O
O		O
O		O
O		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

Table1: QuadRom Frequency Selection Table

B24	B24	Bit2	Bit7	Bit6	Bit5	Bit4	CPU	SDR	AGP	PCI	ZCLK
Bit6	Bit5	FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	0	0	0	0	0	0	100.20	100.20	66.80	33.40	66.80
0	0	0	0	0	0	1	100.20	133.60	66.80	33.40	66.80
0	0	0	0	0	1	0	100.20	200.40	66.80	33.40	66.80
0	0	0	0	0	1	1	100.20	167.00	66.80	33.40	66.80
0	0	0	0	1	0	0	133.60	100.20	66.80	33.40	66.80
0	0	0	0	1	0	1	133.60	133.60	66.80	33.40	66.80
0	0	0	0	1	1	0	133.60	200.40	66.80	33.40	66.80
0	0	0	0	1	1	1	133.60	167.00	66.80	33.40	66.80
0	0	0	1	0	0	0	200.05	100.03	66.68	33.34	66.68
0	0	0	1	0	0	1	200.05	133.37	66.68	33.34	66.68
0	0	0	1	0	1	0	200.05	200.05	66.68	33.34	66.68
0	0	0	1	0	1	1	200.05	160.04	66.68	33.34	66.68
0	0	0	1	1	0	0	166.70	100.20	66.68	33.40	66.68
0	0	0	1	1	0	1	166.70	133.36	66.80	33.40	66.80
0	0	0	1	1	1	0	160.04	200.05	66.68	33.34	66.68
0	0	0	1	1	1	1	166.70	166.70	66.68	33.34	66.68
0	0	1	0	0	0	0	100.20	100.20	66.80	33.40	133.60
0	0	1	0	0	0	1	100.20	133.60	66.80	33.40	133.60
0	0	1	0	0	1	0	100.20	200.40	66.80	33.40	133.60
0	0	1	0	0	1	1	100.20	167.00	66.80	33.40	133.60
0	0	1	0	1	0	0	133.60	100.20	66.80	33.40	133.60
0	0	1	0	1	0	1	133.60	133.60	66.80	33.40	133.60
0	0	1	0	1	1	0	133.60	200.40	66.80	33.40	133.60
0	0	1	0	1	1	1	133.60	167.00	66.80	33.40	133.60
0	0	1	1	0	0	0	200.05	100.03	66.68	33.34	133.37
0	0	1	1	0	0	1	200.05	133.37	66.68	33.34	133.37
0	0	1	1	0	1	0	200.05	200.05	66.68	33.34	133.37
0	0	1	1	0	1	1	200.05	160.04	66.68	33.34	133.37
0	0	1	1	1	0	0	166.70	100.20	66.68	33.40	133.60
0	0	1	1	1	0	1	166.70	133.36	66.80	33.40	133.60
0	0	1	1	1	1	0	160.04	200.05	66.68	33.34	133.37
0	0	1	1	1	1	1	166.70	166.70	66.68	33.34	133.37

Table1: QuadRom Frequency Selection Table (Continued)

B24	B24	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	SDR	AGP	PCI	ZCLK
Bit6	Bit5	FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	1	0	0	0	0	0	100.00	100.00	66.66	33.33	66.66
0	1	0	0	0	0	1	100.00	133.33	66.66	33.33	66.66
0	1	0	0	0	1	0	100.00	200.00	66.66	33.33	66.66
0	1	0	0	0	1	1	100.00	166.67	66.66	33.33	66.66
0	1	0	0	1	0	0	133.33	100.00	66.66	33.33	66.66
0	1	0	0	1	0	1	133.33	133.33	66.66	33.33	66.66
0	1	0	0	1	1	0	133.33	200.00	66.66	33.33	66.66
0	1	0	0	1	1	1	133.33	166.67	66.66	33.33	66.66
0	1	0	1	0	0	0	200.00	100.00	66.66	33.33	66.66
0	1	0	1	0	0	1	200.00	133.33	66.66	33.33	66.66
0	1	0	1	0	1	0	200.00	200.00	66.66	33.33	66.66
0	1	0	1	0	1	1	200.00	160.00	66.66	33.33	66.66
0	1	0	1	1	0	0	166.66	100.00	66.66	33.33	66.66
0	1	0	1	1	0	1	166.67	133.33	66.66	33.33	66.66
0	1	0	1	1	1	0	160.00	200.00	66.66	33.33	66.66
0	1	0	1	1	1	1	166.67	166.67	66.66	33.33	66.66
0	1	1	0	0	0	0	100.00	100.00	66.66	33.33	133.33
0	1	1	0	0	0	1	100.00	133.33	66.66	33.33	133.33
0	1	1	0	0	1	0	100.00	200.00	66.66	33.33	133.33
0	1	1	0	0	1	1	100.00	166.67	66.66	33.33	133.33
0	1	1	0	1	0	0	133.33	100.00	66.66	33.33	133.33
0	1	1	0	1	0	1	133.33	133.33	66.66	33.33	133.33
0	1	1	0	1	1	0	133.33	200.00	66.66	33.33	133.33
0	1	1	0	1	1	1	133.33	166.67	66.66	33.33	133.33
0	1	1	0	0	0	0	200.00	100.00	66.66	33.33	133.33
0	1	1	0	0	0	1	200.00	133.33	66.66	33.33	133.33
0	1	1	0	0	1	0	200.00	200.00	66.66	33.33	133.33
0	1	1	0	0	1	1	200.00	160.00	66.66	33.33	133.33
0	1	1	1	1	0	0	166.66	100.00	66.66	33.33	133.33
0	1	1	1	1	0	1	166.67	133.33	66.66	33.33	133.33
0	1	1	1	1	1	0	160.00	200.00	66.66	33.33	133.33
0	1	1	1	1	1	1	166.67	166.67	66.66	33.33	133.33

Table1: QuadRom Frequency Selection Table (Continued)

B24	B24	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	SDR	AGP	PCI	ZCLK
Bit6	Bit5	FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	1	0	0	0	0	0	100.20	100.20	66.80	33.40	80.16
0	1	0	0	0	0	1	100.20	133.60	66.80	33.40	80.16
0	1	0	0	0	1	0	100.20	200.40	66.80	33.40	80.16
0	1	0	0	0	1	1	100.20	167.00	66.80	33.40	80.16
0	1	0	0	1	0	0	133.60	100.20	66.80	33.40	80.16
0	1	0	0	1	0	1	133.60	133.60	66.80	33.40	80.16
0	1	0	0	1	1	0	133.60	200.40	66.80	33.40	80.16
0	1	0	0	1	1	1	133.60	167.00	66.80	33.40	80.16
0	1	0	1	0	0	0	200.05	100.03	66.68	33.34	80.02
0	1	0	1	0	0	1	200.05	133.37	66.68	33.34	80.02
0	1	0	1	0	1	0	200.05	200.05	66.68	33.34	80.02
0	1	0	1	0	1	1	200.05	160.04	66.68	33.34	80.02
0	1	0	1	1	0	0	166.70	100.20	66.68	33.40	80.16
0	1	0	1	1	0	1	166.70	133.36	66.80	33.40	80.16
0	1	0	1	1	1	0	160.04	200.05	66.68	33.34	80.02
0	1	0	1	1	1	1	166.70	166.70	66.68	33.34	80.02
0	1	1	0	0	0	0	100.20	100.20	66.80	33.40	100.20
0	1	1	0	0	0	1	100.20	133.60	66.80	33.40	100.20
0	1	1	0	0	1	0	100.20	200.40	66.80	33.40	100.20
0	1	1	0	0	1	1	100.20	167.00	66.80	33.40	100.20
0	1	1	0	1	0	0	133.60	100.20	66.80	33.40	100.20
0	1	1	0	1	0	1	133.60	133.60	66.80	33.40	100.20
0	1	1	0	1	1	0	133.60	200.40	66.80	33.40	100.20
0	1	1	0	1	1	1	133.60	167.00	66.80	33.40	100.20
0	1	1	0	0	0	0	200.05	100.03	66.68	33.34	100.03
0	1	1	0	0	0	1	200.05	133.37	66.68	33.34	100.03
0	1	1	0	0	1	0	200.05	200.05	66.68	33.34	100.03
0	1	1	0	0	1	1	200.05	160.04	66.68	33.34	100.03
0	1	1	1	1	0	0	166.70	100.20	66.68	33.40	100.20
0	1	1	1	1	0	1	166.70	133.36	66.80	33.40	100.20
0	1	1	1	1	1	0	160.04	200.05	66.68	33.34	100.03
0	1	1	1	1	1	1	166.70	166.70	66.68	33.34	100.03

Table1: QuadRom Frequency Selection Table (Continued)

B24	B24	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	SDR	AGP	PCI	ZCLK
Bit6	Bit5	FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	1	0	0	0	0	0	100.00	100.00	66.66	33.33	80.00
0	1	0	0	0	0	1	100.00	133.33	66.66	33.33	80.00
0	1	0	0	0	1	0	100.00	200.00	66.66	33.33	80.00
0	1	0	0	0	1	1	100.00	166.67	66.66	33.33	80.00
0	1	0	0	1	0	0	133.33	100.00	66.66	33.33	80.00
0	1	0	0	1	0	1	133.33	133.33	66.66	33.33	80.00
0	1	0	0	1	1	0	133.33	200.00	66.66	33.33	80.00
0	1	0	0	1	1	1	133.33	166.67	66.66	33.33	80.00
0	1	0	1	0	0	0	200.00	100.00	66.66	33.33	80.00
0	1	0	1	0	0	1	200.00	133.33	66.66	33.33	80.00
0	1	0	1	0	1	0	200.00	200.00	66.66	33.33	80.00
0	1	0	1	0	1	1	200.00	160.00	66.66	33.33	80.00
0	1	0	1	1	0	0	166.66	100.00	66.66	33.33	80.00
0	1	0	1	1	0	1	166.67	133.33	66.66	33.33	80.00
0	1	0	1	1	1	0	160.00	200.00	66.66	33.33	80.00
0	1	0	1	1	1	1	166.67	166.67	66.66	33.33	80.00
0	1	1	0	0	0	0	100.00	100.00	66.66	33.33	100.00
0	1	1	0	0	0	1	100.00	133.33	66.66	33.33	100.00
0	1	1	0	0	1	0	100.00	200.00	66.66	33.33	100.00
0	1	1	0	0	1	1	100.00	166.67	66.66	33.33	100.00
0	1	1	0	1	0	0	133.33	100.00	66.66	33.33	100.00
0	1	1	0	1	0	1	133.33	133.33	66.66	33.33	100.00
0	1	1	0	1	1	0	133.33	200.00	66.66	33.33	100.00
0	1	1	0	1	1	1	133.33	166.67	66.66	33.33	100.00
0	1	1	0	0	0	0	200.00	100.00	66.66	33.33	100.00
0	1	1	0	0	0	1	200.00	133.33	66.66	33.33	100.00
0	1	1	0	0	1	0	200.00	200.00	66.66	33.33	100.00
0	1	1	0	0	1	1	200.00	160.00	66.66	33.33	100.00
0	1	1	1	1	0	0	166.66	100.00	66.66	33.33	100.00
0	1	1	1	1	0	1	166.67	133.33	66.66	33.33	100.00
0	1	1	1	1	1	0	160.00	200.00	66.66	33.33	100.00
0	1	1	1	1	1	1	166.67	166.67	66.66	33.33	100.00

I²C Table: Function Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PDEN	PD# Enable	RW	Disable	Enable	1
Bit 6	-	AZCLKFS	Async Zclk Freq Select in N-programming (Mode 01, see table 3)	RW	66.6MHz	133.3MHz	1
Bit 5	-	WDS_EN	WD Soft Enable	RW	Disable	Enable	1
Bit 4	-	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 3	-	AZCLKFS	Async Zclk Freq Select (Mode 10 & 11, see table 3)	RW	66MHz	132MHz	1
Bit 2	-	Reserved	Reserved	RW	-		1
Bit 1	-	AEN1	Zclk/Agp/Pci Freq Source Select Control	RW	See Table 3 : ZCLK, AGP & PCI Frequency Source Decode Table		0
Bit 0	-	AEN0		RW			0

Table 3: ZCLK Frequency Source Decode Table

Byte0 Bit1	Byte0 Bit0	ZCLK & AGP & PCI
0	0	See Table 1, QuadRom Frequency Table
0	1	N-Programming for ZCLK/AGP/PCI
1	0	See Table 1 for AGP/PCI, B0b3 for ZCLK freq
1	1	N-Prog for AGP/PCI, B0b3 for ZCLK freq

I²C Table: Async N-Programming Frequency Select Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N PLL3 Div7	The decimal representation of N PLL2 Div (7:0) + 8 is equal to VCO divider value for PLL2. Default at power up = 66.67MHz	RW	-	-	0
Bit 6	-	N PLL3 Div6		RW	-	-	1
Bit 5	-	N PLL3 Div5		RW	-	-	0
Bit 4	-	N PLL3 Div4		RW	-	-	0
Bit 3	-	N PLL3 Div3		RW	-	-	0
Bit 2	-	N PLL3 Div2		RW	-	-	1
Bit 1	-	N PLL3 Div1		RW	-	-	1
Bit 0	-	N PLL3 Div0		RW	-	-	1

I²C Table: Reserved Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5		Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

Byte1 (7:0) Hex	VCO Freq	AGP Freq	PCI Freq
26	360.34	60.06	30.03
27	361.53	60.26	30.13
28	362.73	60.45	30.23
29	363.92	60.65	30.33
2A	365.11	60.85	30.43
2B	366.31	61.05	30.53
2C	367.50	61.25	30.62
2D	368.69	61.45	30.72
2E	369.89	61.65	30.82
2F	371.08	61.85	30.92
30	372.27	62.05	31.02
31	373.47	62.24	31.12
32	374.66	62.44	31.22
33	375.85	62.64	31.32
34	377.05	62.84	31.42
35	378.24	63.04	31.52
36	379.43	63.24	31.62
37	380.62	63.44	31.72
38	381.82	63.64	31.82
39	383.01	63.84	31.92
3A	384.20	64.03	32.02
3B	385.40	64.23	32.12
3C	386.59	64.43	32.22
3D	387.78	64.63	32.32
3E	388.98	64.83	32.41
3F	390.17	65.03	32.51
40	391.36	65.23	32.61
41	392.56	65.43	32.71
42	393.75	65.62	32.81
43	394.94	65.82	32.91
44	396.14	66.02	33.01
45	397.33	66.22	33.11
46	398.52	66.42	33.21
47	399.72	66.62	33.31
48	400.91	66.82	33.41
49	402.10	67.02	33.51
4A	403.30	67.22	33.61
4B	404.49	67.41	33.71

Byte1 (7:0) Hex	VCO Freq	AGP Freq	PCI Freq
4C	405.68	67.61	33.81
4D	406.87	67.81	33.91
4E	408.07	68.01	34.01
4F	409.26	68.21	34.11
50	410.45	68.41	34.20
51	411.65	68.61	34.30
52	412.84	68.81	34.40
53	414.03	69.01	34.50
54	415.23	69.20	34.60
55	416.42	69.40	34.70
56	417.61	69.60	34.80
57	418.81	69.80	34.90
58	420.00	70.00	35.00
59	421.19	70.20	35.10
5A	422.39	70.40	35.20
5B	423.58	70.60	35.30
5C	424.77	70.80	35.40
5D	425.97	70.99	35.50
5E	427.16	71.19	35.60
5F	428.35	71.39	35.70
60	429.55	71.59	35.80
61	430.74	71.79	35.89
62	431.93	71.99	35.99
63	433.12	72.19	36.09
64	434.32	72.39	36.19
65	435.51	72.59	36.29
66	436.70	72.78	36.39
67	437.90	72.98	36.49
68	439.09	73.18	36.59
69	440.28	73.38	36.69
6A	441.48	73.58	36.79
6B	442.67	73.78	36.89
6C	443.86	73.98	36.99
6D	445.06	74.18	37.09
6E	446.25	74.37	37.19
6F	447.44	74.57	37.29
70	448.64	74.77	37.39
71	449.83	74.97	37.49

Byte1 (7:0) Hex	VCO Freq	AGP Freq	PCI Freq
72	451.02	75.17	37.59
73	452.22	75.37	37.68
74	453.41	75.57	37.78
75	454.60	75.77	37.88
76	455.80	75.97	37.98
77	456.99	76.16	38.08
78	458.18	76.36	38.18
79	459.37	76.56	38.28
7A	460.57	76.76	38.38
7B	461.76	76.96	38.48
7C	462.95	77.16	38.58
7D	464.15	77.36	38.68
7E	465.34	77.56	38.78
7F	466.53	77.76	38.88
80	467.73	77.95	38.98
81	468.92	78.15	39.08
82	470.11	78.35	39.18
83	471.31	78.55	39.28
84	472.50	78.75	39.37
85	473.69	78.95	39.47
86	474.89	79.15	39.57
87	476.08	79.35	39.67
88	477.27	79.55	39.77
89	478.47	79.74	39.87
8A	479.66	79.94	39.97
8B	480.85	80.14	40.07
8C	482.05	80.34	40.17
8D	483.24	80.54	40.27
8E	484.43	80.74	40.37
8F	485.62	80.94	40.47
90	486.82	81.14	40.57
91	488.01	81.34	40.67
92	489.20	81.53	40.77
93	490.40	81.73	40.87
94	491.59	81.93	40.97
95	492.78	82.13	41.07
96	493.98	82.33	41.16
97	495.17	82.53	41.26

Byte1 (7:0) Hex	VCO Freq	AGP Freq	PCI Freq
98	496.36	82.73	41.36
99	497.56	82.93	41.46
9A	498.75	83.12	41.56
9B	499.94	83.32	41.66
9C	501.14	83.52	41.76
9D	502.33	83.72	41.86
9E	503.52	83.92	41.96
9F	504.72	84.12	42.06
A0	505.91	84.32	42.16
A1	507.10	84.52	42.26
A2	508.30	84.72	42.36
A3	509.49	84.91	42.46
A4	510.68	85.11	42.56
A5	511.87	85.31	42.66
A6	513.07	85.51	42.76
A7	514.26	85.71	42.86
A8	515.45	85.91	42.95
A9	516.65	86.11	43.05
AA	517.84	86.31	43.15
AB	519.03	86.51	43.25
AC	520.23	86.70	43.35
AD	521.42	86.90	43.45
AE	522.61	87.10	43.55
AF	523.81	87.30	43.65
B0	525.00	87.50	43.75
B1	526.19	87.70	43.85
B2	527.39	87.90	43.95
B3	528.58	88.10	44.05
B4	529.77	88.30	44.15
B5	530.97	88.49	44.25
B6	532.16	88.69	44.35
B7	533.35	88.89	44.45
B8	534.55	89.09	44.55
B9	535.74	89.29	44.64
BA	536.93	89.49	44.74
BB	538.12	89.69	44.84
BC	539.32	89.89	44.94
BD	540.51	90.09	45.04

I²C Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5		Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Frequency Select Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS3	Freq Select Bit 7	RW	See Table1 : Quad Rom Frequency Selection Table		0
Bit 6	-	FS2	Freq Select Bit 6	RW			0
Bit 5	-	FS1	Freq Select Bit 5	RW			0
Bit 4	-	FS0	Freq Select Bit 4	RW			0
Bit 3	-	FS Source	Frequency HW/IIC Select	RW	Latch Input	IIC	0
Bit 2	-	FS4	Freq Select Bit 2	RW	See Table1		0
Bit 1	-	SS_EN	Spread Enable	RW	OFF	ON	1
Bit 0	-	Outputs	Output Control	RW	Running	Tri-state	0

I²C Table: Read Back Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDHRB	WD Hard Alarm Status Read back	R	Normal	Alarm	X
Bit 6	-	WDSRB	WD Soft Alarm Status Read back	R	Normal	Alarm	X
Bit 5	-	MULTISEL	Multisel Read back	R	-	-	X
Bit 4	-	FS4RB	FS4 Read back	R	-	-	X
Bit 3	-	FS3RB	FS3 Read back	R	-	-	X
Bit 2	-	FS2RB	FS2 Read back	R	-	-	X
Bit 1	-	FS1RB	FS1 Read back	R	-	-	X
Bit 0	-	FS0RB	FS0 Read back	R	-	-	X

I²C Table: Output Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	10	ZCLK_1	Output Control	RW	Disable	Enable	1
Bit 6	9	ZCLK_0	Output Control	RW	Disable	Enable	1
Bit 5	14	PCI_F0	PCI_STOP# Control	RW	Stop Disable	Stop Enable	0
Bit 4	15	PCI_F1	PCI_STOP# Control	RW	Stop Disable	Stop Enable	0
Bit 3	40, 39	CPUT0/C0	CPU_STOP# Control	RW	Stop Disable	Stop Enable	1
Bit 2	44, 43	CPUT1/C1	CPU_STOP# Control	RW	Stop Disable	Stop Enable	1
Bit 1	40, 39	CPUT0/C0	Output Control	RW	Disable	Enable	1
Bit 0	44, 43	CPUT1/C1	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	15	PCICLK_F1	Output Control	RW	Disable	Enable	1
Bit 6	14	PCICLK_F0	Output Control	RW	Disable	Enable	1
Bit 5	23	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	22	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	21	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	20	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	17	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	16	PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

I²C Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WD7	These bits represent X*290ms the watchdog timer will wait before it goes to alarm mode. Default is 16 X 290ms =4.64 seconds	RW	-	-	0
Bit 6	-	WD6		RW	-	-	0
Bit 5	-	WD5		RW	-	-	0
Bit 4	-	WD4		RW	-	-	1
Bit 3	-	WD3		RW	-	-	0
Bit 2	-	WD2		RW	-	-	0
Bit 1	-	WD1		RW	-	-	0
Bit 0	-	WD0		RW	-	-	0

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WDEN	Watchdog Enable	R	Disable	Enable	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	WD SF4	Writing to these bit will configure the safe frequency as Byte4bit 2, (7:4)	RW	-	-	0
Bit 3	-	WD SF3		RW	-	-	0
Bit 2	-	WD SF2		RW	-	-	0
Bit 1	-	WD SF1		RW	-	-	0
Bit 0	-	WD SF0		RW	-	-	1

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Bit 8	RW	-	-	X
Bit 6	-	M Div6	The decimal representation of M Div (6:0) + 2 is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 5	-	M Div5		RW	-	-	X
Bit 4	-	M Div4		RW	-	-	X
Bit 3	-	M Div3		RW	-	-	X
Bit 2	-	M Div2		RW	-	-	X
Bit 1	-	M Div1		RW	-	-	X
Bit 0	-	M Div0		RW	-	-	X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	The decimal representation of N Div (8:0) + 8 is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 6	-	N Div6		RW	-	-	X
Bit 5	-	N Div5		RW	-	-	X
Bit 4	-	N Div4		RW	-	-	X
Bit 3	-	N Div3		RW	-	-	X
Bit 2	-	N Div2		RW	-	-	X
Bit 1	-	N Div1		RW	-	-	X
Bit 0	-	N Div0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	These Spread Spectrum bits will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 6	-	SSP6		RW	-	-	X
Bit 5	-	SSP5		RW	-	-	X
Bit 4	-	SSP4		RW	-	-	X
Bit 3	-	SSP3		RW	-	-	X
Bit 2	-	SSP2		RW	-	-	X
Bit 1	-	SSP1		RW	-	-	X
Bit 0	-	SSP0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	Reserved	Reserved	R	-	-	0
Bit 5	-	SSP13	It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 4	-	SSP12		RW	-	-	X
Bit 3	-	SSP11		RW	-	-	X
Bit 2	-	SSP10		RW	-	-	X
Bit 1	-	SSP9		RW	-	-	X
Bit 0	-	SSP8		RW	-	-	X

I²C Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SDDiv3	SD divider ratio can be configured via these 4 bits individually.	RW	See Table 4: Divider Ratio Combination Table		X
Bit 6	-	SDDiv2		RW			X
Bit 5	-	SDDiv1		RW			X
Bit 4	-	SDDiv0		RW			X
Bit 3	-	CPU Div3	CPU divider ratio can be configured via these 4 bits individually.	RW	See Table 4: Divider Ratio Combination Table		X
Bit 2	-	CPU Div2		RW			X
Bit 1	-	CPU Div1		RW			X
Bit 0	-	CPU Div0		RW			X

Table 4: CPU, SDR Divider Ratio Combination Table

	Divider (3:2)								
Divider (1:0)	Bit	00		01		10		11	MSB
			1		2		4		8
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	7	0111	14	1011	28	1111	56
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	X
Bit 6	-	Reserved	Reserved	RW	-	-	X
Bit 5	-	Reserved	Reserved	RW	-	-	X
Bit 4	-	Reserved	Reserved	RW	-	-	X
Bit 3	-	Reserved	Reserved	RW	-	-	X
Bit 2	-	Reserved	Reserved	RW	-	-	X
Bit 1	-	Reserved	Reserved	RW	-	-	X
Bit 0	-	Reserved	Reserved	RW	-	-	X

I²C Table: Output Divider Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	X
Bit 6	-	Reserved	Reserved	RW	-	-	X
Bit 5	-	SDINV	SD Phase Invert	RW	Default	Inverse	X
Bit 4	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	X
Bit 3	-	Reserved	Reserved	RW	-	-	X
Bit 2	-	Reserved	Reserved	RW	-	-	X
Bit 1	-	Reserved	Reserved	RW	-	-	X
Bit 0	-	Reserved	Reserved	RW	-	-	X

I²C Table: Group Skew Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUSkw1	CPU-CPU Skew Control	RW	See Table 5: 4-Steps Skew Programming Table		1
Bit 6	-	CPUSkw0		RW			1
Bit 5	-	SDSkw1	CPU-SD Skew Control	RW	See Table 5: 4-Steps Skew Programming Table		0
Bit 4	-	SDSkw0		RW			0
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	ZCLKSkw1	CPU-ZCLK Skew Control	RW	See Table 5: 4-Steps Skew Programming Table		0
Bit 6	-	ZCLKSkw0		RW			0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	AGPSkw1	CPU-AGP Skew Control	RW	See Table 5: 4-Steps Skew Programming Table		0
Bit 2	-	AGPSkw0		RW			0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCI_FSkw1	CPU-PCI_F Skew Control	RW	See Table 5: 4-Steps Skew Programming Table		0
Bit 6	-	PCI_FSkw0		RW			0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	PCISkw1	CPU-PCI Skew Control	RW	See Table 5: 4-Steps Skew Programming Table		0
Bit 2	-	PCISkw0		RW			0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

Table 5: 4-Steps Skew Programming Table

4 Step	0	1	LSB
0	0ps	250ps	-
1	500ps	750ps	-
MSB	-	-	-

I²C Table: Slew Rate Control Register

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	24/48Slw1	24/48 Slew Rate Control	RW	-	-	0
Bit 6	-	24/48Slw0		RW	-	-	0
Bit 5	-	AGPSlw1	AGP Slew Rate Control	RW	-	-	0
Bit 4	-	AGPSlw0		RW	-	-	0
Bit 3	-	ZCLKSlw1	ZCLK Slew Rate Control	RW	-	-	0
Bit 2	-	ZCLKSlw0		RW	-	-	0
Bit 1	-	REFSlw1	REF Slew Rate Control	RW	-	-	0
Bit 0	-	REFSlw0		RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 22	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SDSlw1	SD Slew Rate Control	RW	-	-	0
Bit 6	-	SDSlw0		RW	-	-	0
Bit 5	30	AGPCLK1	Output Control	RW	Disable	Enable	1
Bit 4	31	AGPCLK0	Output Control	RW	Disable	Enable	1
Bit 3	-	PCI_FSlw1	PCI_F Slew Rate Control	RW	-	-	0
Bit 2	-	PCI_FSlw0		RW	-	-	0
Bit 1	-	PCISlw1	PCI Slew Rate Control	RW	-	-	0
Bit 0	-	PCISlw0		RW	-	-	0

I²C Table: Output Control Register

Byte 23	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	MultSel1	IREF X plier Control	RW	See Table 6		0
Bit 6	26	SEL24_48	24MHz or 48MHz	RW	48MHz	24MHz	1
Bit 5	47	SDRAM_OUT	Output Control	RW	Disable	Enable	1
Bit 4	27	12_48MHz	Output Control	RW	Disable	Enable	1
Bit 3	26	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 2	4	REF2	Output Control	RW	Disable	Enable	1
Bit 1	3	REF1	Output Control	RW	Disable	Enable	1
Bit 0	2	REF0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 24	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	27	SEL12_48	12MHz or 48MHz	RW	48MHz	12MHz	0
Bit 6	-	FS6	Freq Select bit 6	RW	See Table 1		0
Bit 5		FS5	Freq Select bit 5	RW			0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	45,33	STOP_PD Swap	Swap CPU_STOP# and PD# location	RW	Stop-Pin33 PD#-Pin45	Stop-Pin45 PD#-Pin33	1
Bit 2	-	SS_SEL	SS Scheme Select1	RW	See Table 2: Spread Spectrum Selection Table		0
Bit 1	-	SS_SEL	SS Scheme Select1	RW			0
Bit 0	-	MultSel0	IREF X plier Control	RW	See Table 6: MultSel Selection Table		1

Table2: Spread Spectrum Select Table

SS1 (Byte 24 bit 2)	SS0 (Byte 24 bit 1)	QuadRom Sec1&3 b(6:5,FS3 Byte4:bit7) = 000, 100	QuadRom Sec1&3 b(6:5,FS3 Byte4:bit7) = 001, 101	QuadRom Sec2&4 b(6:3) = 0011
0	0	OFF	0.35%	0.40%
0	1	OFF	0.50%	0.55%
1	0	0.22%	0.75%	0.80%
1	1	0.48%	1.00%	1.00%

Absolute Maximum Ratings

Core Supply Voltage	4.6 V
I/O Supply Voltage	3.6V
Logic Inputs	GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Case Temperature	115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD(op)}$	C_L = 0 pF; Select @ 100MHz		213	280	mA
Power Down Supply Current	I_{DDPD}	C_L = 0 pF; With input address to V_{DD} or GND		15	40	mA
Input frequency	F_i	V_{DD} = 3.3 V	11		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.		1.8	3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.		1	3	ms
Skew[1]	$T_{CPU-PCI}$	V_T = 1.5 V	1.5	2.19	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V,+/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.1			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16		57	mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.96	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.95	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	51.6	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		70	500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		100	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLKT/C

T_A = 0 - 70°C; V_{DD}=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	757	850	mV
Voltage Low	VLow		-150	9	150	
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		775	1150	mV
Min Voltage	Vuds		-450	-3		
Crossing Voltage (abs)	Vcross(abs)		250	386	550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		42	140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	300	700	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	280	700	ps
Rise Time Variation	d-t_r				125	ps
Fall Time Variation	d-t_f				125	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	50	55	%
Skew	t_{sk3}	V_T = 50%		32	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		43	150	ps

Electrical Characteristics - ZCLK

T_A = 0 - 70°C; V_{DD}=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.36	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.37	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.3	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		15	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66		201	250	ps

Electrical Characteristics - AGPCLK

T_A = 0 - 70°C; V_{DD}=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.83	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.69	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.7	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		32	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66		240	250	ps

Electrical Characteristics - 12_48MHz, 24_48MHz

T_A = 0 - 70°C; V_{DD}=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V	-29			
		$V_{OH@MAX}$ = 3.135 V			-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V	29			
		$V_{OL@MAX}$ = 0.4 V			27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.27	1	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.4	1	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.7	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		268	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V , +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.98	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.87	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	54.2	55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V		213	1000	ps

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

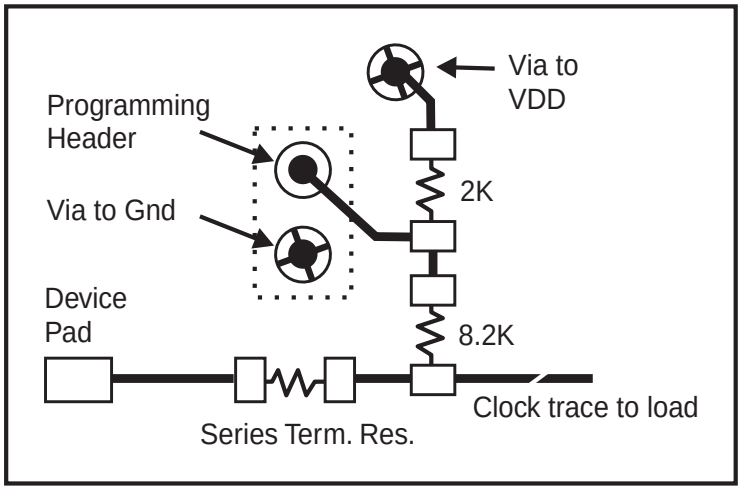
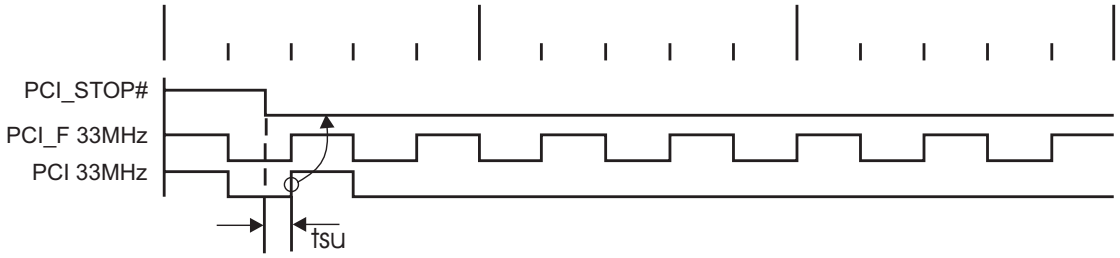


Fig. 1

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI and stoppable PCI_F clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

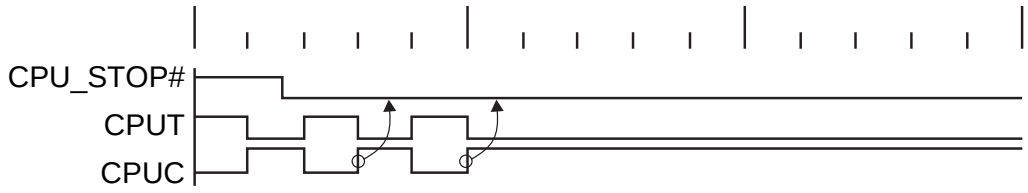
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

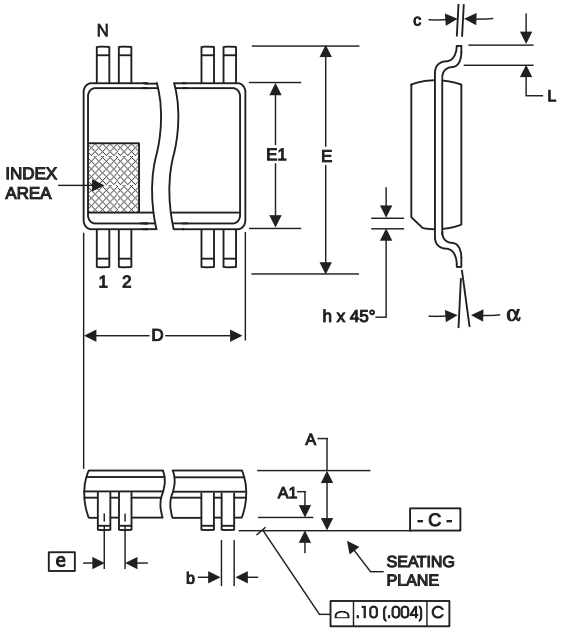
The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=Low and CPUC=High. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS952011yFT

Example:

ICS XXXXXX y F - T

- **Designation for tape and reel packaging**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0721A—07/29/03