Integrated Circuit Systems, Inc.

ICS952301

Advance Information

Frequency Timing Generator for Transmeta Systems

Recommended Application:

Transmeta

Output Features:

- 1CPU up to 66.6MHz & overclocking of 66MHz.
- 7 PCI (3.3V) @ 33.3MHz (all are free running selectable) w/ 2 selectable 1X/2X.
- 1 REF (3.3V) at 14.318MHz.
- 1 48MHz (3.3V).
- 1 24_48MHz selectable output.

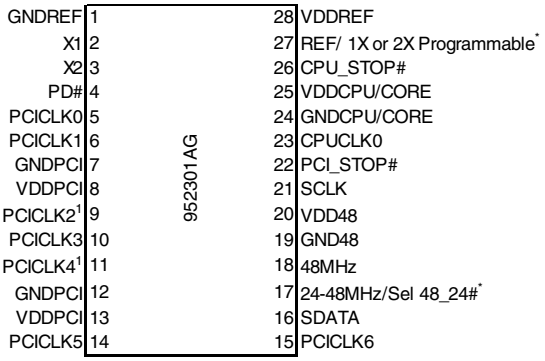
Features:

- Supports Spread Spectrum modulation for CPU and PCI clocks, default -2.0% downspread.
- Efficient Power management scheme through stop clocks and power down modes.
- Uses external 14.318MHz crystal, no external load cap required for CL=18pF crystal.
- 28-pin TSSOP package, 4.40mm (173mil).

Skew Characteristics:

- PCI – PCI ≤ 500ps
- CPU(early) – PCI = 1.5ns – 4ns.

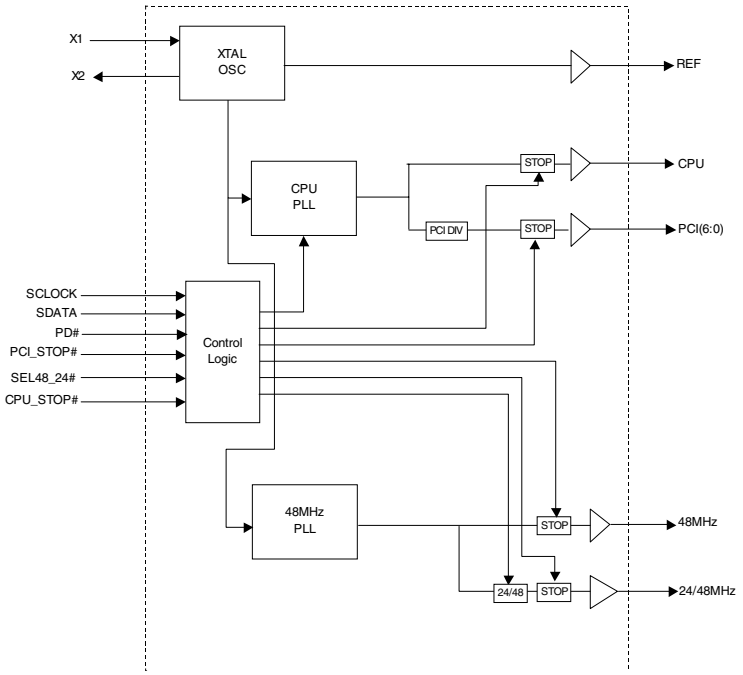
Pin Configuration



28-Pin 173mil TSSOP

Note: ^ Internal Pulldown Resistor
* Internal Pullup Resistor
1 1X/2X Programmable

Block Diagram



Power Groups

VDD_Core, GND_Core = PLL core
VDDREF, GNDREF = REF, X1, X2
VDDPCI, GNDPCI = PCICLK (6:0)
VDD48, GND48 = 48MHz (1:0)

Pentium is a trademark on Intel Corporation.

Pin Descriptions

PIN #	PIN	PIN TYPE	DESCRIPTION
1	GNDREF	PWR	Ground pin.
2	X1	IN	Crystal input, nominally 14.318MHz.
3	X2	OUT	Crystal output, nominally 14.318MHz.
4	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
5	PCICLK0	OUT	PCI clock outputs.
6	PCICLK1	OUT	PCI clock outputs.
7	GNDPCI	PWR	Ground pin.
8	VDDPCI	PWR	Supply for PCI, nominal 3.3V.
9	PCICLK21	OUT	PCI clock outputs.
10	PCICLK3	OUT	PCI clock outputs.
11	PCICLK41	OUT	PCI clock outputs.
12	GNDPCI	PWR	Ground pin.
13	VDDPCI	PWR	Supply for PCI, nominal 3.3V.
14	PCICLK5	OUT	PCI clock outputs.
15	PCICLK6	OUT	PCI clock outputs.
16	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
17	24-48MHz/Sel 48_24#*	I/O	Selectable 48 or 24MHz output
18	48MHz	OUT	48MHz output clock
19	GND48	PWR	Ground pin.
20	VDD48	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
21	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
22	PCI_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
23	CPUCLK0	OUT	CPU clock outputs.
24	GNDCPU/CORE	PWR	Ground pin.
25	VDDCPU/CORE	PWR	3.3V power for the PLL core.
26	CPU_STOP#	IN	Stops all CPUCLKs besides the CPUCLK_F clocks at logic 0 level, when input low
27	REF/ 1X or 2X Programmable*	OUT	14.318 MHz reference clock. Latched input select for strength of PCICLK(4,2). Default 1X with internal pullup.
28	VDDREF	PWR	3.3V power for the REF.

ICS952301 Power Management Requirements

PD#	CPU STOP#	PCI STOP#	Byte 0 Bit 0	VCO	CPUCLK 0	PCICLK Not Free Run	PCICLK Free-Run	24 MHz	48 MHZ	REF
0	X	X	X	STOP	LOW	LOW	LOW	LOW	LOW	LOW
1	0	1	0	RUN	STOP	RUN	RUN	RUN	RUN	RUN
1	1	0	0	RUN	RUN	STOP	RUN	RUN	RUN	RUN
1	1	1	1	RUN	Tri-State	Tri-State	Tri-State	Tri-State	Tri-State	Tri-State

Note: If Byte 3 bit [7:2]=0 Not Free-Run, can be controlled by PCI_STOP#
If Byte 3 bit [7:2]=1 Free-Run, cannot controlled by PCI_STOP#

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Bit2	Bit7	Bit6	Bit5	Bit4	CPU	PCI
	FS4	FS3	FS2	FS1	FS0		
Bit 2,7:4	0	0	0	0	0	60	30
	0	0	0	0	1	60	30
	0	0	0	1	0	60	30
	0	0	0	1	1	60	30
	0	0	1	0	0	66.6	33.3
	0	0	1	0	1	66.6	33.3
	0	0	1	1	0	66.6	33.3
	0	0	1	1	1	66.6	33.3
	0	1	0	0	0	67.32	33.66
	0	1	0	0	1	68.64	34.32
	0	1	0	1	0	69.96	34.98
	0	1	0	1	1	72.6	36.3
	0	1	1	0	0	61.5	30.75
	0	1	1	0	1	63	31.5
	0	1	1	1	0	64	32
	0	1	1	1	1	65	32.5
	1	0	0	0	0	60	30
	1	0	0	0	1	66.6	33.3
	1	0	0	1	0	50	25
	1	0	0	1	1	48	24
	1	0	1	0	0	58.8	29.4
	1	0	1	0	1	57.6	28.8
	1	0	1	1	0	56.4	28.2
	1	0	1	1	1	54	27
	1	1	0	0	0	60	30
	1	1	0	0	1	60	30
	1	1	0	1	0	60	30
	1	1	0	1	1	60	30
	1	1	1	0	0	66.6	33.3
	1	1	1	0	1	66.6	33.3
	1	1	1	1	0	66.6	33.3
	1	1	1	1	1	66.6	33.3
Bit3	Reserved						
Bit1	0-Normal 1-Spread spectrun Enabled						
Bit0	0-Running 1-Tristate all outputs						

Note: PWD = Power-Up Default

BYTE 0	Affected Pin		Control Function	TYPE	Bit Control		PWD
	Pin #	Name			0	1	
Bit 7	-	-	Frequency select by bit 7	RW	See Frequency table		1
Bit 6	-	-	Frequency select by bit 6	RW			1
Bit 5	-	-	Frequency select by bit 5	RW			1
Bit 4			Frequency select by bit 4	RW			1
Bit 3	-	-	Reserved	R	-	-	1
Bit 2	-	-	Frequency select by bit 2	RW	See Frequency table		1
Bit 1	-	-	Spread Enable	RW	Normal	Enable	0
Bit 0	-	-	Output Control	RW	Running	Tri-state	0

BYTE 2	Affected Pin		Control Function	TYPE	Bit Control		PWD
	Pin #	Name			0	1	
Bit 7	18	48MHz	Output Disable	RW	Disable	Enable	1
Bit 6	17	24_48MHz	Output Disable	RW	Disable	Enable	1
Bit 5	23	CPUCLK0	Output disable	RW	Disable	Enable	1
Bit 4	27	REF	Output disable	RW	Disable	Enable	1
Bit 3	9	PCICLK2	1X or 2X	RW	2X	1X	1
Bit 2	11	PCICLK4	1X or 2X	RW	2X	1X	1
Bit 1	-	-	PCI HW SEL Status	R	2X	1X	1
Bit 0	-	-	(Reserved)	-	-	-	X

BYTE 4	Affected Pin		Control Function	TYPE	Bit Control		PWD
	Pin #	Name			0	1	
Bit 7	-	-	(Reserved)	-	-	-	X
Bit 6	-	-	(Reserved)	-	-	-	X
Bit 5	-	-	(Reserved)	-	-	-	X
Bit 4	-	-	(Reserved)	-	-	-	X
Bit 3	-	-	(Reserved)	-	-	-	X
Bit 2	-	-	(Reserved)	-	-	-	X
Bit 1	-	-	(Reserved)	-	-	-	X
Bit 0	-	-	(Reserved)	-	-	-	X

BYTE 6	Affected Pin		Control Function	TYPE	Bit Control		PWD
	Pin #	Name			0	1	
Bit 7	-	-	(Reserved)	-	-	-	0
Bit 6	-	-	(Reserved)	-	-	-	0
Bit 5	-	-	(Reserved)	-	-	-	0
Bit 4	-	-	(Reserved)	-	-	-	0
Bit 3	-	-	(Reserved)	-	-	-	0
Bit 2	-	-	(Reserved)	-	-	-	1
Bit 1	-	-	(Reserved)	-	-	-	1
Bit 0	-	-	(Reserved)	-	-	-	0

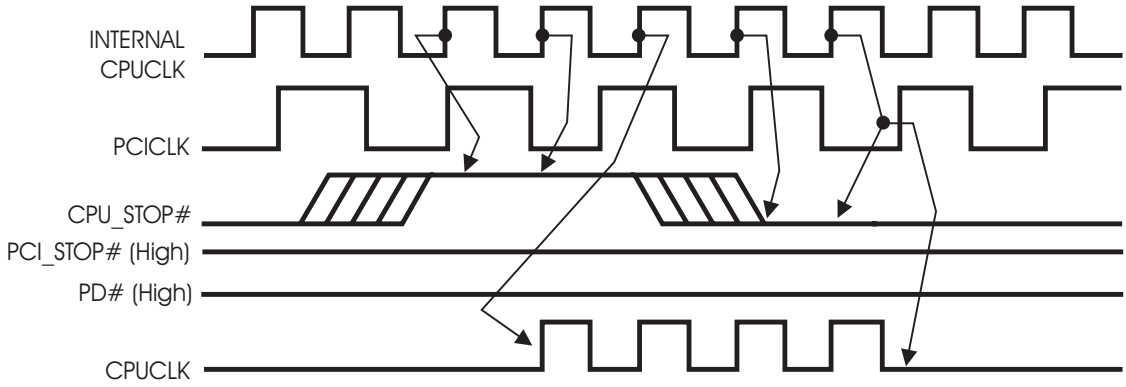
BYTE 1	Affected Pin		Control Function	TYPE	Bit Control		PWD
	Pin #	Name			0	1	
Bit 7	15	PCICLK6	Output disable	RW	Disable	Enable	1
Bit 6	14	PCICLK5	Output disable	RW	Disable	Enable	1
Bit 5	11	PCICLK4	Output disable	RW	Disable	Enable	1
Bit 4	10	PCICLK3	Output disable	RW	Disable	Enable	1
Bit 3	9	PCICLK2	Output disable	RW	Disable	Enable	1
Bit 2	6	PCICLK1	Output disable	RW	Disable	Enable	1
Bit 1	5	PCICLK0	Output disable	RW	Disable	Enable	1
Bit 0	-	-	(Reserved)	-	-	-	0

BYTE 3	Affected Pin		Control Function	TYPE	Bit Control		PWD
	Pin #	Name			0	1	
Bit 7	15	PCICLK6	Free Run Status	RW	Disable	Enable	1
Bit 6	14	PCICLK5	Free Run Status	RW	Disable	Enable	1
Bit 5	11	PCICLK4	Free Run Status	RW	Disable	Enable	1
Bit 4	10	PCICLK3	Free Run Status	RW	Disable	Enable	1
Bit 3	9	PCICLK2	Free Run Status	RW	Disable	Enable	1
Bit 2	6	PCICLK1	Free Run Status	RW	Disable	Enable	1
Bit 1	5	PCICLK0	Free Run Status	RW	Disable	Enable	1
Bit 0	-	-	(Reserved)	-	-	-	X

BYTE 5	Affected Pin		Control Function	TYPE	Bit Control		PWD
	Pin #	Name			0	1	
Bit 7	-	-	(Reserved)	-	-	-	X
Bit 6	-	-	(Reserved)	-	-	-	X
Bit 5	-	-	(Reserved)	-	-	-	X
Bit 4	-	-	(Reserved)	-	-	-	X
Bit 3	-	-	(Reserved)	-	-	-	X
Bit 2	-	-	(Reserved)	-	-	-	X
Bit 1	-	-	(Reserved)	-	-	-	X
Bit 0	-	-	(Reserved)	-	-	-	X

CPU_STOP# Timing Diagram

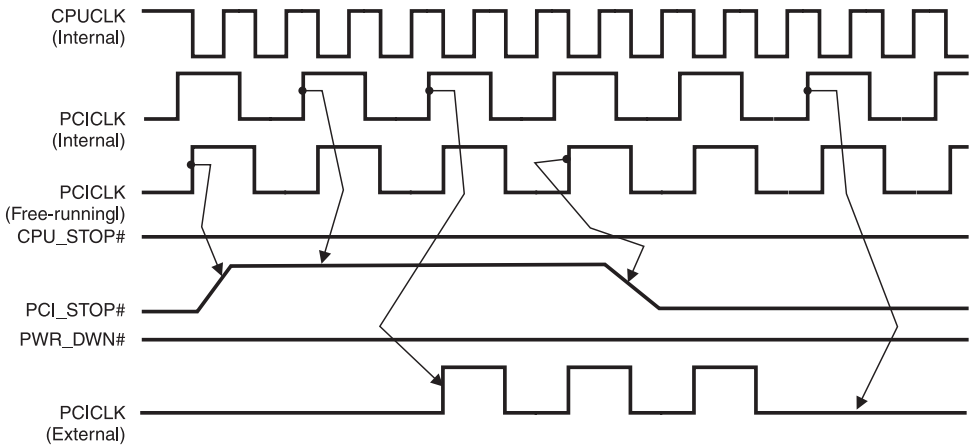
CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS952301**. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9248-192**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS952301**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS952301** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS952301 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS952301.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

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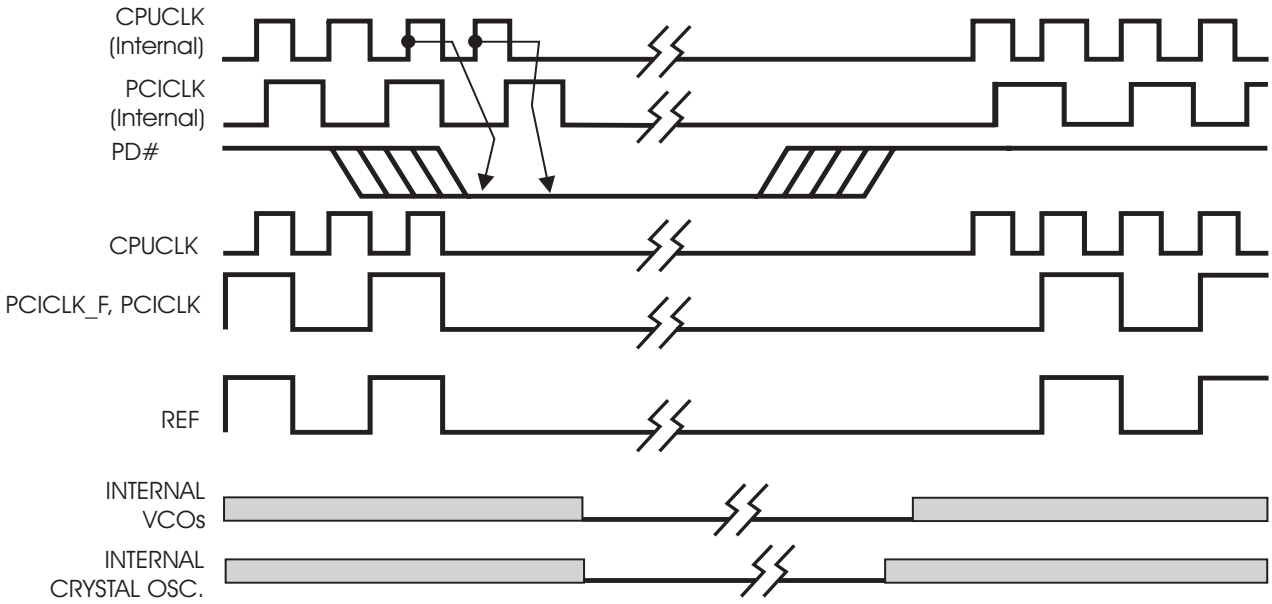
PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internally by the **ICS952301** prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the crystal oscillator. The power on latency is guaranteed to be less than 3ms. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS952301 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9248.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parame

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD(op)}$	C_L = 0 pF; Select @ 66MHz		11	180	mA
Power Down Supply Current	I_{DDPD}	C_L = 0 pF; With input address to Vdd or GND		0	600	µA
Input frequency	F_i	V_{DD} = 3.3 V;	11	14.32	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-PCI}$	V_T = 1.5 V	1.5	2	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

Output Type: 1

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5% C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedence	Rdsp	V_O = Vdd * 0.5	12	32	60	Ohm
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	1.8	2.1		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.15	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-32	-27	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	27	49		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.4	2	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.6	2	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.5 V	44	48	55	%
Skew	t_{sk2B}[1]	V_T = 1.5 V		18	175	ps
Jitter	$t_{jcyc-cyc2B}$[1]	V_T = 1.5 V		122	250	ps
	t_{jabs2B}[1]	V_T = 1.5 V	-250	198	+250	ps

Electrical Characteristics - REF

Output Type: 1

T_A = 0 - 70C; V_{DD} = 3.3 V, +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedence	Rdsp	V_O = Vdd * 0.5	12	32	60	Ohm
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-29	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	51		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.9	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.9	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52	55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V		559	1000	ps

Electrical Characteristics - 48MHz & 48/24MHz

Output Type: 1

T_A = 0 - 70C; V_{DD} = 3.3 V , +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

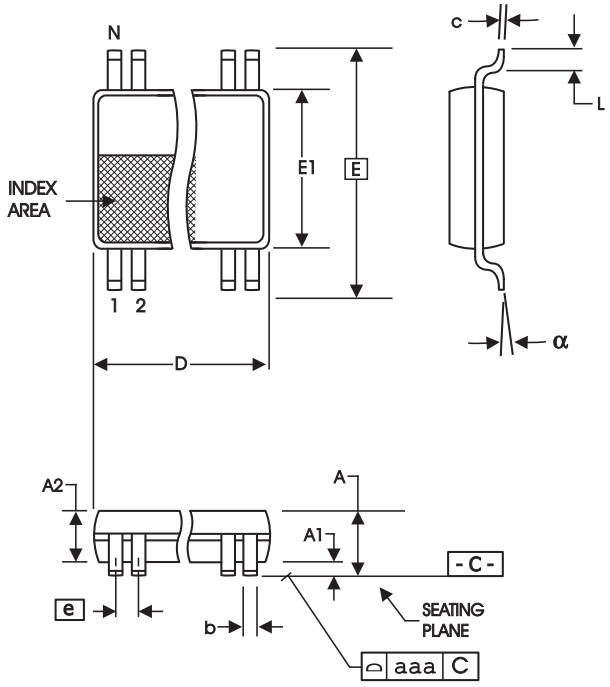
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedence	Rdsp	V_O = Vdd * 0.5	20	30	65	Ohm
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-29	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	51		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.7	1.2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		0.7	1.2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52	55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V		164	500	ps
	t_{jabs5}	V_T = 1.5 V		221	800	ps

Electrical Characteristics - PCICLK

Output Type: 5 PCICLK(6:0)

T_A = 0 - 70C; V_{DD} = 3.3 V,+/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedence	Rdsp	V_O = Vdd * 0.5	12	32	60	Ohm
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.1	2.8		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.15	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-75	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16	44	57	mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.6	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.8	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		16	500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		100	500	ps
	t_{jabs1}	V_T = 1.5 V		210	500	ps



4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

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Ordering Information

ICS952301yGT

Example:

ICS 95XXXX y G - T

- **Designation for tape and reel packaging**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

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