



## Programmable Timing Control Hub™ for Next Gen P4™ processor

### Recommended Application:

CK409 48-pin part

### Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 1 - 0.7V current-mode differential CPU pairs for ITP
- 1 - 0.7V current-mode differential SRC pair
- 9 - PCI (33MHz), including 3 free running PCI
- 1 - USB, 48MHz
- 1 - DOT, 48MHz
- 2 - REF, 14.318MHz
- 3 - 3V66, 66.66MHz
- 1 - 3V66/VCH, selectable 48MHz or 66MHz

### Key Specifications:

- CPU/SRC outputs cycle-cycle jitter < 125ps
- 3V66 outputs cycle-cycle jitter < 250ps
- PCI outputs cycle-cycle jitter < 250ps
- CPU outputs skew: < 100ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks

### Functionality

FS2 B6b5	FS A	FS B	CPU MHz	SRC MHz	3V66 MHz	PCI MHz	REF MHz	USB/ DOT MHz
0	0	0	100.00	100/200	66.66	33.33	14.318	48.00
	0	1	200.00	100/200	66.66	33.33	14.318	48.00
	1	0	133.33	100/200	66.66	33.33	14.318	48.00
	1	1	166.66	100/200	66.66	33.33	14.318	48.00
1	0	0	200.00	100/200	66.66	33.33	14.318	48.00
	0	1	400.00	100/200	66.66	33.33	14.318	48.00
	1	0	266.66	100/200	66.66	33.33	14.318	48.00
	1	1	333.33	100/200	66.66	33.33	14.318	48.00

### Features/Benefits:

- Supports tight ppm accuracy clocks for Serial-ATA
- Supports spread spectrum modulation, 0 to -0.5% down spread and +/- 0.25% center spread
- Supports CPU clks up to 400MHz in test mode
- Uses external 14.318MHz crystal
- Supports undriven differential CPU, SRC pair in PD# and CPU\_STOP# for power management.

### Pin Configuration

FS_A/REF1	1	48	VDDA
FS_B/REF0	2	47	GND
VDDREF	3	46	IREF
X1	4	45	CPUCLKT_ITP
X2	5	44	CPUCLKC_ITP
GND	6	43	GND
PCICLK_F0	7	42	CPUCLKT1
PCICLK_F1	8	41	CPUCLKC1
PCICLK_F2	9	40	VDDCPU
VDDPCI	10	39	CPUCLKT0
GND	11	38	CPUCLKC0
PCICLK0	12	37	GND
PCICLK1	13	36	SRCCLKT
PCICLK2	14	35	SRCCLKC
PCICLK3	15	34	VDD
VDDPCI	16	33	VttPWR_GD#
GND	17	32	SDATA
PCICLK4	18	31	SCLK
PCICLK5	19	30	3V66_0
PD#	20	29	3V66_1
48MHz_DOT	21	28	GND
48MHz_USB	22	27	VDD3V66
GND	23	26	3V66_2
VDD48	24	25	3V66_3/VCH

\*\*120KΩ pull-down

**48-pin SSOP**

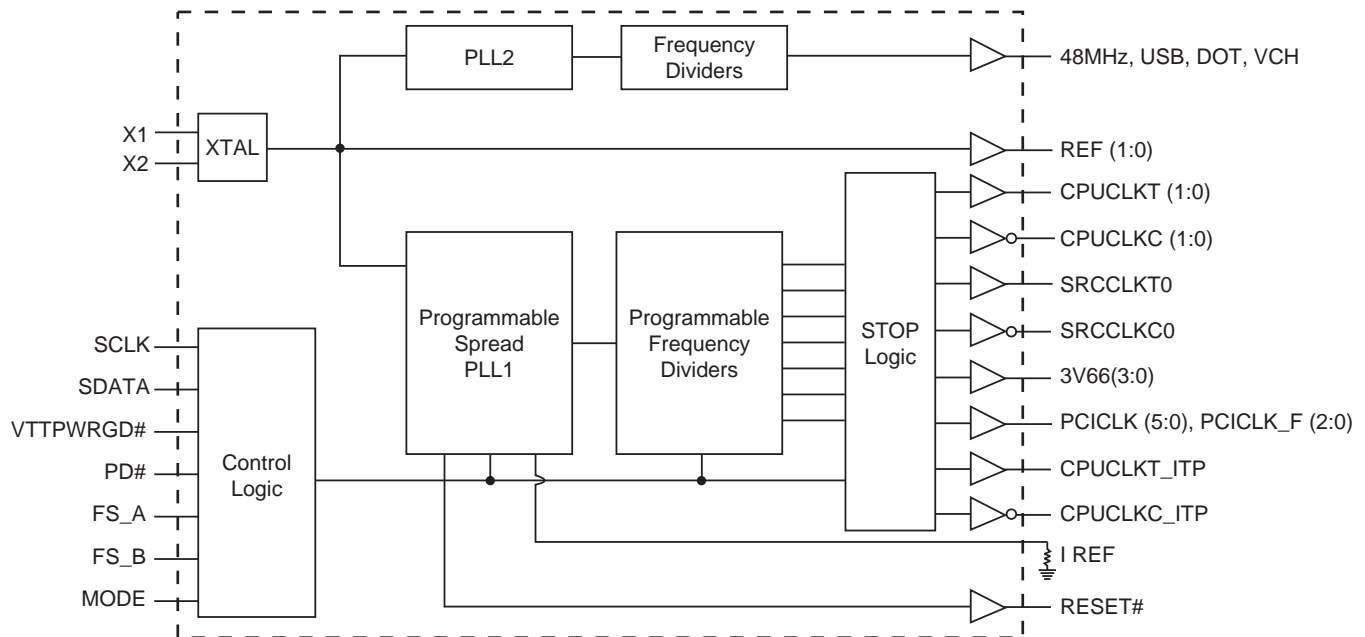
## Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	FS_A/REF1	I/O	FS_A latched input for frequency select Reference output, 14.318Hz
2	FS_B/REF0	I/O	FS_B latched input for frequency select Reference output, 14.318Hz
3	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
4	X1	IN	Crystal input, Nominally 14.318MHz.
5	X2	OUT	Crystal output, Nominally 14.318MHz
6	GND	PWR	Ground pin.
7	PCICLK_F0	OUT	Free running PCI clock not affected by PCI_STOP# .
8	PCICLK_F1	OUT	Free running PCI clock not affected by PCI_STOP# .
9	PCICLK_F2	OUT	Free running PCI clock not affected by PCI_STOP# .
10	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
11	GND	PWR	Ground pin.
12	PCICLK0	OUT	PCI clock output.
13	PCICLK1	OUT	PCI clock output.
14	PCICLK2	OUT	PCI clock output.
15	PCICLK3	OUT	PCI clock output.
16	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
17	GND	PWR	Ground pin.
18	PCICLK4	OUT	PCI clock output.
19	PCICLK5	OUT	PCI clock output.
20	PD#	IN	Asynchronous active low input pin, with 120Kohm internal pull-up resistor, used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped.
21	48MHz_DOT	OUT	48.008MHz Dot clock output
22	48MHz_USB	OUT	48.008MHz USB clock output
23	GND	PWR	Ground pin.
24	VDD48	PWR	Power for 48MHz output buffers and fixed PLL core.
25	3V66_3/VCH	OUT	3.3V 66.66MHz clock output VCH: 48MHz VCH clock output
26	3V66_2	OUT	3.3V 66.66MHz clock output
27	VDD3V66	PWR	Power pin for the 3V66 clocks.
28	GND	PWR	Ground pin.
29	3V66_1	OUT	3.3V 66.66MHz clock output
30	3V66_0	OUT	3.3V 66.66MHz clock output
31	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
32	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
33	VttPWR_GD#	IN	This 3.3V LVTTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input.
34	VDD	OUT	Power supply, nominal 3.3V
35	SRCCLKC	OUT	Complementary clock of differential pair for S-ATA support. +/- 300ppm accuracy required.
36	SRCCLKT	OUT	True clock of differential pair for S-ATA support. +/- 300ppm accuracy required.
37	GND	PWR	Ground pin.
38	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
39	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
40	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
41	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
42	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
43	GND	PWR	Ground pin.
44	CPUCLKC_ITP	OUT	"Complementary" clocks of differential pair CPU outputs for ITP.. These are current mode outputs. External resistors are required for voltage bias.
45	CPUCLKT_ITP	OUT	"True" clocks of differential pair CPU outputs for ITP. These are current mode outputs. External resistors are required for voltage bias.
46	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
47	GND	PWR	Ground pin.
48	VDDA	PWR	3.3V power for the PLL core.

## General Description

**ICS952621** is a programmable 48 pin clock chip following Intel CK409 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS952621** is driven with a 14.318MHz crystal. It generates CPU outputs up to 200MHz. It also provides a tight ppm accuracy output for Serial ATA support.

## Block Diagram



## Power Groups

Pin Number		Description
VDD	GND	
3	6	Xtal, Ref
27	28	3V66 [0:3]
10,16	11,17	PCICLK outputs
34	37	SRCCLK outputs
48	47	Master clock, CPU Analog
24	23	48MHz, Fix Digital, Fix Analog
--	47	IREF
40	43	CPUCLK clocks

**Absolute Max**

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		$V_{DD} + 0.5V$	V
VDD_In	3.3V Logic Input Supply Voltage	-0.5	$V_{DD} + 0.5V$	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

**Electrical Characteristics - Input/Supply/Common Output Parameters**
 $T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = 3.3\text{ V} \pm 5\%$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	$V_{IH}$	3.3V +/-5%	2		$V_{DD} + 0.3$	V	
Input Low Voltage	$V_{IL}$	3.3V +/-5%	$V_{SS} - 0.3$		0.8	V	
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$	-5		5	uA	
Input Low Current	$I_{IL1}$	$V_{IN} = 0\text{ V}$ ; Inputs with no pull-up resistors	-5			uA	
	$I_{IL2}$	$V_{IN} = 0\text{ V}$ ; Inputs with pull-up resistors	-200			uA	
Operating Supply Current	$I_{DD3.3OP}$	Full Active, $C_L = \text{Full load}$ ;		260	350	mA	
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven		0.3	35	mA	
		all differential pairs tri-stated			12	mA	
Input Frequency <sup>3</sup>	$F_i$	$V_{DD} = 3.3\text{ V}$		14.31818		MHz	3
Pin Inductance <sup>1</sup>	$L_{pin}$				7	nH	1
Input Capacitance <sup>1</sup>	$C_{IN}$	Logic Inputs			5	pF	1
	$C_{OUT}$	Output pin capacitance			6	pF	1
	$C_{INX}$	X1 & X2 pins			5	pF	1
Clk Stabilization <sup>1,2</sup>	$T_{STAB}$	From VDD Power-Up or de-assertion of PD# to 1st clock.			1.8	ms	1,2
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		CPU output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	2

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>See timing diagrams for timing requirements.

<sup>3</sup>Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

**Electrical Characteristics - CPU & SRC 0.7V Current Mode Differential Pair**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 2\text{pF}$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	$Z_o^1$	$V_o = V_x$	3000			$\Omega$	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	749	850	mV	1
Voltage Low	VLow		-150	3	150		1
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		756	1150	mV	1
Min Voltage	Vuds		-300	-7			1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300	0	300	ppm	1,2
Average period	Tperiod	200MHz nominal	4.9985	5.0000	5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982	6.0000	6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978	7.5000	7.5023	ns	2
		133.33MHz spread	7.4978		5.4000	ns	2
		100.00MHz nominal	9.9970	10.0000	10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	$T_{absmin}$	200MHz nominal	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	$t_r$	$V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$	175	279	700	ps	1
Fall Time	$t_f$	$V_{OH} = 0.525\text{V}$ , $V_{OL} = 0.175\text{V}$	175	280	700	ps	1
Rise Time Variation	d- $t_r$			30	125	ps	1
Fall Time Variation	d- $t_f$			30	125	ps	1
Duty Cycle	$d_{t3}$	Measurement from differential waveform	45	50.9	55	%	1
Skew	$t_{sk3}$	$V_T = 50\%$		8	100	ps	1
Jitter, Cycle to cycle	$t_{jyc-cyc}$	Measurement from differential waveform		40	125	ps	1

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

**SRC clock outputs run at only 100MHz or 200MHz, specs for 133.33 and 166.66 do not apply to SRC clock pair.**

**Electrical Characteristics - 3V66 Mode: 3V66 [3:0]**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}30\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	$T_{\text{period}}$	66.66MHz output nominal	14.9955		15.0045	ns	2
		66.66MHz output spread	14.9955		15.0799	ns	2
Output High Voltage	$V_{OH}$	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 1\text{ mA}$			0.55	V	
Output High Current	$I_{OH}$	$V_{OH} = 1.0\text{ V}$			-33	mA	
		$V_{OH} = 3.135\text{ V}$	-33			mA	
Output Low Current	$I_{OL}$	$V_{OL} = 1.95\text{ V}$	30			mA	
		$V_{OL} = 0.4\text{ V}$			38	mA	
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Rise Time	$t_{r1}$	$V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$	0.5	1.78	2	ns	1
Fall Time	$t_{f1}$	$V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$	0.5	1.72	2	ns	1
Duty Cycle	$d_{t1}$	$V_T = 1.5\text{ V}$	45	49.9	55	%	1
Skew	$t_{sk1}$	$V_T = 1.5\text{ V}$		80	250	ps	1
Jitter	$t_{j\text{cyc-cyc}}$	$V_T = 1.5\text{ V}$ 3V66		172	250	ps	1

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz
**Electrical Characteristics - PCICLK**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}30\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	$T_{\text{period}}$	33.33MHz output nominal	29.9910		30.0090	ns	2
		33.33MHz output spread	29.9910		30.1598	ns	2
Output High Voltage	$V_{OH}$	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 1\text{ mA}$			0.55	V	
Output High Current	$I_{OH}$	$V_{OH} = 1.0\text{ V}$			-33	mA	
		$V_{OH} = 3.135\text{ V}$	-33			mA	
Output Low Current	$I_{OL}$	$V_{OL} = 1.95\text{ V}$	30			mA	
		$V_{OL} = 0.4\text{ V}$			38	mA	
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Rise Time	$t_{r1}$	$V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$	0.5	1.78	2	ns	1
Fall Time	$t_{f1}$	$V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$	0.5	1.72	2	ns	1
Duty Cycle	$d_{t1}$	$V_T = 1.5\text{ V}$	45	51.2	55	%	1
Skew	$t_{sk1}$	$V_T = 1.5\text{ V}$		59	500	ps	1
Jitter	$t_{j\text{cyc-cyc}}$	$V_T = 1.5\text{ V}$ 3V66		140	250	ps	1

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

**Electrical Characteristics - VCH, USB**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-200		200	ppm	1,2
Clock period	$T_{\text{period}}$	48.008MHz output nominal	20.8257		20.8340	ns	2
Output High Voltage	$V_{OH}$	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 1\text{ mA}$			0.55	V	
Output High Current	$I_{OH}$	$V_{OH} = 1.0\text{ V}$			-29	mA	
		$V_{OH} = 3.135\text{ V}$	-23			mA	
Output Low Current	$I_{OL}$	$V_{OL} = 1.95\text{ V}$	29			mA	
		$V_{OL} = 0.4\text{ V}$			27	mA	
Edge Rate		Rising edge rate	1		2	V/ns	1
Edge Rate		Falling edge rate	1		2	V/ns	1
Rise Time	$t_{r1}$	$V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$	1	1.45	2	ns	1
Fall Time	$t_{f1}$	$V_{OH} = 2.4\text{ V}, V_{OL} = 0.4\text{ V}$	1	1.37	2	ns	1
Duty Cycle	$d_{t1}$	$V_T = 1.5\text{ V}$	45	52.5	55	%	1
Skew	$t_{sk1}$	$V_T = 1.5\text{ V}$			1	ns	1
Long Term Jitter		125us period jitter (8kHz frequency modulation amplitude)		0.628	6	ns	1

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz
**Electrical Characteristics - 48MHz DOT Clock**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 5\text{-}10\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-200		200	ppm	1,2
Clock period	$T_{\text{period}}$	48.008MHz output nominal	20.8257		20.8340	ns	2
Output High Voltage	$V_{OH}$	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 1\text{ mA}$			0.55	V	
Output High Current	$I_{OH}$	$V_{OH} = 1.0\text{ V}$			-29	mA	
		$V_{OH} = 3.135\text{ V}$	-23			mA	
Output Low Current	$I_{OL}$	$V_{OL} = 1.95\text{ V}$	29			mA	
		$V_{OL} = 0.4\text{ V}$			27	mA	
Edge Rate		Rising edge rate	2		4	V/ns	1
Edge Rate		Falling edge rate	2		4	V/ns	1
Rise Time	$t_{r1}$	$V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$	0.5	0.87	1	ns	1
Fall Time	$t_{f1}$	$V_{OH} = 2.4\text{ V}, V_{OL} = 0.4\text{ V}$	0.5	0.89	1	ns	1
Duty Cycle	$d_{t1}$	$V_T = 1.5\text{ V}$	45	52.3	55	%	1
Skew	$t_{sk1}$	$V_T = 1.5\text{ V}$			1	ns	1
Long Term Jitter		125us period jitter (8kHz frequency modulation amplitude)		0.636	2	ns	1

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz


**Electrical Characteristics - REF-14.318MHz**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1
Clock period	$T_{\text{period}}$	14.318 MHz output nominal	69.8270		69.8550	ns	
Output High Voltage	$V_{OH}^1$	$I_{OH} = -1\text{ mA}$	2.4			V	
Output Low Voltage	$V_{OL}^1$	$I_{OL} = 1\text{ mA}$			0.4	V	
Output High Current	$I_{OH}$	$V_{OH} = 1.0\text{ V}$			-33	mA	
		$V_{OH} = 3.135\text{ V}$	-33			mA	
Output Low Current	$I_{OL}$	$V_{OL} = 1.95\text{ V}$	30			mA	
		$V_{OL} = 0.4\text{ V}$			38	mA	
Rise Time	$t_{r1}^1$	$V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$	0.5	1.93	2	ns	1
Fall Time	$t_{f1}^1$	$V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$	0.5	1.92	2	ns	1
Skew	$t_{sk1}^1$	$V_T = 1.5\text{ V}$		14	500	ps	1
Duty Cycle	$d_{11}^1$	$V_T = 1.5\text{ V}$	45	53.8	55	%	1
Jitter	$t_{\text{cyc-cyc}}^1$	$V_T = 1.5\text{ V}$		400	1000	ps	1

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Group to Group Skews at Common Transition Edges**

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66 to PCI	$S_{3V66\text{-PCI}}$	3V66 (4:0) leads 33MHz PCI	1.50	2.0	3.50	ns
DOT-USB	$S_{\text{DOT\_USB}}$	180 degrees out of phase	0.00		1.00	ns
DOT-VCH	$S_{\text{DOT\_VCH}}$	in phase	0.00		1.00	ns




**I<sup>2</sup>C Table: Read-Back Register**

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RESERVED	RESERVED	-	RESERVED		X
Bit 6	-	RESERVED		-	RESERVED		X
Bit 5	-	RESERVED		-	RESERVED		X
Bit 4	-	RESERVED		R	RESERVED		X
Bit 3	-	RESERVED		R	RESERVED		X
Bit 2	-	RESERVED		R	RESERVED		X
Bit 1	-	FSA	Freq Select 1 Read Back	R	READBACK of CPU(2:0) Frequency		X
Bit 0	-	FSA	Freq Select 0 Read Back	R			X

**I<sup>2</sup>C Table: Spreading and Device Behavior Control Register**

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		SRC/SRC#	SRC Free-Running Control	RW	FREE-RUN	STOPPABLE	0
Bit 6		SRC	Output Control	RW	Disable	Enable	1
Bit 5		RESERVED		R	RESERVED		X
Bit 4		RESERVED		R	RESERVED		X
Bit 3		RESERVED		R	RESERVED		X
Bit 2		RESERVED		R	RESERVED		X
Bit 1		CPUT1/CPUC1	Output Control	RW	Disable	Enable	1
Bit 0		CPUT0/CPUC0	Output Enable	RW	Disable	Enable	1

**I<sup>2</sup>C Table: Output Control Register**

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		SRC_PD# Drive Mode	0: Driven in PD#	RW	Driven	Hi-Z	0
Bit 6		SRC_Stop# Drive Mode	0: Driven in PCI_Stop#	RW	Driven	Hi-Z	0
Bit 5		RESERVED	RESERVED	-	RESERVED		X
Bit 4		CPUT1_PD# Drive Mode	0: driven in PD#	RW	Driven	Hi-Z	0
Bit 3		CPUT0_PD# Drive Mode	1: Tri-stated	RW	Driven	Hi-Z	0
Bit 2		RESERVED	RESERVED	-	RESERVED		X
Bit 1		RESERVED	RESERVED	-	RESERVED		X
Bit 0		RESERVED	RESERVED	-	RESERVED		X

**I<sup>2</sup>C Table: Output Control Register**

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		PCI_Stop#	PCI_Stop# Control 0: all stoppable PCI are stopped	RW	Enable	Disable	1
Bit 6		RESERVED	RESERVED	-	RESERVED		X
Bit 5		PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4		PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3		PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2		PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1		PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0		PCICLK0	Output Control	RW	Disable	Enable	1


**I<sup>2</sup>C Table: Output Control Register**

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		48MHz_USB 2x output drive	0=2x drive	RW	2x drive	1xdrive	1
Bit 6		48MHz_USB	Output Control	RW	Disable	Enable	1
Bit 5		RESERVED	RESERVED	-	RESERVED		X
Bit 4		RESERVED	RESERVED	-	RESERVED		X
Bit 3		RESERVED	RESERVED	-	RESERVED		X
Bit 2		PCICLK_F2	Output Control	RW	stoppable	Free-run	1
Bit 1		PCICLK_F1	Output Control	RW	stoppable	Free-run	1
Bit 0		PCICLK_F0	Output Control	RW	stoppable	Free-run	1

**I<sup>2</sup>C Table: Output Control Register**

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		DOT_48MHZ	Output Control	RW	Disable	Enable	1
Bit 6		CPU_T/C_ITP	Output Control	RW	Disable	Enable	1
Bit 5		3V66_3/VCH Frequency Select	Output Select	RW	3V66	VCH	0
Bit 4		3V66_3/VCH Frequency Select	Output Control	RW	Disable	Enable	1
Bit 3		RESERVED	RESERVED	-	RESERVED		X
Bit 2		3V66_2	Output Control	RW	Disable	Enable	1
Bit 1		3V66_1	Output Control	RW	Disable	Enable	1
Bit 0		3V66_0	Output Control	RW	Disable	Enable	1

**I<sup>2</sup>C Table: Output Control and Fix Frequency Register**

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Test Clock Mode	Test Clock Mode	-	Disable	Enable	0
Bit 6		RESERVED	-	-	-	-	0
Bit 5		CPU *2 Test Clock	FS_A and FS_B Operation	-	Normal	Test Mode	0
Bit 4		SRC Frequency Select	SRC Frequency Select	-	100MHz	200MHz	0
Bit 3		Spread Spectrum Type	Down/Center	-	Down	Center	0
Bit 2		Spread Spectrum Mode	Spread Spectrum Enable		Spread OFF	Spread ON	0
Bit 1		REF1	Output Control	RW	Disable	Enable	1
Bit 0		REF0	Output Control	RW	Disable	Enable	1

**I<sup>2</sup>C Table: Vendor & Revision ID Register**

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1


**I<sup>2</sup>C Table: Byte Count Register**

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 08 = 8 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	0
Bit 1	-	BC1		RW	-	-	0
Bit 0	-	BC0		RW	-	-	0

**PD#, Power Down**

PD# is an asynchronous active low input used to shut off all clocks cleanly prior to clock power. When PD# is asserted low all clocks will be driven low before turning off the VCO. In PD# de-assertion all clocks will start without glitches.

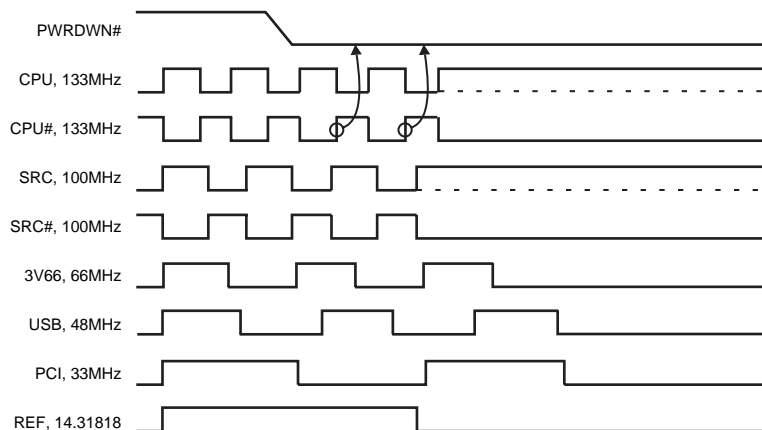
PWRDWN#	CPU	CPU #	SRC	SRC#	3V66	PCIF/PCI	USB/DOT	REF	Note
1	Normal	Normal	Normal	Normal	66MHz	33MHz	48MHz	14.318MHz	
0	Iref * 2 or Float	Float	Iref * 2 or Float	Float	Low	Low	Low	Low	

## Notes:

1. Refer to tristate control of CPU and SRC clocks in section 7.7 for tristate timing and operation.
2. Refer to Control Registers in section 16 for CPU\_Stop, SRC\_Stop and PwrDwn SMBus tristate control addresses.

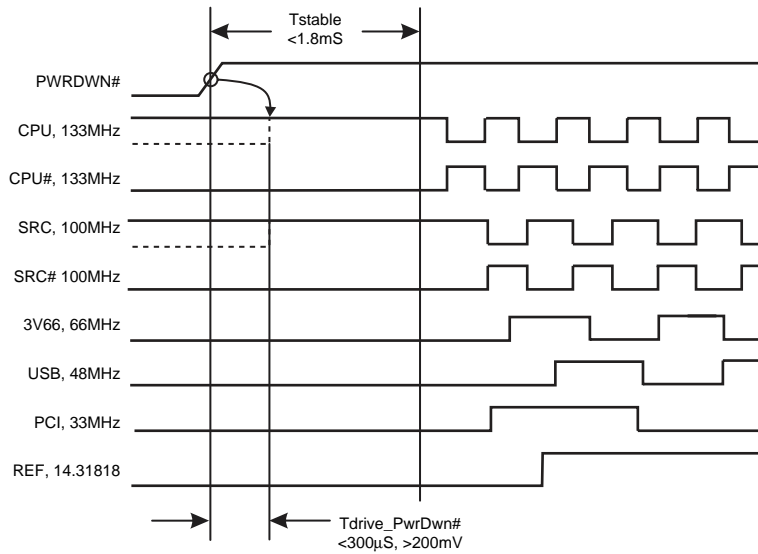
**PD# Assertion**

PD# should be sampled low by 2 consecutive CPU# rising edges before stopping clocks. All single ended clocks will be held low on their next high to low transition. All differential clocks will be held high on the next high to low transition of the complimentary clock. If the control register determining to drive mode is set to 'tri-state', the differential pair will be stopped in tri-state mode, undriven. When the drive mode but corresponding to the CPU or SRC clock of interest is set to '0' the true clock will be driven high at  $2 \times I_{ref}$  and the complementary clock will be tristated. If the control register is programmed to '1' both clocks will be tristated.



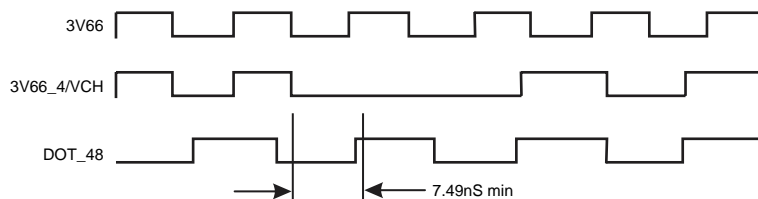
### PD# De-assertion

The time from the de-assertion of PD# or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD# tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µs of PD# deassertion.



### 3V66\_3/VCH Pin Functionality

The 3V66\_4/VCH pin can be configured to be a 66.66MHz modulated output or a non-spread 48MHz output. The default is 3V66 clock. The switching is controlled by Byte 5 Bit 5. If it is set to '1' this pin will output the 48MHz VCH clock. The output will go low on the falling edge of 3V66 for a minimum of 7.49ns. Then the output will transition to 48MHz on the next rising edge of DOT\_48 clock.

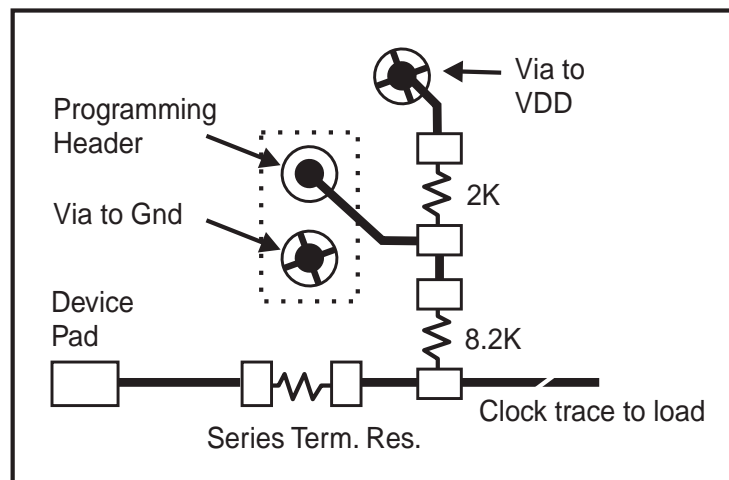


## Shared Pin Operation - Input/Output Pins

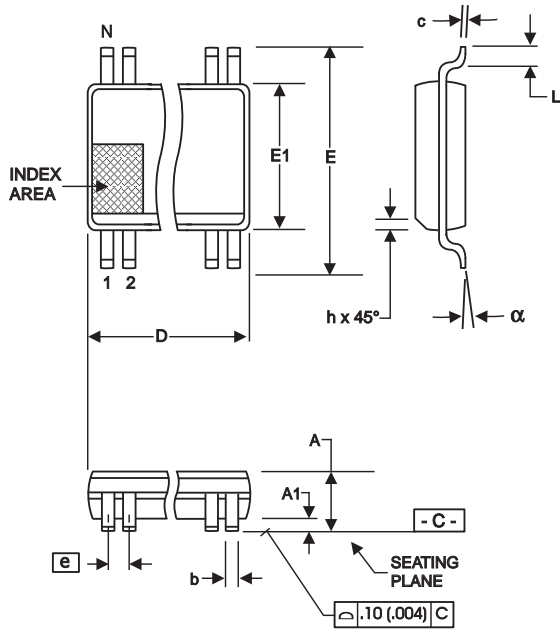
The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.



**Fig. 1**



SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
alpha	0°	8°	0°	8°

**VARIATIONS**

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

**Ordering Information**

**ICS952621yFLF-T**

Example:

**ICS XXXX y F LF-T**

