



Dual 1-to-8 Low Voltage Clock Buffer/Translator

Description

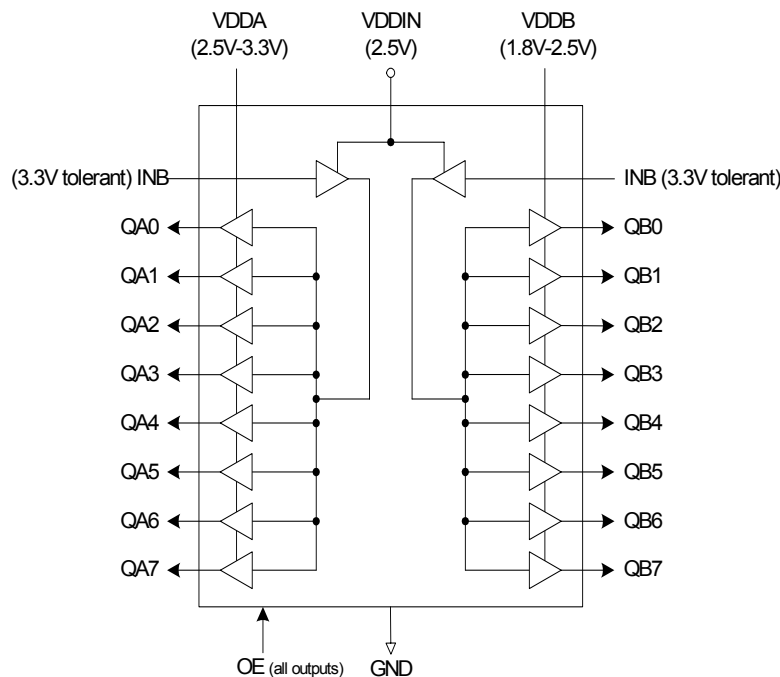
The ICSLV218 is a high-speed clock buffer consisting of two independent single-input to eight-output low-skew, non-inverting clock drivers.

The ICSLV218 has three independent supply rails: The input supply rail, VDDIN, operates from a fixed 2.5 V supply, while the output supply rails, VDDA and VDDB, operate from 2.5 V-3.3 V and 1.8 V-2.5 V supplies respectively. This configuration, combined with 3.3 V tolerance on the INA and INB inputs, allows for many different possibilities of up and/or down voltage translation.

Features

- Dual 1:8 clock drivers
- Pin-compatible with MK74CB218
- Independent supply rails on input and output banks for voltage translation
- 3.3 V input tolerance
- Low skew outputs within same bank (150 ps)
- Output Enable tri-states both banks of eight
- Clock speeds up to 200 MHz
- Industrial temperature range (-40 to 85°C)
- 28-pin SSOP (150 mil body) Pb (lead) free package

Block Diagram

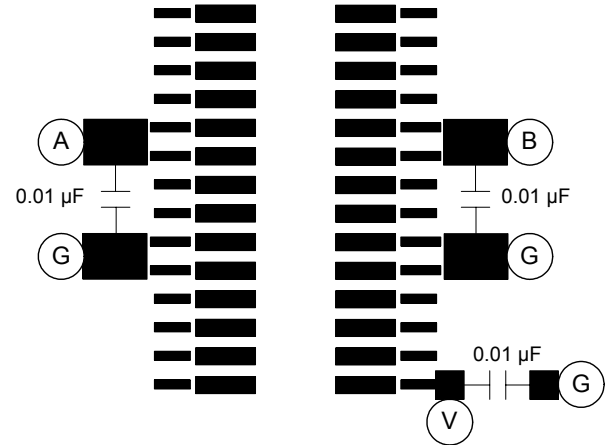




Pin Assignment

INA	1	28	INB
QA0	2	27	QB0
QA1	3	26	QB1
QA2	4	25	QB2
VDDA	5	24	VDDB
VDDA	6	23	VDDB
QA3	7	22	QB3
QA4	8	21	QB4
GND	9	20	GND
GND	10	19	GND
QA5	11	18	QB5
QA6	12	17	QB6
QA7	13	16	QB7
OE	14	15	VDD

Suggested Layout



NOTE: 33 ohm series termination resistors for each output are essential for operation.

For simplicity, series termination resistors are not shown for the outputs, but should be placed as close to the device as possible. It is most critical to have the 0.01 μF decoupling capacitors closest.

(A) = connect to VDDA

(B) = connect to VDDB

(V) = connect to VDD

(G) = connect to low inductance ground plane

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	INA	Input	Clock input for eight A outputs. 3.3 V tolerant.
2, 3, 4	QA0, QA1, QA2	Output	Clock A outputs.
5, 6	VDDA	Power	Power supply for QA outputs. Connect to a voltage from 2.5 V to 3.3 V.
7, 8	QA3, QA4	Output	Clock A outputs.
9, 10	GND	Power	Connect to ground.
11, 12, 13	QA5, QA6, QA7	Output	Clock A outputs.
14	OE	Input	Output Enable. Tri-states all clock outputs when this input is low. Internal pull-up to VDDIN.
15	VDD	Power	Power supply for inputs. Connect to 2.5 V.
16, 17, 18	QB7, QB6, QB5	Output	Clock B outputs.
19, 20	GND	Power	Connect to ground.
21, 22	QB4, QB3	Output	Clock B outputs.
23, 24	VDDB	Power	Power supply for QB outputs. Connect to a voltage from 1.8 V to 2.5 V.
25, 26, 27	QB2, QB1, QB0	Output	Clock B outputs.
28	INB	Input	Clock input for eight B outputs. 3.3 V tolerant.



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICSLV218. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltages, VDDIN, VDDA, or VDDB (referenced to GND)	5 V
Inputs INA and INB (referenced to GND)	-0.5 V to 3.6 V
Outputs	-0.5 V to VDDA+0.5 V or VDDB+0.5 V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65°C to 150°C
Soldering Temperature	260°C (max. of 20 seconds)



DC Electrical Characteristics

Unless stated otherwise, $V_{DDIN} = V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 10\%$, Ambient Temperature = -40 to 85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	V _{DDIN}		2.375	2.5	2.75	V
	V _{DDA}		2.375		3.63	V
	V _{DDB}		1.62		2.75	V
Operating Supply Current	I _{DDIN}	All outputs at 100 MHz, No load		25		μA
	I _{DDA}	All outputs at 100 MHz, No load		17		mA
	I _{DDB}	All outputs at 100 MHz, No load		17		mA
Input High Voltage	V _{IH}	INA, INB, OE pins	1.7			V
Input Low Voltage	V _{IL}	INA, INB, OE pins			0.7	V
Output High Voltage, QA0-QA7	V _{OH}	V _{DDA} =3.3 V, I _{OH} = -25 mA	2.0			V
		V _{DDA} =2.5 V, I _{OH} = -16 mA	2.0			V
Output Low Voltage, QA0-QA7	V _{OL}	I _{OL} = 25 mA			0.4	V
		V _{DDA} =2.5 V, I _{OL} = 16 mA			0.4	V
Output High Voltage, QB0-QB7	V _{OH}	V _{DDB} = 2.5 V, I _{OH} = -16 mA	2			V
		V _{DDB} = 1.8 V, I _{OH} = -8 mA	V _{DD} -0.45			V
Output Low Voltage, QB0-QB7	V _{OL}	V _{DDB} = 2.5 V, I _{OL} = 16 mA			0.4	V
		V _{DDB} = 1.8 V, I _{OL} = 8 mA			0.45	V
Output Impedance				15		Ω
Short Circuit Current		Each output, V _{OUT} =GND or V _{DD}		±100		mA
Input Capacitance	C _{IN}			7		pF
On-chip Pull-up Resistor	R _{PU}	OE		250		kΩ

Note: Short circuits may be applied indefinitely, but only one output may be shorted at a time to prevent exceeding the power dissipation rating of this package.



AC Electrical Characteristics

Unless stated otherwise, $V_{DDIN} = V_{DDA} = V_{ddb} = 2.5\text{ V} \pm 10\%$, Ambient Temperature = -40 to 85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency	F_{IN}	INA or INB, Note 3	0		200	MHz
Propagation Delay, INA to QA0-QA7		$C_L = 10\text{ pF}$			5	ns
Propagation Delay, INB to QB0-QB7		$C_L = 10\text{ pF}$			5	ns
Output Clock Rise Time		20% to 80%, $C_L = 10\text{ pF}$			2.5	ns
Output Clock Fall Time		80% to 20%, $C_L = 10\text{ pF}$			2.5	ns
Output Duty Cycle		$C_L = 10\text{ pF}$	45	48	55	%
Output to Output Skew		Measured on rising edge at $V_{DD}/2$, Note 1		100	150	ps
Output Clock A to B Skew		At $V_{DD}/2$, Note 2			1500	ps
Output Enable Time		OE high to output on			20	ns
Output Disable Time		OE low to tri-state			20	ns

Notes:

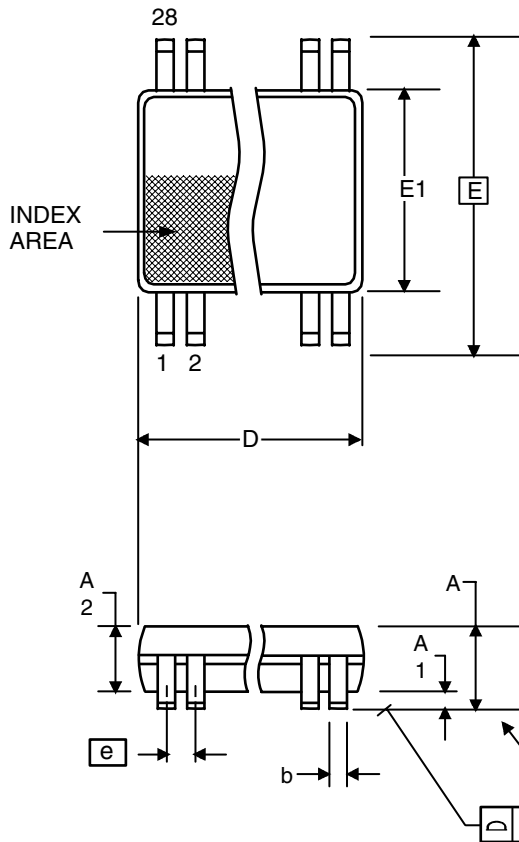
- Between any two A outputs, or any two B outputs, with equal loading.
- Between any clock A output and any clock B output with INA connected to INB, and equal loading.
- Care must be taken not to exceed the absolute maximum junction temperature or power dissipation rating of the package: Power dissipated = $(16\text{ outputs} \times \text{frequency} \times V_{DD}^2 \times C_L) < [(T_j - T_a) / \theta_{JA}]$.

Thermal Characteristics

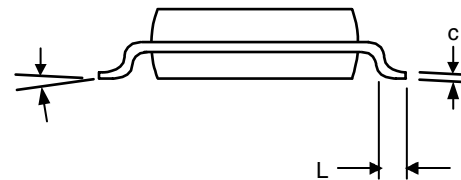
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		100		$^\circ\text{C/W}$
	θ_{JA}	1 m/s air flow		80		$^\circ\text{C/W}$
	θ_{JA}	3 m/s air flow		67		$^\circ\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}			60		$^\circ\text{C/W}$

**Package Outline and Package Dimensions (28-pin SSOP, 150 mil Body)**

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	.008	.012
C	0.18	0.25	.007	.010
D	9.80	10.00	.386	.394
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

**Ordering Information**

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICSLV218RILF	ICSLV218RILF	Tubes	28-pin SSOP	-40 to +85°C
ICSLV218RILFT	ICSLV218RILF	Tape and Reel	28-pin SSOP	-40 to +85°C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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