



### 14-Bit Configurable Registered Buffer for DDR2

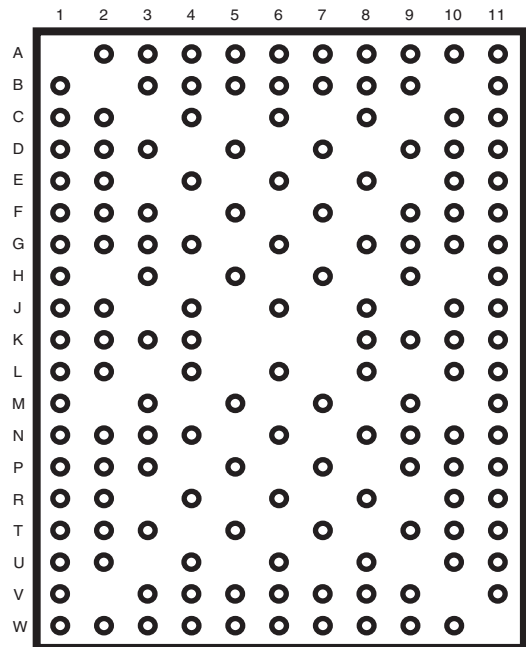
#### Recommended Application:

- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS97U877
- Ideal for DDR2 400, 533 and 667

#### Product Features:

- 14-bit 1:2 registered buffer with parity check functionality
- Supports SSTL\_18 JEDEC specification on data inputs and outputs
- 50% more dynamic driver strength than standard SSTU32864
- Supports LVCMOS switching levels on C1 and RESET# inputs
- Low voltage operation  
V<sub>DD</sub> = 1.7V to 1.9V
- Available in 150 BGA package
- Green packages available

#### Pin Configuration



**150 Ball BGA  
(Top View)**

#### Functionality Truth Table

| Inputs |                  |                  |                  |                  |                      | Outputs        |                |                |
|--------|------------------|------------------|------------------|------------------|----------------------|----------------|----------------|----------------|
| RESET# | DCS#             | CSR#             | CK               | CK#              | Dn,<br>DODT,<br>DCKE | Qn             | QCS#           | QODT,<br>QCKE  |
| H      | L                | L                | ↑                | ↓                | L                    | L              | L              | L              |
| H      | L                | L                | ↑                | ↓                | H                    | H              | L              | H              |
| H      | L                | L                | L or H           | L or H           | X                    | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| H      | L                | H                | ↑                | ↓                | L                    | L              | L              | L              |
| H      | L                | H                | ↑                | ↓                | H                    | H              | L              | H              |
| H      | L                | H                | L or H           | L or H           | X                    | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| H      | H                | L                | ↑                | ↓                | L                    | L              | H              | L              |
| H      | H                | L                | ↑                | ↓                | H                    | H              | H              | H              |
| H      | H                | L                | L or H           | L or H           | X                    | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| H      | H                | H                | ↑                | ↓                | L                    | Q <sub>0</sub> | H              | L              |
| H      | H                | H                | ↑                | ↓                | H                    | Q <sub>0</sub> | H              | H              |
| H      | H                | H                | L or H           | L or H           | X                    | Q <sub>0</sub> | Q <sub>0</sub> | Q <sub>0</sub> |
| L      | X or<br>floating | X or<br>floating | X or<br>floating | X or<br>floating | X or<br>floating     | L              | L              | L              |



# ICSSSTUA32S869B

## Advance Information

### Ball Assignments

|   | 1        | 2   | 3                  | 4      | 5    | 6      | 7   | 8    | 9                  | 10  | 11    |
|---|----------|-----|--------------------|--------|------|--------|-----|------|--------------------|-----|-------|
| A | NB       | VDD | MCL <sup>(1)</sup> | NC     | GND  | VREF   | GND | NC   | MCL <sup>(1)</sup> | VDD | NC    |
| B | VDD      | NB  | VDD                | GND    | GND  | GND    | GND | GND  | VDD                | NB  | VDD   |
| C | QCKEA    | VDD | NB                 | GND    | NB   | GND    | NB  | GND  | NB                 | VDD | QCKEB |
| D | Q2A      | VDD | GND                | NB     | DCKE | NB     | D2  | NB   | GND                | VDD | Q2B   |
| E | Q3A      | VDD | NB                 | D3     | NB   | NC     | NB  | DODT | NB                 | NC  | Q3B   |
| F | QODTA    | VDD | GND                | NB     | NC   | NB     | NC  | NB   | GND                | VDD | QODTB |
| G | Q5A      | VDD | GND                | D5     | NB   | CLK    | NB  | D6   | GND                | VDD | Q5B   |
| H | Q6A      | NB  | GND                | NB     | NC   | NB     | NC  | NB   | GND                | NB  | Q6B   |
| J | QCSA#    | VDD | NB                 | NC     | NB   | RESET# | NB  | CSR# | NB                 | VDD | QCSB# |
| K | VDD      | VDD | GND                | GND    | NB   | NB     | NB  | GND  | VDD                | VDD | VDD   |
| L | Q8A      | VDD | NB                 | DCS#   | NB   | CLK#   | NB  | D8   | NB                 | VDD | Q8B   |
| M | Q9A      | NB  | GND                | NB     | NC   | NB     | NC  | NB   | GND                | NB  | Q9B   |
| N | Q10A     | VDD | GND                | D9     | NB   | NC     | NB  | D10  | GND                | VDD | Q10B  |
| P | Q11A     | VDD | GND                | NB     | NC   | NB     | NC  | NB   | GND                | VDD | Q11B  |
| R | Q12A     | C1  | NB                 | D11    | NB   | NC     | NB  | D12  | NB                 | VDD | Q12B  |
| T | Q13A     | VDD | GND                | NB     | D13  | NB     | D14 | NB   | GND                | VDD | Q13B  |
| U | Q14A     | VDD | NB                 | GND    | NB   | GND    | NB  | GND  | NB                 | VDD | Q14B  |
| V | VDD      | NB  | VDD                | GND    | GND  | GND    | GND | GND  | VDD                | NB  | VDD   |
| W | PTYERR1# | VDD | MCL <sup>(1)</sup> | PARIN1 | GND  | VREF   | GND | PPO1 | MCL <sup>(1)</sup> | VDD | NB    |

Note: NC denotes a no-connect (ball present but not connected to the die). NB indicates no ball is populated at that gridpoint.



### Parity and Standby Function Table

| Inputs |                  |                  |                  |                  |  |                       | Output              |                         |  |
|--------|------------------|------------------|------------------|------------------|--|-----------------------|---------------------|-------------------------|--|
| RESET# | DCS#             | CSR#             | CK               | CK#              | £ of inputs = H<br>D1...D14 <sup>(1)</sup> | PARIN1 <sup>(2)</sup> | PPO1 <sup>(2)</sup> | PTYERR1# <sup>(3)</sup> |  |
| H      | L                | X                | ↑                | ↓                | Even                                       | L                     | L                   | H                       |  |
| H      | L                | X                | ↑                | ↓                | Odd  | L                     | H                   | L                       |  |
| H      | L                | X                | ↑                | ↓                | Even                                       | H                     | H                   | L                       |  |
| H      | L                | X                | ↑                | ↓                | Odd  | H                     | L                   | H                       |  |
| H      | L                | L                | ↑                | ↓                | Even                                       | L                     | L                   | H                       |  |
| H      | L                | L                | ↑                | ↓                | Odd  | L                     | H                   | L                       |  |
| H      | L                | L                | ↑                | ↓                | Even                                       | H                     | H                   | L                       |  |
| H      | L                | L                | ↑                | ↓                | Odd  | H                     | L                   | H                       |  |
| H      | H                | H                | ↑                | ↓                | X  | X                     | PPO <sub>n0</sub>   | PTYERR <sub>n0</sub> #  |  |
| H      | X                | X                | L or H           | L or H           | X  | X                     | PPO <sub>n0</sub>   | PTYERR <sub>n0</sub> #  |  |
| L      | X or<br>floating | X or<br>floating | X or<br>floating | X or<br>floating | X or<br>floating                           | X or<br>floating      | L                   | H                       |  |

NOTE 1 Inputs D1, D4 and D4 are not included in this range.

NOTE 2 PARIN1 arrives one (C1 = 0) or two (C = 1) clock cycles after data to which it applies.

NOTE 3 This transition assumes PTYERR1# is high at the crossing of CK going high and CK# going low.

If PTYERR1# is low, it stays latched low for two clock cycles or until RESET# is driven low. PARIN1 is used to generate PPO1 and PTYERR1#.



# ICSSSTUA32S869B Advance Information

## General Description

The **ICSSSTUA32S869B** is 14-bit 1:2 registered buffer with parity is designed for 1.7 V to 1.9 V VDD operation. All clock and data inputs are compatible with the JEDEC standard for SSTL\_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers optimized to drive the DDR2 DIMM load. They provide 50% more dynamic driver strength than the standard SSTU32864 outputs.

The **ICSSSTUA32S869B** operates from a differential clock (CK and CK). Data are registered at the crossing of CK going high, and CK going low.

The device supports low-power standby operation. When the reset input (RESET) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when RESET is low all registers are reset, and all outputs except PTYERR1# are forced low. The LVCMOS RESET input must always be held at a valid logic high or low level.

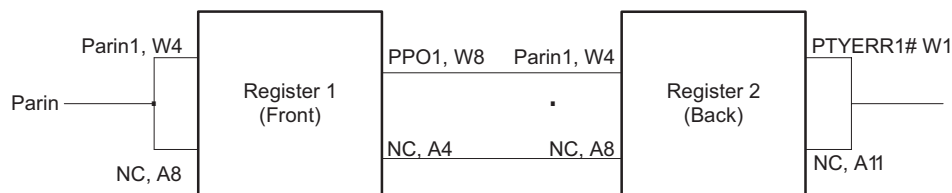
To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

In the DDR2 RDIMM application, RESET is specified to be completely asynchronous with respect to CK and CK. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. **ICSSSTUA32S869B** must ensure that the outputs remain low as long as the data inputs are low, the clock is stable during the time from the low-to-high transition of RESET and the input receivers are fully enabled. This will ensure that there are no glitches on the output.

The device monitors both DCS and CSR inputs and will gate the Qn, PPO1 (Parital-Parity-Out) and PTYERR1# (Parity Error) Parity outputs from changing states when both DCS and CSR are high. If either DCS or CSR input is low, the Qn, PPO1 and PTYERR1# outputs will function normally. The RESET input has priority over the DCS and CSR controls and will force the Qn and PPO outputs low and the PTYERR1# high.

The **ICSSSTUA32S869B** includes a parity checking function. The **ICSSSTUA32S869B** accepts a parity bit from the memory controller at its input pin PARIN1 one or two cycles after the corresponding data input, compares it with the data received on the D-inputs and indicates on its opendrain PTYERR1 pin (active low) whether a parity error has occurred. The number of cycles depends on the setting of C1, see Figure 6 and 7.

When used as a single device, the C1 input is tied low. When used in pairs, the C1 inputs is tied low for the first register (front) and the C1 input is tied high for the second register. When used as a single register, the PPO1 and PTYERR1# signals are produced two clock cycles after the corresponding data input. When used in pairs, the PTYERR1# signals of the first register are left floating. The PPO1 outputs of the first register are cascaded to the PARIN1 signals on the second register (back). The PPO1 and PTYERR1# signals of the second register are produced three clock cycles after the corresponding data input. Parity implementation and device wiring for single and dual die is described in Figure 1. If an error occurs, and the PTYERR1# is driven low, it stays low for two clock cycles or until RESET is driven low. The DIMM-dependent signals (DCKE, DCS, CSR and DODT) are not included in the parity check computations. All registers used on an individual DIMM must be of the same configuration, i.e single or dual die.



Set C1 = 0 for Register 1; Set C1 = 1 for Register 2. NC denotes No Connect.

**Figure 1 — Parity implementation and device wiring for SSTU32S869 and SSTU32D869**



### Terminal Functions

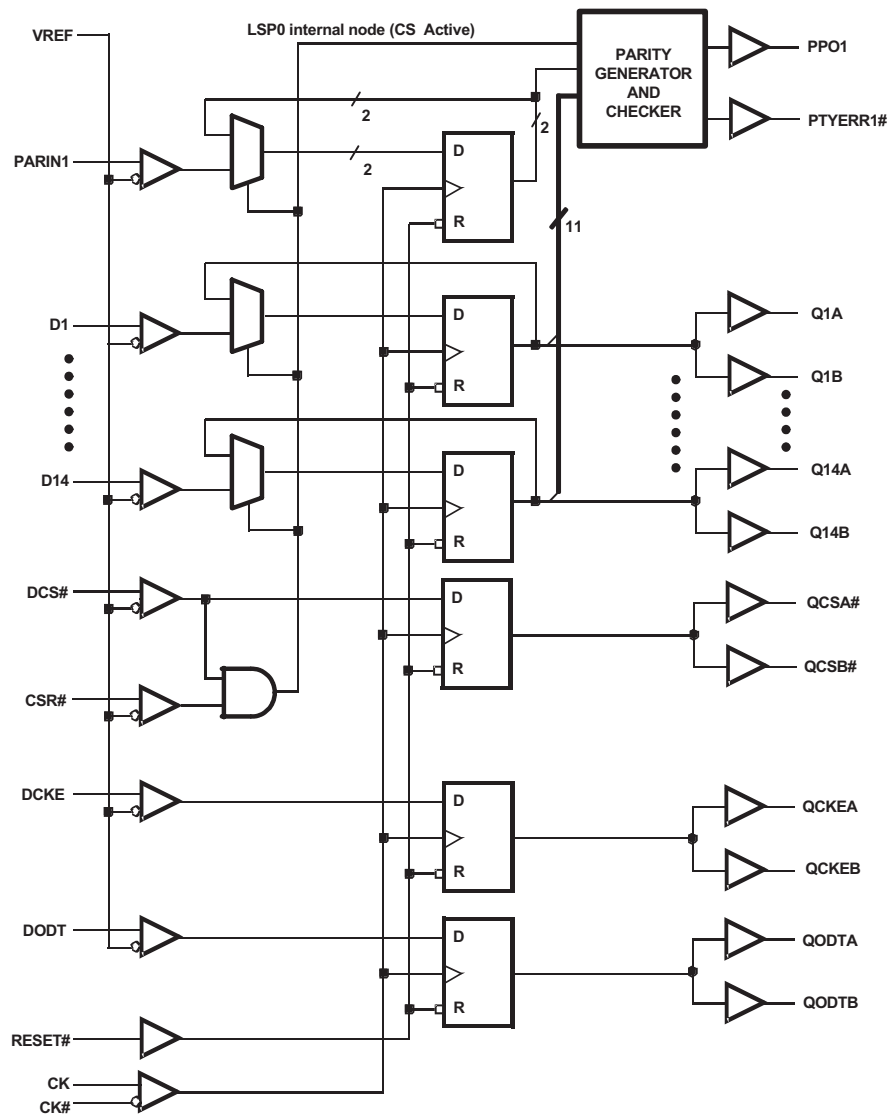
| Signal Group             | Signal Name  | Type            | Description   |
|--------------------------|--|-----------------|---|
| Ungated inputs           | DCKE, DODT   | SSTL_18         | DRAM function pins not associated with Chip Select.   |
| Chip Select gated inputs | D1 ... D14 <sup>(1)</sup>  | SSTL_18         | DRAM inputs, re-driven only when Chip Select is LOW.  |
| Chip Select inputs       | DCS#, CSR#   | SSTL_18         | DRAM Chip Select signals. This pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present.  |
| Re-driven outputs        | Q1A...Q14A,<br>Q1B ... Q14B,<br>QCSA#, QCSB#<br>QCKEA, QCKEB<br>QODTA, QODTB | SSTL_18         | Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.  |
| Parity input             | PARIN1   | SSTL_18         | Inout parity is received on pin PARIN1 and should maintain parity across the D1...D14 <sup>(1)</sup> inputs, at the rising edge of the clock, one cycle after Chip Select is LOW.   |
| Parity output            | PPO1   | SSTL_18         | Partial Parity Output. Indicates parity out of D1-D14 <sup>(1)</sup>  |
| Parity error output      | PTYERR1#   | Open drain      | When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. PTYERR1# will be active for two clock cycles, and delayed by in total 2 clock cycles for compatibility with final parity out timing on the industry-standard DDR2 register with parity (in JEDEC definition). |
| Configuration Inputs     | C1   | 1.8V<br>LVCMOS  | When Low, register is configured as Register 1. When High, register is configured as Register 2.  |
| Clock inputs             | CK, CK#  | SSTL_18         | Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).  |
| Miscellaneous inputs     | RESET#   | 1.8 V<br>LVCMOS | Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. RESET# also resets the PTYERR# signal.  |
|                          | VREF   | 0.9 V nominal   | Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.   |
|                          | VDD  | Power Input     | Power supply voltage  |
|                          | GND  | Ground Input    | Ground  |

NOTE 1 Inputs D1, D4 and D7 and their corresponding outputs Qn are not included in this range.



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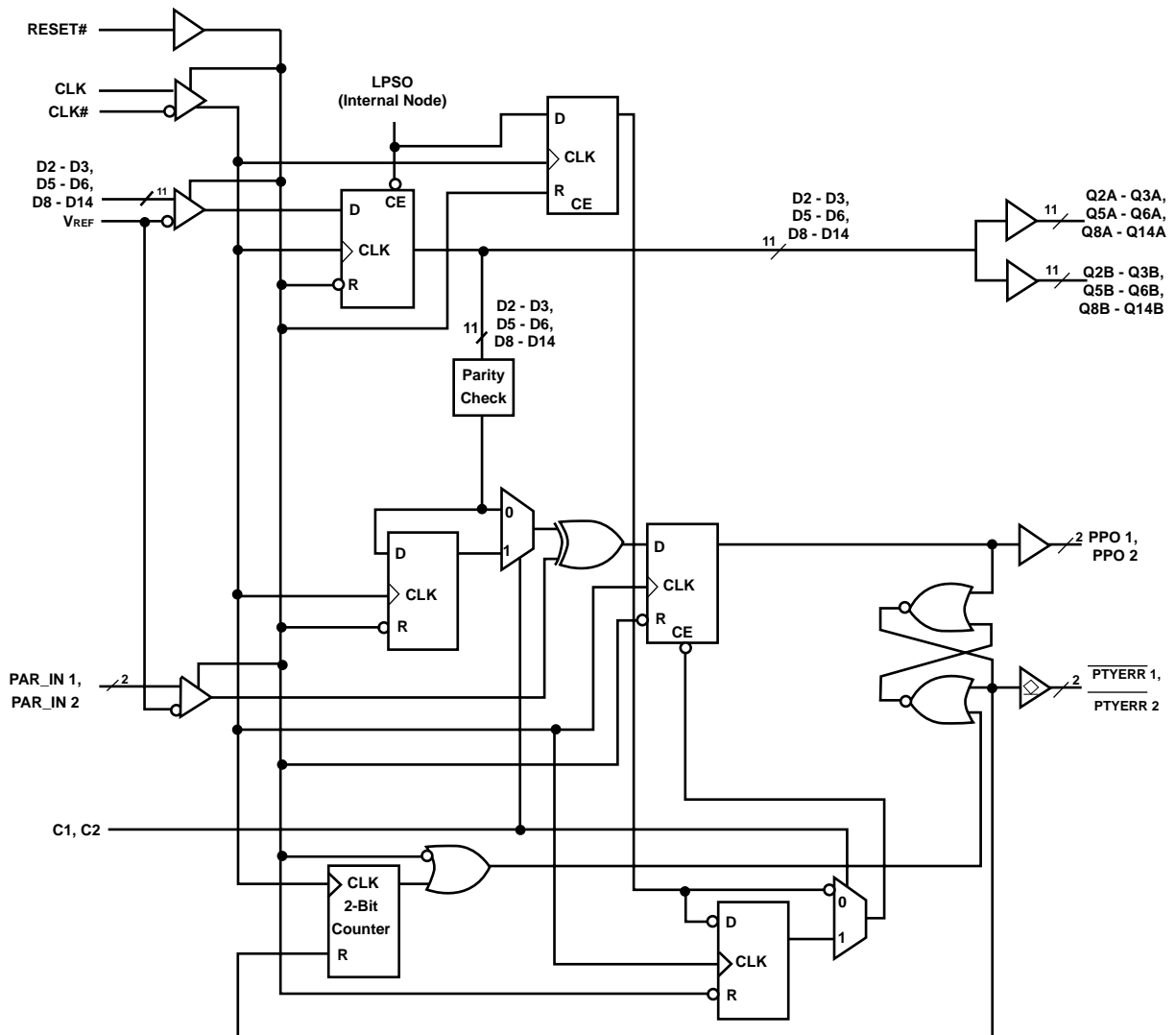
## Block Diagram





# ICSSSTUA32S869B Advance Information

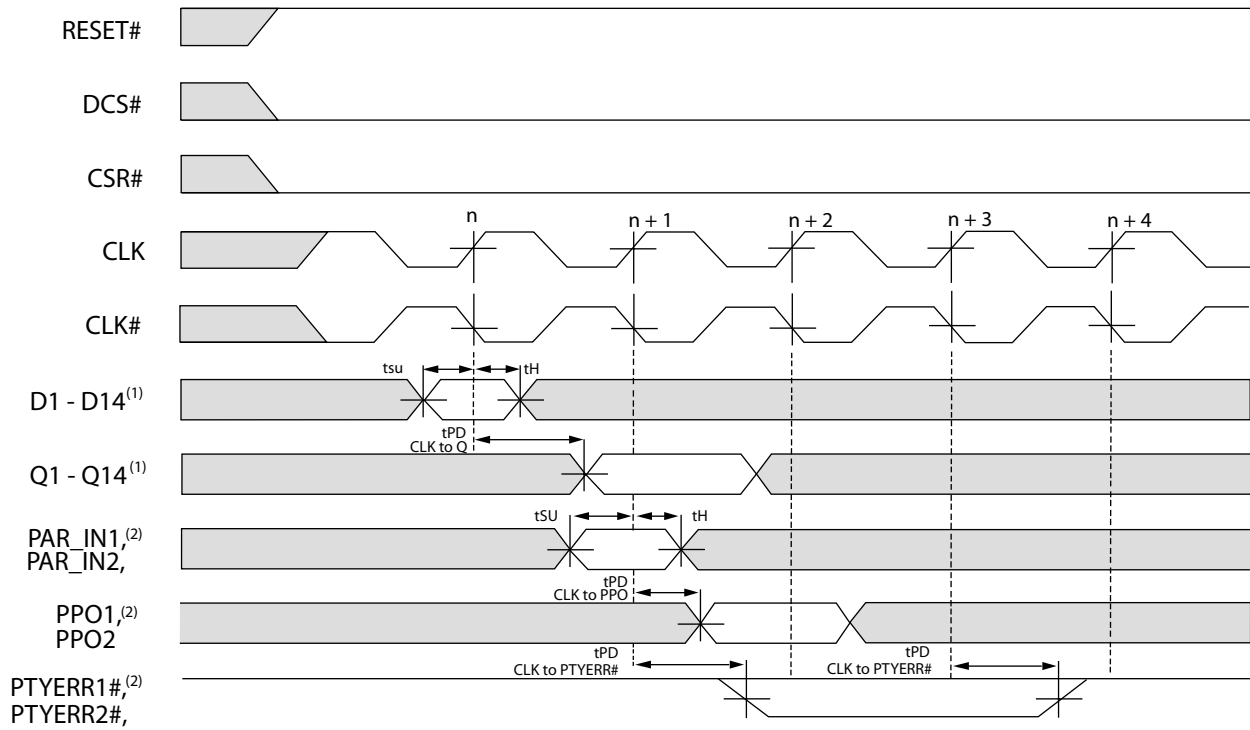
## Block Diagram



NOTE 2 PARIN 1 is used to generate PPO1 and PTYERR1#.



### Register Timing

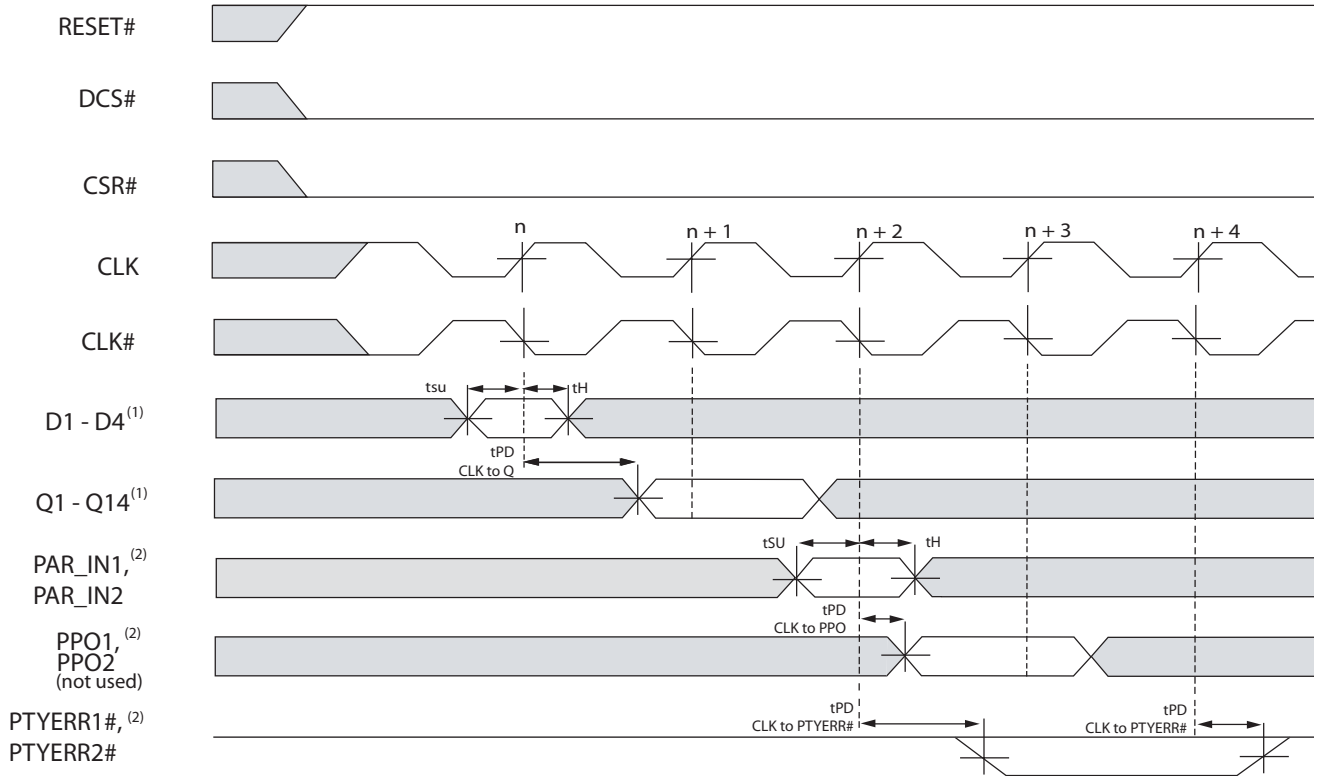


Note 1 This range doesn't include D1, D4 and D7 and their corresponding outputs





### Register Timing



Note 1: This range doesn't include D1, D4 and D7 and their corresponding outputs



### Absolute Maximum Ratings

|  |                    |
|--|--------------------|
| Storage Temperature                    | -65°C to +150°C    |
| Supply Voltage                         | -0.5 to 2.5V       |
| Input Voltage <sup>1</sup>             | -0.5 to VDD + 2.5V |
| Output Voltage <sup>1,2</sup>          | -0.5 to VDDQ + 0.5 |
| Input Clamp Current                    | ±50 mA             |
| Output Clamp Current                   | ±50mA              |
| Continuous Output Current              | ±50mA              |
| VDDQ or GND Current/Pin                | ±100mA             |
| Package Thermal Impedance <sup>3</sup> | 36°C               |

#### Notes:

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level  $V_0 > V_{DDQ}$ .
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Recommended Operating Conditions

| PARAMETER           | DESCRIPTION                    | MIN                      | TYP                     | MAX                      | UNITS |
|---------------------|--------------------------------|--------------------------|-------------------------|--------------------------|-------|
| V <sub>DD</sub>     | I/O Supply Voltage             | 1.7                      | 1.8                     | 1.9                      | V     |
| V <sub>REF</sub>    | Reference Voltage              | 0.49 x V <sub>DD</sub>   | 0.5 x V <sub>DD</sub>   | 0.51 x V <sub>DD</sub>   |       |
| V <sub>TT</sub>     | Termination Voltage            | V <sub>REF</sub> - 0.04  | V <sub>REF</sub>        | V <sub>REF</sub> + 0.04  |       |
| V <sub>I</sub>      | Input Voltage                  | 0                        |                         | V <sub>DDQ</sub>         |       |
| V <sub>IH(DC)</sub> | DC Input High Voltage          | V <sub>REF</sub> + 0.125 |                         |                          |       |
| V <sub>IH(AC)</sub> | AC Input High Voltage          | V <sub>REF</sub> + 0.250 |                         |                          |       |
| V <sub>IL(DC)</sub> | DC Input Low Voltage           |                          |                         | V <sub>REF</sub> - 0.125 |       |
| V <sub>IL(AC)</sub> | AC Input Low Voltage           |                          |                         | V <sub>REF</sub> - 0.250 |       |
| V <sub>IH</sub>     | Input High Voltage Level       | RESET#,                  | 0.65 x V <sub>DDQ</sub> |                          |       |
| V <sub>IL</sub>     | Input Low Voltage Level        | C0                       |                         | 0.35 x V <sub>DDQ</sub>  |       |
| V <sub>ICR</sub>    | Common mode Input Range        | CLK, CLK#                | 0.675                   | 1.125                    |       |
| V <sub>ID</sub>     | Differential Input Voltage     |                          | 0.600                   |                          |       |
| I <sub>OH</sub>     | High-Level Output Current      |                          |                         | -8                       |       |
| I <sub>OL</sub>     | Low-Level Output Current       |                          |                         | 8                        |       |
| T <sub>A</sub>      | Operating Free-Air Temperature | 0                        |                         | 70                       | °C    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

Note: Reset# and Cn inputs must be held at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless Reset# is low.

### Mode Select

| C1 | Device Mode                 |
|----|-----------------------------|
| 0  | First Device in Pair, Front |
| 1  | Second Device in Pair, Back |



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## Advance Information

### Electrical Characteristics - DC

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 2.5 \pm 0.2\text{V}$ ,  $V_{DDQ} = 2.5 \pm 0.2\text{V}$ ; (unless otherwise stated)

| SYMBOL    | PARAMETERS   | CONDITIONS   | $V_{DDQ}$ | MIN             | TYP | MAX     | UNITS                     |
|-----------|--|--|-----------|-----------------|-----|---------|---------------------------|
| $V_{IK}$  |  | $I_I = -18\text{mA}$   |           |                 |     | -1.2    | V                         |
| $V_{OH}$  |  | $I_{OH} = -100\mu\text{A}$   | 1.7V      | $V_{DDQ} - 0.2$ |     |         |                           |
|           |  | $I_{OH} = 6\text{mA}$  | 1.7V      | 1.2             |     |         |                           |
| $V_{OL}$  |  | $I_{OL} = 100\mu\text{A}$  | 1.7V      |                 |     | 0.2     |                           |
|           |  | $I_{OL} = 6\text{mA}$  | 1.7V      |                 |     | 0.5     |                           |
| $I_I$     | All Inputs   | $V_I = V_{DD}$ or GND  | 1.9V      |                 |     | $\pm 5$ | $\mu\text{A}$             |
| $I_{DD}$  | Standby (Static)                                     | RESET# = GND   | 1.9V      |                 |     | 0.2     | $\mu\text{A}$             |
|           | Operating (Static)                                   | $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ ,<br>RESET# = $V_{DD}$  |           |                 | TBD |         |                           |
| $I_{DDD}$ | Dynamic operating<br>(clock only)                    | RESET# = $V_{DD}$ ,<br>$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ ,<br>CLK and CLK# switching<br>50% duty cycle.   | 1.8V      |                 | TBD |         | $\mu/\text{clock}$<br>MHz |
|           | Dynamic Operating<br>(per each data input)           | RESET# = $V_{DD}$ ,<br>$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ ,<br>CLK and CLK# switching<br>50% duty cycle. One data<br>input switching at half<br>clock frequency, 50%<br>duty cycle |           | $I_O = 0$       |     | TBD     |                           |
| $C_i$     | Input capacitance,<br>$D_n$ , PAR_IN inputs          | $V_I = V_{REF} \pm 250\text{mV}$   | 1.8V      | 2.5             |     | 3.5     | pF                        |
|           | Input capacitance,<br>DCS# <sub>n</sub>              | $V_I = V_{REF} \pm 250\text{mV}$   |           | 2               |     | 3       | pF                        |
|           | Input capacitance,<br>CK and CK# inputs <sup>2</sup> | $V_{ICR} = 0.9\text{V}$ ; $V_{I(PP)} = 600\text{mV}$   |           | 2               |     | 3       | pF                        |
|           | Input capacitance,<br>RESET# input                   | $V_I = V_{DD}$ or GND  |           | Note 2          |     | Note 2  | pF                        |
|           | Data Inputs  | $V_I = V_{REF} \pm 350\text{mV}$   |           | 2.5             |     | 3.5     | pF                        |
|           | CLK and CLK#   | $V_{ICR} = 1.25\text{V}$ , $V_{I(PP)} = 360\text{mV}$  |           | 2               |     | 3       |                           |
|           | RESET#   | $V_I = V_{DDQ}$ or GND   |           |                 |     |         | 2.5                       |

Notes:

- 1 - Guaranteed by design, not 100% tested in production.
- 2 - The vendor must supply this value for full device description.

### Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range (See figure 7)

| PARAMETER                       | $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ |     | UNIT |
|---------------------------------|--|-----|------|
|                                 | MIN                                    | MAX |      |
| dV/dt <sub>r</sub>              | 1                                      | 4   | V/ns |
| dV/dt <sub>f</sub>              | 1                                      | 4   | V/ns |
| dV/dt <sub>Δ</sub> <sup>1</sup> |  | 1   | V/ns |

1. Difference between dV/dt<sub>r</sub> (rising edge rate) and dV/dt<sub>f</sub> (falling edge rate)



### Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

| SYMBOL      | PARAMETERS                        | $V_{DD} = 1.8V \pm 0.1V$                                      |      | UNITS |
|-------------|-----------------------------------|---|------|-------|
|             |                                   | MIN   | MAX  |       |
| $f_{clock}$ | Clock frequency                   |   | 340  | MHz   |
| $t_{ACT}$   | Differential inputs active time   |   | 10   | ns    |
| $t_{INACT}$ | Differential inputs inactive time |   | 15   | ns    |
| $t_s$       | Setup time                        | Data before CLK $\uparrow$ , CLK# $\downarrow$                | 0.5  | ns    |
|             |                                   | DCS0 before CLK $\uparrow$ , CLK# $\downarrow$ , CSR# high    | 0.7  |       |
| $t_H$       | Hold time                         | DCS#, DODT, DCKE and Q after CK $\uparrow$ , CK# $\downarrow$ | 0.30 | ns    |
|             | Hold time                         | PARIN1 after CK $\uparrow$ , CK# $\downarrow$                 | 0.30 | ns    |

- Notes:**
- 1 - Guaranteed by design, not 100% tested in production.
  - 2 - For data signal input slew rate of 1V/ns.
  - 3 - For data signal input slew rate of 0.5V/ns and < 1V/ns.
  - 4 - CLK/CLK# signal input slew rate of 1V/ns.

### Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

| Symbol      | Parameter                                | Measurement Conditions                       | MIN | MAX | Units |
|-------------|--|--|-----|-----|-------|
| $f_{max}$   | Max input clock frequency                |  | 340 |     | MHz   |
| $t_{PDM}$   | Propagation delay, single bit switching  | CK $\uparrow$ to CK# $\downarrow$ QN         | 1.2 | 1.9 | ns    |
| $t_{LH}$    | Low to High propagation delay            | CK $\uparrow$ to CK# $\downarrow$ to PTYERR# | 1.2 | 3   | ns    |
| $t_{HL}$    | High to low propagation delay            | CK $\uparrow$ to CK# $\downarrow$ to PTYERR# | 1   | 3   | ns    |
| $t_{PDMSS}$ | Propagation delay simultaneous switching | CK $\uparrow$ to CK# $\downarrow$ QN         |     | 2   | ns    |
| $t_{PHL}$   | High to low propagation delay            | RESET# $\downarrow$ to QN $\downarrow$       |     | 3   | ns    |
| $t_{PLH}$   | Low to High propagation delay            | RESET# $\downarrow$ to PTYERR1# $\uparrow$   |     | 3   | ns    |

1. Guaranteed by design, not 100% tested in production.



# ICSSSTUA32S869B

## Advance Information

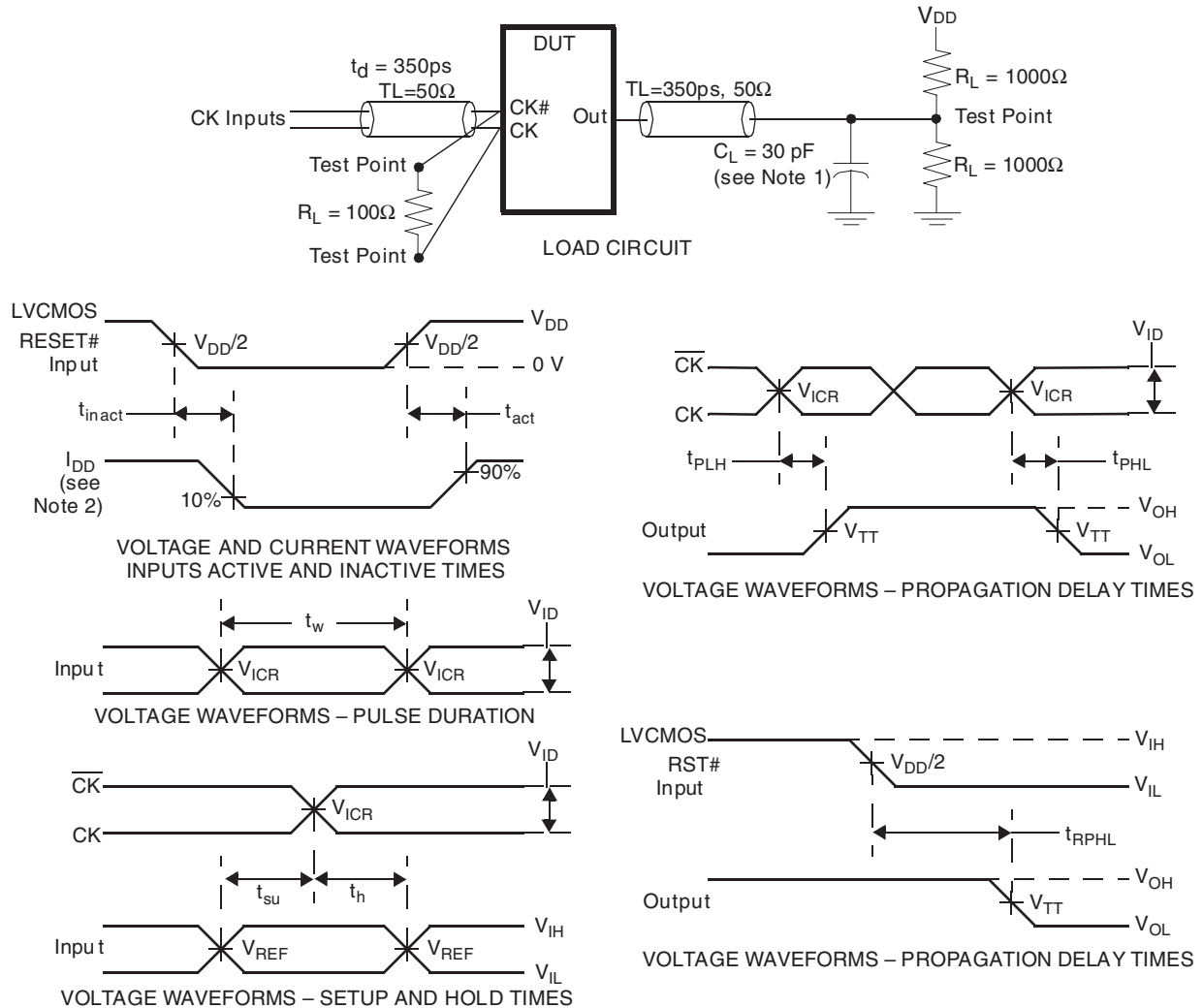


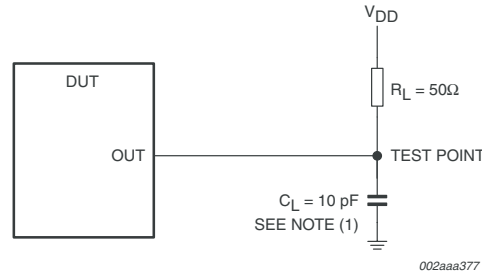
Figure 6 — Parameter Measurement Information ( $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$ )

- Notes:
1.  $C_L$  includes probe and jig capacitance.
  2.  $I_{DD}$  tested with clock and data inputs held at  $V_{DD}$  or GND, and  $I_o = 0 \text{ mA}$ .
  3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ , input slew rate =  $1 \text{ V/ns} \pm 20\%$  (unless otherwise specified).
  4. The outputs are measured one at a time with one transition per measurement.
  5.  $V_{REF} = V_{DD}/2$
  6.  $V_{IH} = V_{REF} + 250 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVC MOS input.
  7.  $V_{IL} = V_{REF} - 250 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVC MOS input.
  8.  $V_{ID} = 600 \text{ mV}$
  9.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PDM}$ .



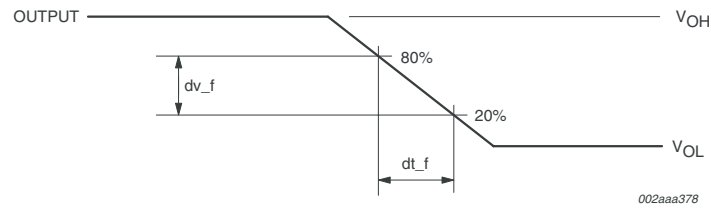
### Output slew rate measurement information ( $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$ )

All input pulses are supplied by generators having the following characteristics: PRR 10 MHz;  $Z_o = 50$ ; input slew rate =  $1 \text{ V/ns} \pm 20\%$ , unless otherwise specified.

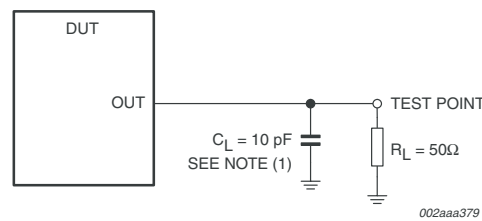


(1)  $C_L$  includes probe and jig capacitance.

**Figure 12 — Load circuit, HIGH-to-LOW slew measurement**

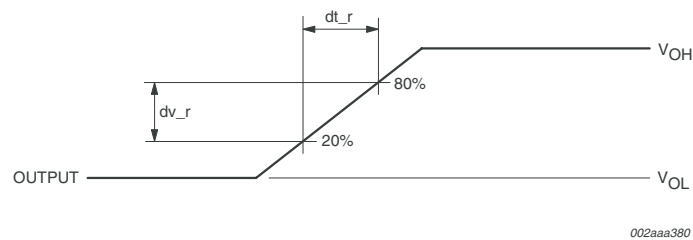


**Figure 13 — Voltage waveforms, HIGH-to-LOW slew rate measurement**



(1)  $C_L$  includes probe and jig capacitance.

**Figure 14 — Load circuit, LOW-to-HIGH slew measurement**

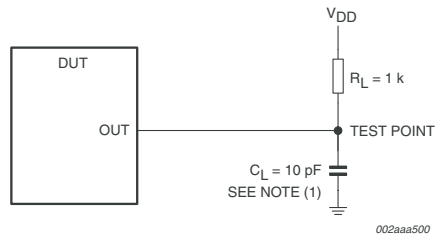


**Figure 15 — Voltage waveforms, LOW-to-HIGH slew rate measurement**



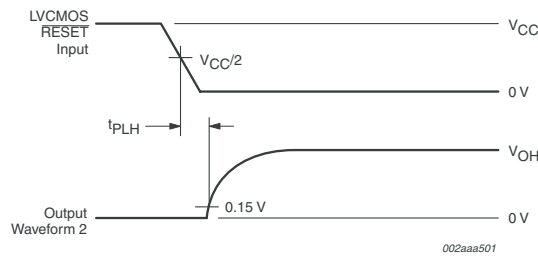
### Error output load circuit and voltage measurement information ( $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$ )

All input pulses are supplied by generators having the following characteristics: PRR10 MHz;  $Z_o = 50$ ; input slew rate =  $1 \text{ V/ns} \pm 20\%$ , unless otherwise specified.

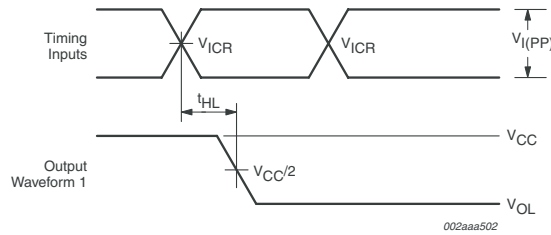


(1)  $C_L$  includes probe and jig capacitance.

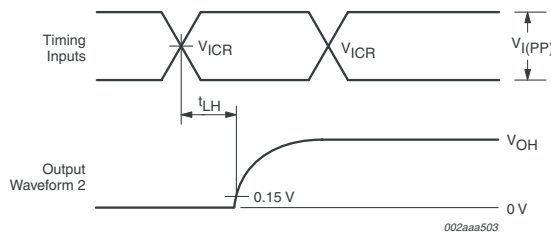
**Figure 16 — Load circuit, error output measurements**



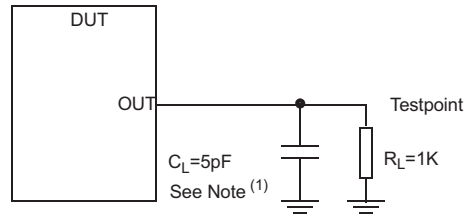
**Figure 17 — Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to RESET# input**



**Figure 18 — Voltage waveforms, open-drain output HIGH-to-LOW transition time with respect to clock inputs**

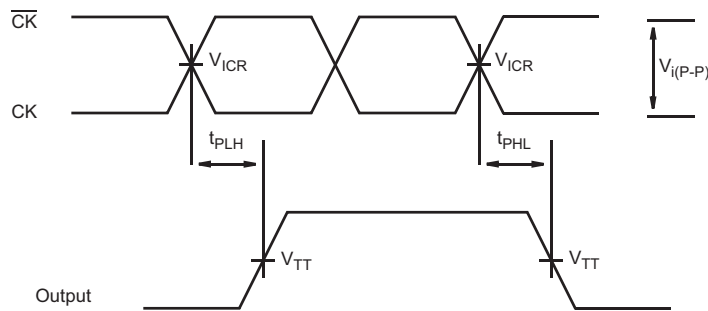


**Figure 19 — Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs**



(1)  $C_L$  includes probe and jig capacitance.

**Figure 22 — Partial parity out load circuit**



$$V_{TT} = V_{DD}/2$$

$V_{ICR}$  Cross Point Voltage

$$V_{i(P-P)} = 600mV$$

$t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$ .

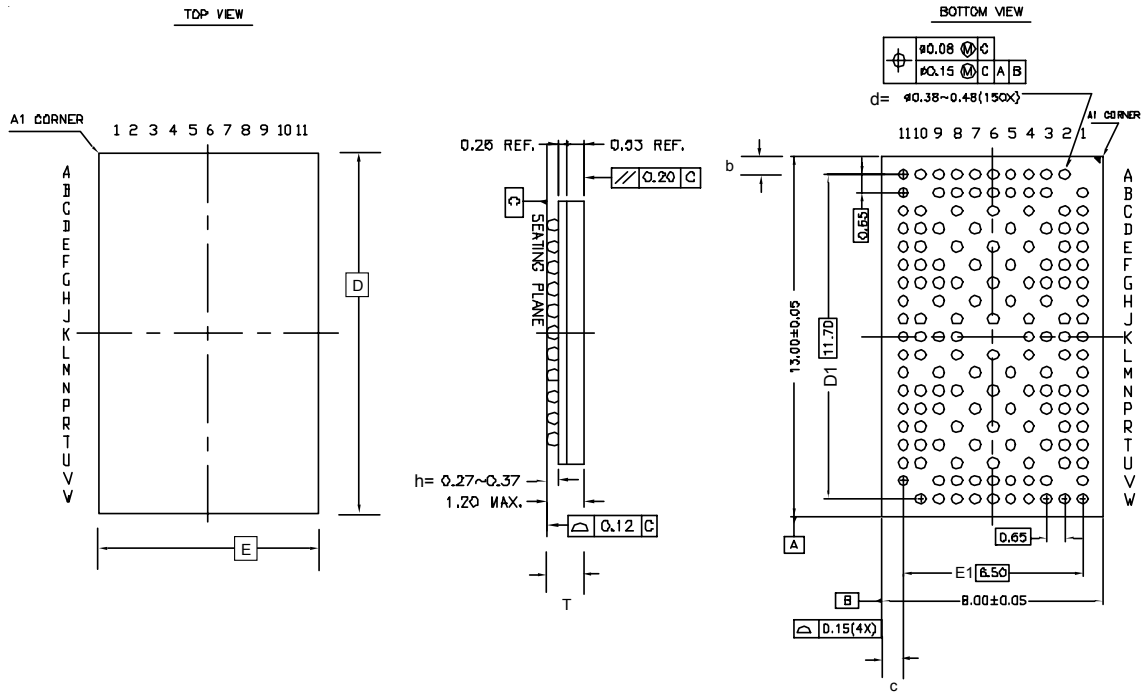
**Figure 23 — Partial parity out voltage waveform, propagation delay time with respect to CLK input**





# ICSSSTUA32S869B

## Advance Information



ALL DIMENSIONS IN MILLIMETERS

| D         | E        | T<br>Min/Max | e        | ----- BALL GRID ----- |      |       | d<br>Min/Max | h<br>Min/Max | D1        | E1       | REF. DIMS |      |
|-----------|----------|--------------|----------|-----------------------|------|-------|--------------|--------------|-----------|----------|-----------|------|
|           |          |              |          | HORIZ                 | VERT | TOTAL |              |              |           |          | b         | c    |
| 13.00 Bsc | 8.00 Bsc | 0.90/1.20    | 0.65 Bsc | 11                    | 19   | 150   | 0.38/0.48    | 0.27/0.37    | 11.70 Bsc | 6.50 Bsc | 0.65      | 0.75 |

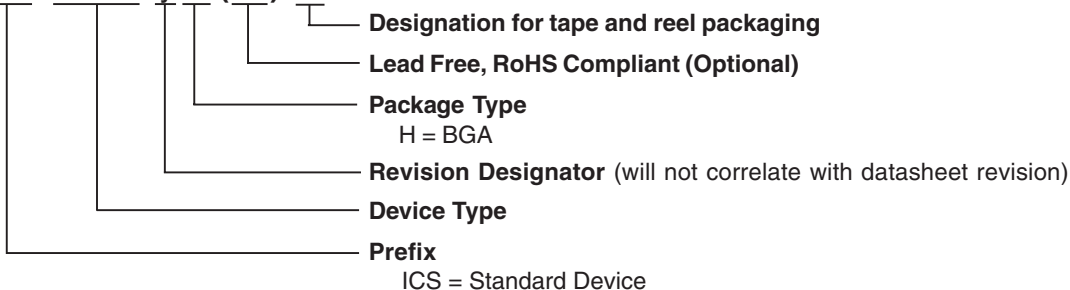
Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

## Ordering Information

### ICSSSTUA32S869BH(LF)-T

Example:

ICS XXXX y H (LF)- T





# ICSSSTUA32S869B

## Advance Information

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### Revision History

| Rev. | Issue Date | Description      | Page # |
|------|------------|------------------|--------|
| 0.1  | 10/27/2005 | Initial Release. | -      |
|      |            |                  |        |
|      |            |                  |        |
|      |            |                  |        |