DDR 24-Bit to 48-Bit Registered Buffer

Recommended Application:

- DDR Memory Modules
- Provides complete DDR DIMM logic solution with ICS93V857 or ICS95V857
- SSTL_2 compatible data registers

Product Features:

- Differential clock signals
- Supports SSTL_2 class II specifications on inputs and outputs
- Low-voltage operation
  - V_{DD} = 2.3V to 2.7V
- Available in 114 ball BGA package.

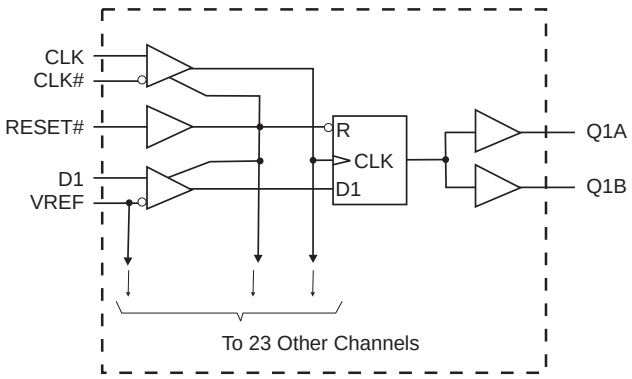
Truth Table[1]

Inputs				Q Outputs
RESET#	**CLK**	**CLK#**	**D**	**Q**
L	X or Floating	X or Floating	X or Floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0[(2)]

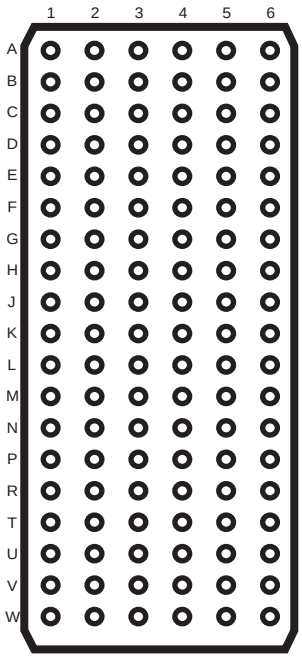
Notes:

1. H = "High" Signal Level
   L = "Low" Signal Level
   ↑ = Transition "Low"-to-"High"
   ↓ = Transition "High"-to-"Low"
   X = Don't Care
2. Output level before the indicated steady state input conditions were established.

Block Diagram



Pin Configuration



114-Pin Ball BGA

Pin Configuration Assignments

	1	2	3	4	5	6
A	Q2A	Q1A	CLK	CLK#	Q1B	Q2B
B	Q3A	VDDQ	GND	GND	VDDQ	Q3B
C	Q5A	Q4A	VDDQ	VDDQ	Q4B	Q5B
D	Q7A	Q6A	GND	GND	Q6B	Q7B
E	Q8A	GND	VDDQ	VDDQ	GND	Q8B
F	Q10A	Q9A	VDDQ	VDDQ	Q9B	Q10B
G	Q12A	Q11A	GND	GND	Q11B	Q12B
H	Q13A	VDD	VDDQ	VDDQ	VDD	Q13B
J	Q14A	Q15A	GND	GND	Q15B	Q14B
K	Q17A	Q16A	VDDQ	VDDQ	Q16B	Q17B
L	Q18A	Q19A	GND	GND	Q19B	Q18B
M	Q20A	VDDQ	GND	GND	VDDQ	Q20B
N	Q22A	Q21A	VDDQ	VDDQ	Q21B	Q22B
P	Q23A	VDDQ	GND	GND	VDDQ	Q23B
R	Q24A	VDD	RESET#	VREF	VDD	Q24B
T	D2	D1	D6	D18	D13	D14
U	D4	D3	D10	D22	D15	D16
V	D5	D7	D11	D23	D19	D17
W	D8	D9	D12	D24	D21	D20

General Description

The 24-bit-to-48-bit **ICSSSTV32852** is a universal bus driver designed for 2.3V to 2.7V V_{DD} operation and SSTL_2 I/O levels, except for the LVCMOS RESET# input.

Data flow from D to Q is controlled by the differential clock (CLK/CLK#) and a control signal (RESET#). The positive edge of CLK is used to trigger the data flow and CLK# is used to maintain sufficient noise margins where as RESET#, an LVCMOS asynchronous signal, is intended for use at the time of power-up only. **ICSSSTV32852** supports low-power standby operation. A logic level "Low" at RESET# assures that all internal registers and outputs (Q) are reset to the logic "Low" state, and all input receivers, data (D) and clock (CLK/CLK#) are switched off. Please note that RESET# must always be supported with LVCMOS levels at a valid logic state because VREF may not be stable during power-up.

To ensure that outputs are at a defined logic state before a stable clock has been supplied, RESET# must be held at a logic "Low" level during power up.

In the DDR DIMM application, RESET# is specified to be completely asynchronous with respect to CLK and CLK#. Therefore, no timing relationship can be guaranteed between the two signals. When entering a low-power standby state, the register will be cleared and the outputs will be driven to a logic "Low" level quickly relative to the time to disable the differential input receivers. This ensures there are no glitches on the output. However, when coming out of low-power standby state, the register will become active quickly relative to the time to enable the differential input receivers. When the data inputs are at a logic level "Low" and the clock is stable during the "Low"-to-"High" transition of RESET# until the input receivers are fully enabled, the design ensures that the outputs will remain at a logic "Low" level.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
R1,P1, N1, N2, M1, L2, L1, K1, K2, J2, J1, H1, G1, G2, F1, F2, E1, D1, D2, C1, C2, B1, A1, A2	Q (24:1)A	OUTPUT	Data output
R6, P6, N6, N5, M6, L5, L6, K6, K5, J5, J6, H6, G6, G5, F6, F5, E6, D6, D5, C6, C5, B6, A6, A5	Q (24:1)B	OUTPUT	Data output
E2, B3, D3, G3, J3, L3, M3, P3, B4, D4, G4, J4, L4, M4, P4, E5	GND	PWR	Ground
B2, M2, P2, C3, E3, F3, H3, K3, N3, C4, E4, F4, H4, K4, N4, B5, M5, P5	VDDQ	PWR	Output supply voltage, 2.5V nominal
W4, V4, U4, W5, W6, V5, T4, V6, U6, U5, T6, T5, W3, V3, U3, W2, W1, V2, T3, V1, U1, U2, T1, T2	D (24:1)	INPUT	Data input
A3	CLK	INPUT	Positive master clock input
A4	CLK#	INPUT	Negative master clock input
H2, H5, R2, R5	VDD	PWR	Core supply voltage, 2.5V nominal
R3	RESET#	INPUT	Reset (active low)
R4	VREF	INPUT	Input reference voltage, 1.25V nominal

Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Supply Voltage	-0.5 to 3.6V
Input Voltage[1]	-0.5 to VDD +0.5
Output Voltage[1,2]	-0.5 to VDDQ +0.5
Input Clamp Current	±50 mA
Output Clamp Current	±50mA
Continuous Output Current	±50mA
VDD, VDDQ or GND Current/Pin	±100mA
Package Thermal Impedance[3]	55°C/W

Notes:
1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level $V_O > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		2.3	2.5	2.7	V
V_{DDQ}	I/O Supply Voltage		2.3	2.5	2.7	
V_{REF}	Reference Voltage		1.15	1.25	1.35	
V_{TT}	Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	
V_I	Input Voltage		0		V_{DDQ}	
$V_{IH\ (DC)}$	DC Input High Voltage	Data Inputs	V_{REF} + 0.15			
$V_{IH\ (AC)}$	AC Input High Voltage		V_{REF} + 0.31			
$V_{IL\ (DC)}$	DC Input Low Voltage				V_{REF} - 0.15	
$V_{IL\ (DC)}$	AC Input Low Voltage				V_{REF} - 0.31	
V_{IH}	Input High Voltage Level	RESET#	1.7			
V_{IL}	Input Low Voltage Level				0.7	
V_{ICR}	Common mode Input Range	CLK, CLK#	0.97		1.53	
V_{ID}	Differential Input Voltage		0.36			
V_{IX}	Cross Point Voltage of Differential Clock Pair		$(V_{DDQ}/2)$ - 0.2		$(V_{DDQ}/2)$ + 0.2	
I_{OH}	High-Level Output Current				19	mA
I_{OL}	Low-Level Output Current				19	
T_A	Operating Free-Air Temperature		0		70	°C

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - DC

T_A = 0 - 70°C; V_{DD} = 2.5 +/-0.2V, V_{DDQ}=2.5 +/-0.2V; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS		V_{DDQ}	MIN	TYP	MAX	UNITS
V_{IK}		I_I = -18mA		2.3V			-1.2	V
V_{OH}		I_{OH} = -100µA		2.3V - 2.7V	V_{DDQ} - 0.2			
		I_{OH} = -16mA		2.3V	2.05			
V_{OL}		I_{OL} = 100µA		2.3V - 2.7V			0.2	
		I_{OL} = 16mA		2.3V			0.20	
I_I	All Inputs	$V_I = V_{DD}$ or GND		2.7V			±5	µA
I_{DD}	Standby (Static)	RESET# = GND	I_O = 0	2.5V			0.01	µA
	Operating (Static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESET# = V_{DD}				40		mA
I_{DDD}	Dynamic operating (clock only)	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLK# switching 50% duty cycle.				35		µA/clock MHz
	Dynamic Operating (per each data input)	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL\ (AC)}$, CLK and CLK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle				7		µA/ clock MHz/data
r_{OH}	Output High	I_{OH} = -20mA		2.3V - 2.7V		12		Ω
r_{OL}	Output Low	I_{OL} = 20mA		2.3V - 2.7V		10		Ω
$r_{O(D)}$	[r_{OH} - r_{OL}] each separate bit	I_O = 20mA, T_A = 25°C		2.5V			4	Ω
C_i	Data Inputs	$V_I = V_{REF}$ ±350mV		2.5V	2.5		3.5	pF
	CLK and CLK#	V_{ICR} = 1.25V, $V_{I(PP)}$ = 360mV			2.5		3.5	

Notes:

1. Guaranteed by design, not 100% tested in production.

Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

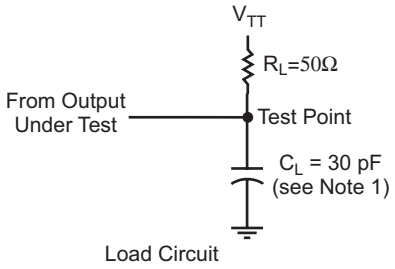
SYMBOL	PARAMETERS		V_{DD} = 2.5V ±0.2V		UNITS
			MIN	MAX	
f_{clock}	Clock frequency			200	MHz
t_{PD}	Clock to output time		1.9	2.7	ns
t_{RST}	Reset to output time			4.5	ns
t_{SL}	Output slew rate		1	4	V/ns
t_S	Setup time, fast slew rate [2, 4]	Data before CLK↑, CLK#↓	0.50		ns
	Setup time, slow slew rate [3, 4]		0.70		ns
T_h	Hold time, fast slew rate [2, 4]	Data after CLK↑, CLK#↓	0.30		ns
	Hold time, slow slew rate [3, 4]		0.50		ns

Notes: 1 - Guaranteed by design, not 100% tested in production.
2 - For data signal input slew rate of 1V/ns.
3 - For data signal input slew rate of 0.5V/ns and < 1V/ns.
4 - CLK/CLK# signal input slew rate of 1V/ns.

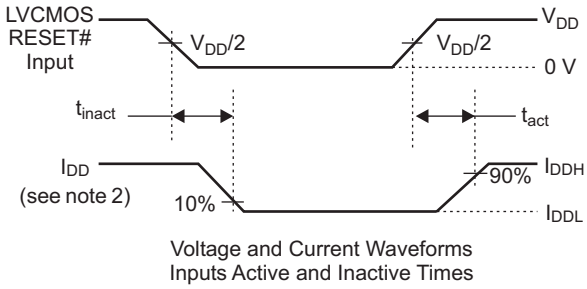
Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

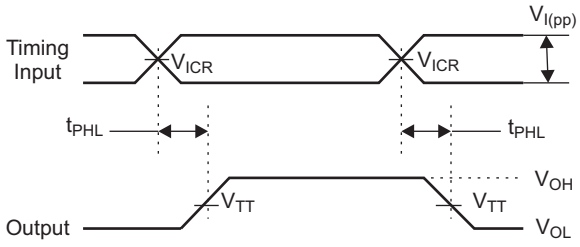
SYMBOL	From (Input)	To (Output)	V_{DD} = 2.5V ±0.2V			UNITS
			MIN	TYP	MAX	
fmax			200			MHz
t_{PD}	CLK, CLK#	Q	1.9		2.7	ns
t_{phl}	RESET#	Q			4.5	ns



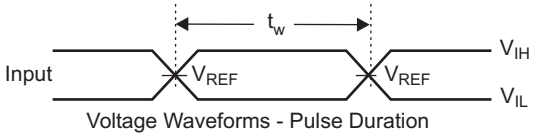
Load Circuit



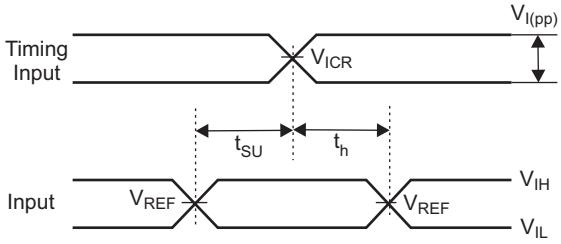
Voltage and Current Waveforms
Inputs Active and Inactive Times



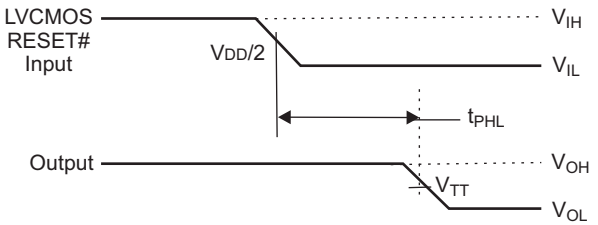
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



Voltage Waveforms - Setup and Hold Times

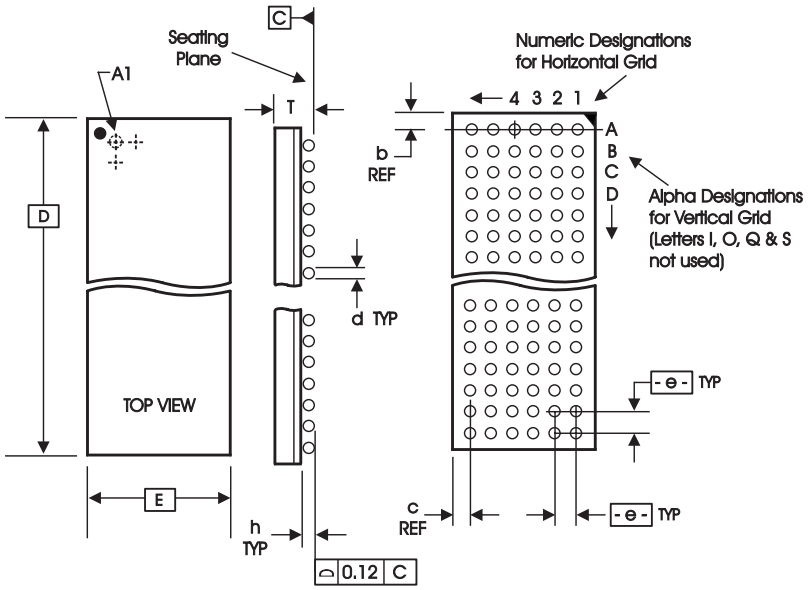


Voltage Waveforms - Propagation Delay Times

Parameter Measurement Information (V_{DD} = 2.5V ±0.2V)

Notes: 1. CL incluces probe and jig capacitance.

2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and Io = 0mA.
3. All input pulses are supplied by generators having the following chareacteristics: PRR ≤10 MHz, Zo=50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DDQ}/2$
6. $V_{IH} = V_{REF}$ + 310mV (ac voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
7. $V_{IL} = V_{REF}$ -310mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. t_{PLH} and t_{PHL} are the same as t_{pd}



D	E	T Min/Max	e	----- BALL GRID ----- HORIZ	VERT	TOTAL	d	h Min/Max	REF. DIMENSIONS b	c
16.00 Bsc	5.50 Bsc	1.30/1.50	0.80 Bsc	6	19	114	0.46	0.31/0.41	0.80	0.75

ALL DIMENSIONS IN MILLIMETERS
10-0055

Ordering Information

ICSSSTV32852yHT

Example:

ICS XXXX y H - T

- **Designation for tape and reel packaging**
- **Package Type**
  H = BGA
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0513F—05/13/03