SONY

ICX044BKA

1/3 inch CCD Image Sensor for NTSC Color Camera

Description

The ICX044BKA is an interline transfer CCD solid-state image sensor suitable for NTSC 1/3 inch color video cameras. High sensitivity is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

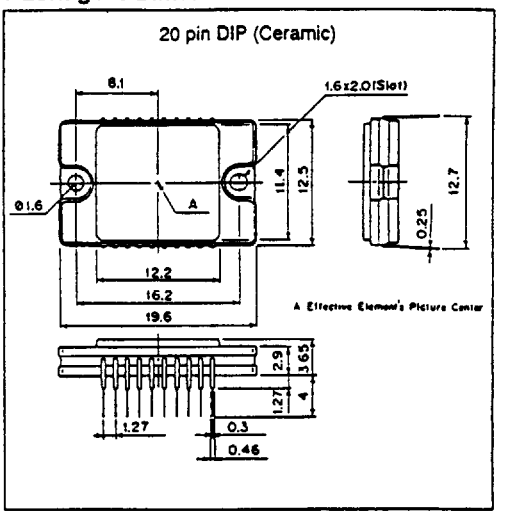
This chip features a field integration read out system and an electronic shutter with variable charge-storage time. 20 pin Cer-DIP package.

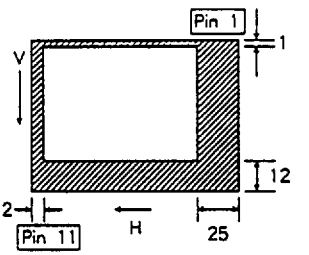
Features

- High sensitivity (+6dB compare with ICX 044AK) and low dark current
- Consecutive various speed shutter
  1/60s (Typ.), 1/100s to 1/10000s
- Low smear
- High antiblooming
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- Reset gate 5V drive

Package Outline

Unit : mm



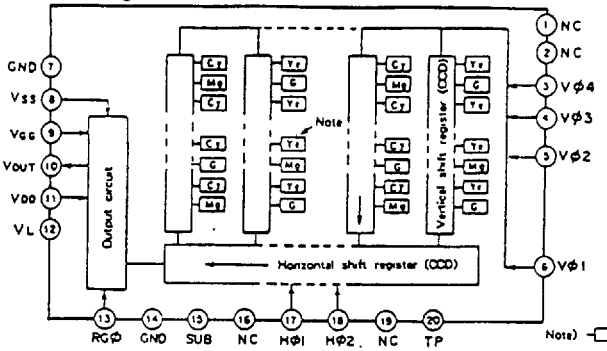


Optical black position (Top View)

Device Structure

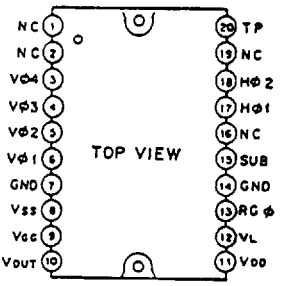
- Optical size 1/3 inch format
- Number of effective pixels
  510 (H) × 492 (V) Approx. 250k pixels
- Number of total pixels
  537 (H) × 505 (V) Approx. 270k pixels
- Interline transfer CCD image sensor
- Chip size 6.3mm (H) × 5.4mm (V)
- Unit cell size 9.6 µm (H) × 7.5 µm (V)
- Optical black Horizontal (H) direction Front 2 pixels Rear 25 pixels
  Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits Horizontal 16
  Vertical 1 (even field only)
- Substrate material silicon

Block Diagram



Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	NC		11	V_{DD}	Output amplifier drain supply
2	NC		12	V_L	Protective transistor bias
3	V φ 4	Vertical register transfer clock	13	RG φ	Reset gate clock
4	V φ 3	Vertical register transfer clock	14	GND	GND
5	V φ 2	Vertical register transfer clock	15	SUB	Substrate (Overflow drain)
6	V φ 1	Vertical register transfer clock	16	NC	
7	GND	GND	17	H φ 1	Horizontal register transfer clock
8	Vss	Output amplifier source	18	H φ 2	Horizontal register transfer clock
9	V_{GG}	Output amplifier gate bias	19	NC	
10	V_{OUT}	Signal output	20	TP	Input bias

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		−0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, Vss, TP − GND	−0.3 to +18	V	
	V_{DD}, V_{OUT}, Vss, TP − SUB	−55 to +10	V	
Clock input voltage	V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, H φ 2 − GND	−15 to +20	V	
	V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, H φ 2 − SUB	to +10	V	
Voltage difference between vertical clock input pins		to+15	V	*
Voltage difference between horizontal clock input pins		to+17	V	
H φ 1, H φ 2 − V φ 4		−17 to +17	V	
RG, V_{GG} − GND		−10 to +15	V	
RG, V_{GG} − SUB		−55 to +10	V	
V_L − SUB		−65 to +0.3	V	
Beside GND, SUB-V_L		−0.3 to +30	V	
Storage temperature		−30 to +80	°C	
Operating temperature		−10 to +60	°C	

* +27V (Max.) when clock width<10 μs, duty factor<0.1%.

Bias Conditions

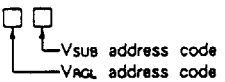
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 680 Ω resistor				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	Δ V_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*1
Fluctuation range after reset gate clock voltage adjustment	Δ V_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*2				
Input bias	TP	14.55	15.0	15.45	V	

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		3		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

*1) Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address–1 digit display
V_{RGL} code address–1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*2) V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

* 3) 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss, SUB, TP pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to V φ 1, V φ 2, V φ 3, V φ 4, H φ 1 and H φ 2, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

* 4) Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

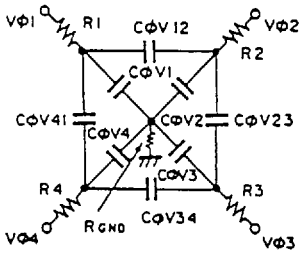
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2} V_{VH3}, V_{VH4}	− 0.2	0	0.1	V	2	V_{VH}= (V_{VH1}+V_{VH2}) /2
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	− 9.6	− 9.0	− 8.5	V	2	V_{VL}= (V_{VL3}+V_{VL4}) /2
	V φ v	8.3	9.0	9.7	V	2	V φ v=V_{VHn} − V_{VLn} (n=1 to 4)
	|V_{VH1} − V_{VH2}|			0.1	V	2	
	V_{VH3} − V_{VH}	− 0.25		0.1	V	2	
	V_{VH4} − V_{VH}	− 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	V φ H	4.75	5.0	5.25	V	3	
	V_{HL}	− 0.05	0	0.05	V	3	
Reset gate clock voltage	V φ RG	4.5	5.0	5.5	V	4	*
	V_{RGLH} − V_{RGLL}			0.8	V	4	Low level coupling
Substrate clock voltage	V φ SUB	23.0	24.0	25.0	V	5	

* No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

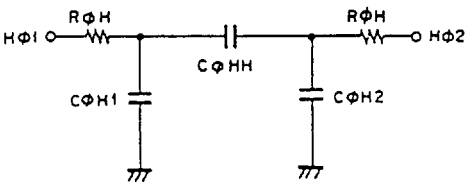
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	− 0.1	0	0.1	V	4	
	V φ RG	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		820		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		1000		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		680		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		470		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		40		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		40		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		5		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		270		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		20		Ω	



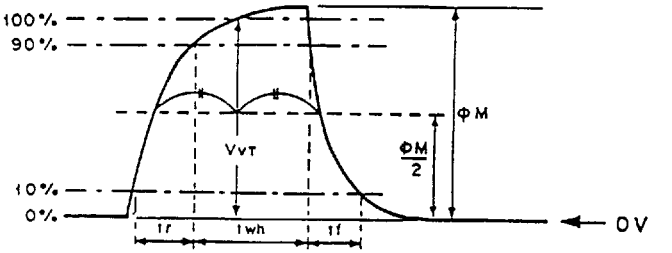
Vertical transfer clock equivalent circuit



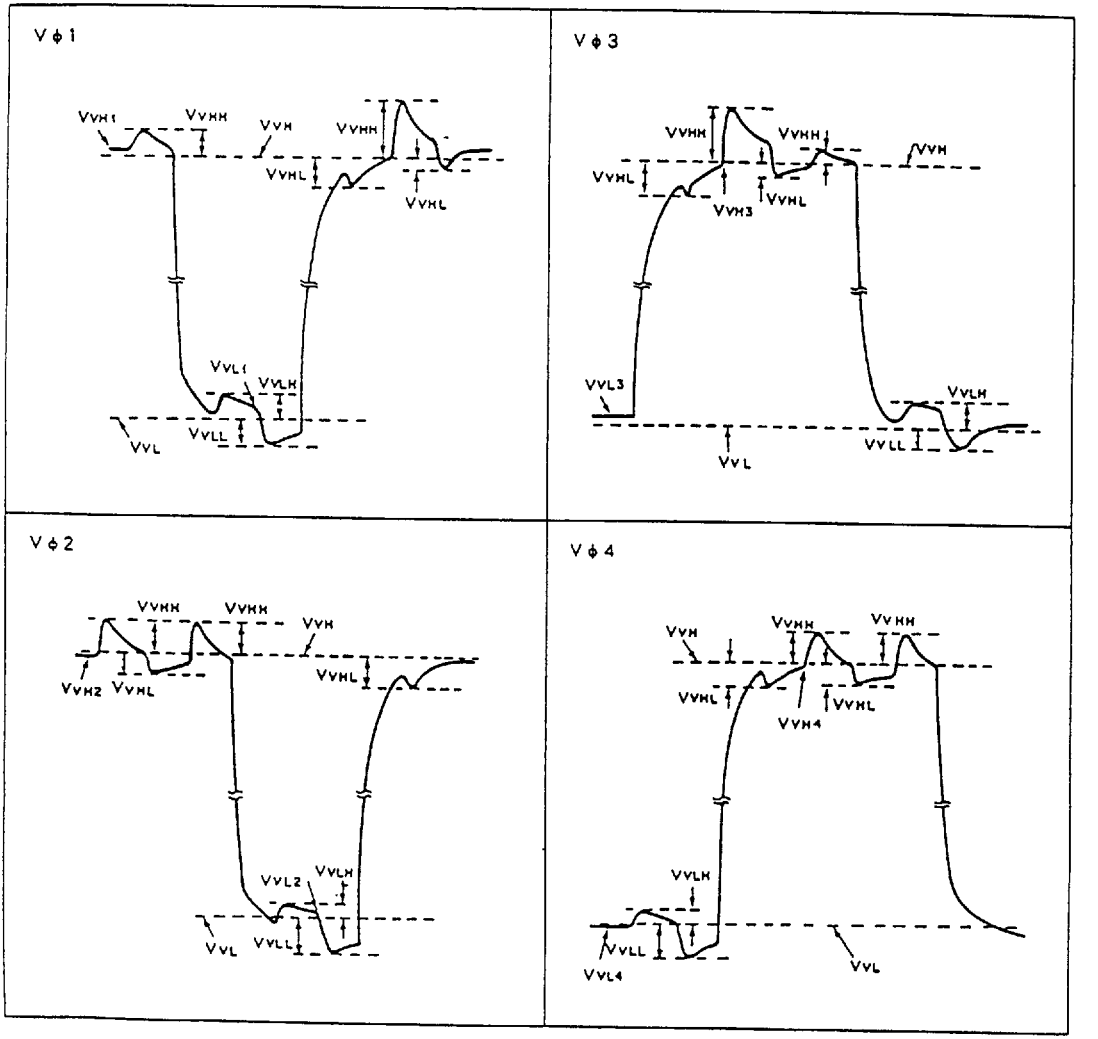
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

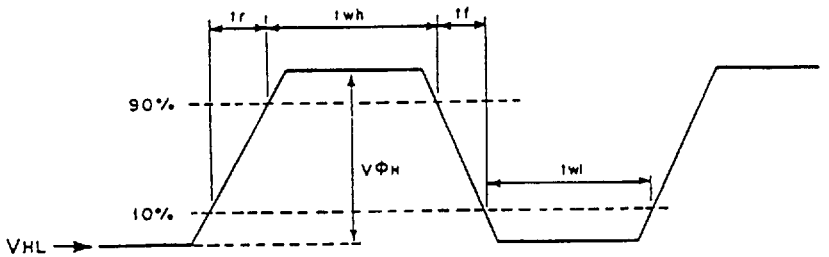
(1) Read out clock waveform



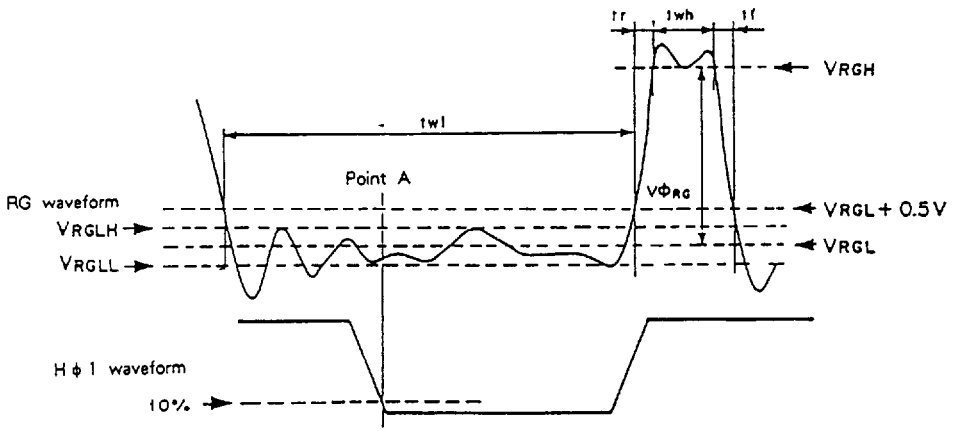
(2) Vertical transfer clock waveform



(3) Horizontal transfer clock waveform diagram



(4) Reset gate clock waveform diagram



VRGLH is the maximum value and VRGLL the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

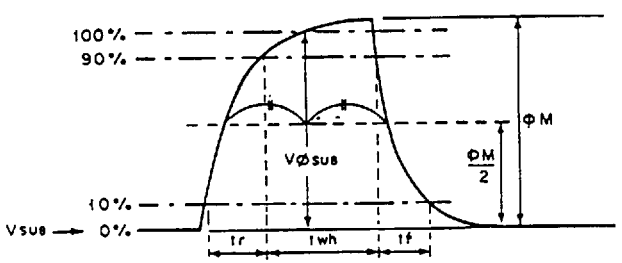
VRGL is the mean value for VRGLH and VRGLL.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

VRGH is the minimum value for twh period.

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		µs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										0.015		0.25	µs	*1
Horizontal transfer clock	$H\phi$	37	41		38	42			12	15	*2	1.0	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.012		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.012		µs	
Reset gate clock	ϕ_{RG}	11	15		75	79			6.5			4.5		ns	
Substrate clock	ϕ_{SUB}	1.5	2.0							0.5			0.5	µs	During charge drain.

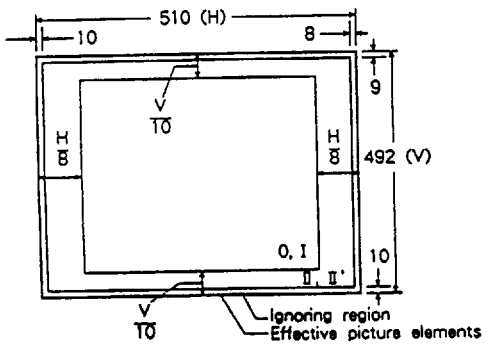
* 1) When vertical transfer clock driver CXD1250 is in use.
* 2) tf ≧ tr−2 ns

Image Sensor Characteristics

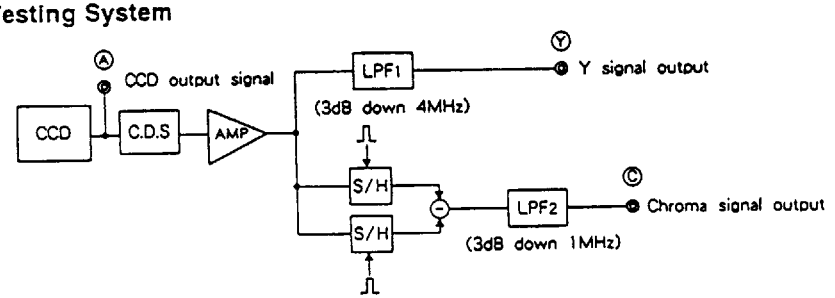
(Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	400	480		mV	1	
Saturation signal	Ysat	600			mV	2	Ta=60°C
Smear	Sm		0.007	0.012	%	3	
Video signal shading	SHy			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Uniformity between signal channels	Δ Sr			10	%	5	
	Δ Sb			10	%	5	
Dark signal	Ydt			2	mV	6	Ta=60°C
Dark signal shading	Δ Ydt			1	mV	7	Ta=60°C
Flicker Y	Fy			2	%	8	
Flicker R − Y	Fcr			5	%	8	
Flicker B − Y	Fcb			5	%	8	
Horizontal stripes R	Lcr			3.5	%	9	
Horizontal stripes G	Lcg			3.5	%	9	
Horizontal stripes B	Lcb			3.5	%	9	
Horizontal stripes W	Lcw			3.5	%	9	
Lag	Lag			0.5	%	10	

Zone Chart of Video Signal Shading



Testing System



Note) Adjust AMP gain so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

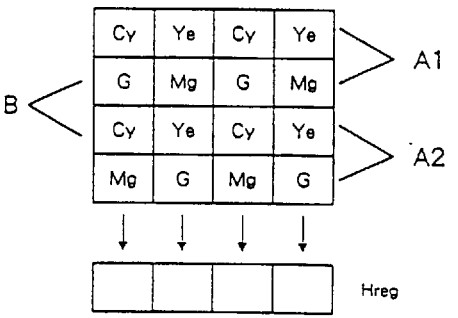
Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference for the signal output which is taken as the Y signal output or the chroma signal output of the testing system.

◎ Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals



Color Coding Diagram

CFA of this image sensor is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns.
The read out line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are [G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{ (G+Cy) + (Mg+Ye) \} \times 1/2$$
$$= 1/2 \{ 2B+3G+2R \}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{ (Mg+Ye) - (G+Cy) \}$$
$$= \{ 2R - G \}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{ (G+Ye) + (Mg+Cy) \} \times 1/2$$
$$= 1/2 \{ 2B+3G+2R \}$$
$$-(B - Y) = \{ (G+Ye) - (Mg+Cy) \}$$
$$= -\{ 2B - G \}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R − Y and − (B − Y) on alternate lines.
It is the same for B field.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/ m², color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F5.6.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard image condition I. After selecting the electronic shutter mode at a 1/250s. shutter speed, measure the Y signal (Ys) at the center of the screen and substitute in the following formula.

   $$S = Ys \times \frac{250}{60}$$

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of Y signal output average value (Y_A=180mV), then test Y signal minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of Y signal output average value (Y_A=180mV). Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value YSm of Y signal output.

   $$Sm = \frac{YSm}{Y_A} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV) with lens diaphragm at F5.6 to F8. Then test maximum (Ymax) and minimum (Ymin) values of Y signal.

   $$SHy = (Ymax - Ymin) / Y_A \times 100\ (\%)$$

5. Video signal between channels uniformity
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then test maximum (Crmax, Cbmax) and minimum (Crmin, Cbmin) values of chroma signals from R − Y and B − Y channels.

   $$\Delta Sr = |(Crmax - Crmin) / Y_A| \times 100\ (\%)$$
   $$\Delta Sb = |(Cbmax - Cbmin) / Y_A| \times 100\ (\%)$$

6. Dark signal
   Test Y signal output average value Ydt when the device ambient temperature is at 60 °C and light is obstructed with horizontal idle transfer level as reference.

7. Dark signal shading
   Following 6, test maximum (Ydmax) and minimum (Ydmin) values of dark signal output.

   $$\Delta Ydt = Ydmax - Ydmin$$

8. Flicker

① Fy

Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then test the Y signal difference (Δ Yf) between even field and odd field.

$Fy = (\Delta Yf / Y_A) \times 100 (\%)$

② Fcr, Fcb

Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then insert R or B filter, and test the C signal difference (Δ Cr, Δ Cb) between even field and odd field and the C signal output average value (CAr, CAb).

$Fci = (\Delta Ci / CAi) \times 100 (\%)$ (i=r, b)

9. Lateral stripe

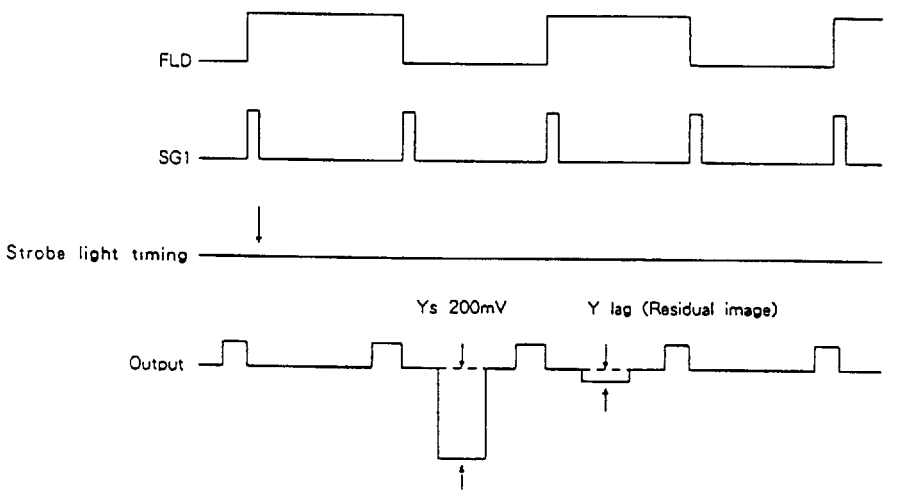
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A=180mV). Then insert R, G and B filters respectively, and test the signal difference (Δ Ylw, Δ Ylr, Δ Ylg, Δ Ylb) between Y signal lines of the same field.

$Lci = (\Delta Yli / Y_A) \times 100 (\%)$ (i=w, r, g, b)

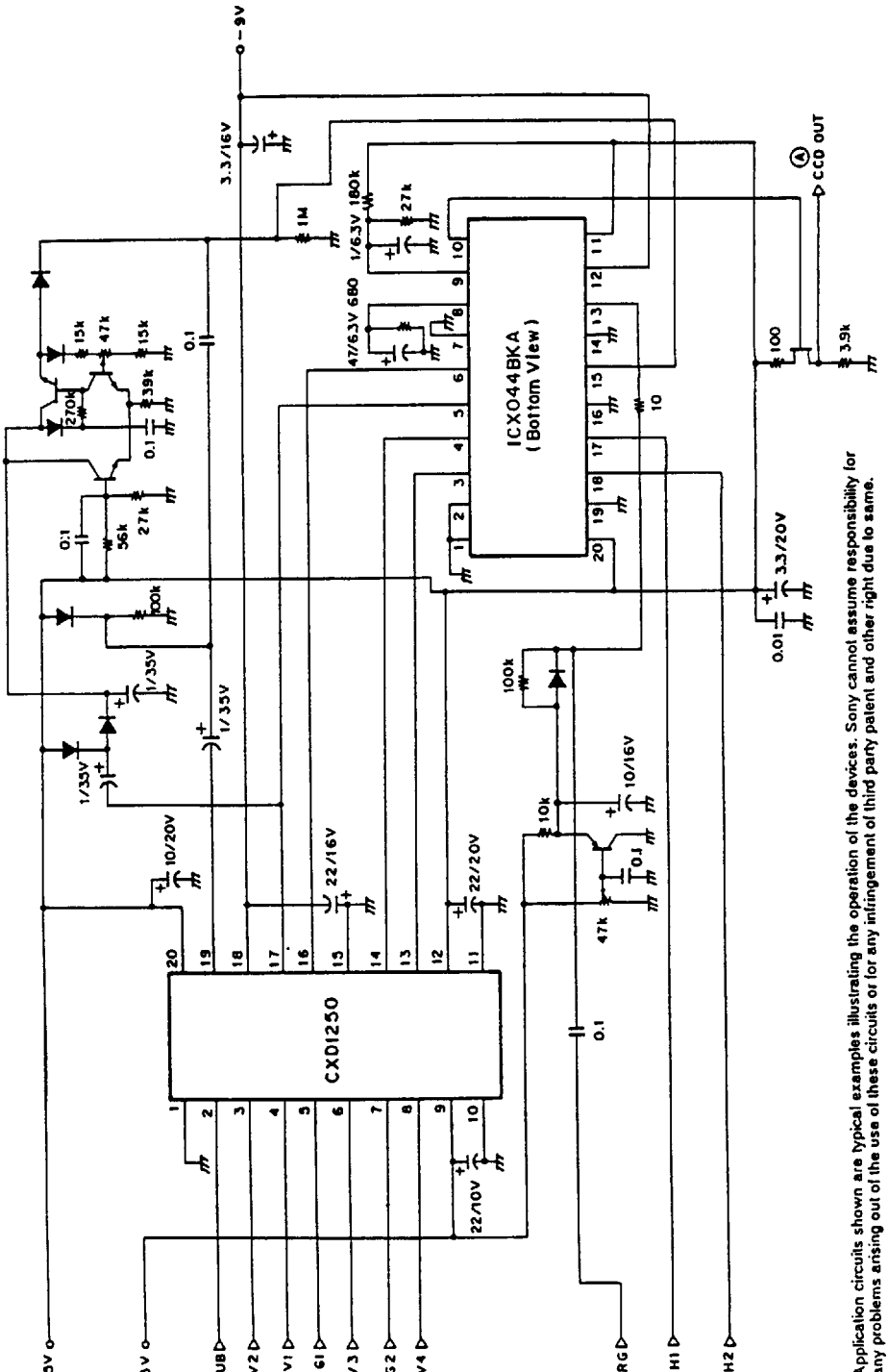
10. Residual image

Adjust Y signal output value (Ys) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Ylag).

Lag = (Ylag/Ys) × 100 (%)



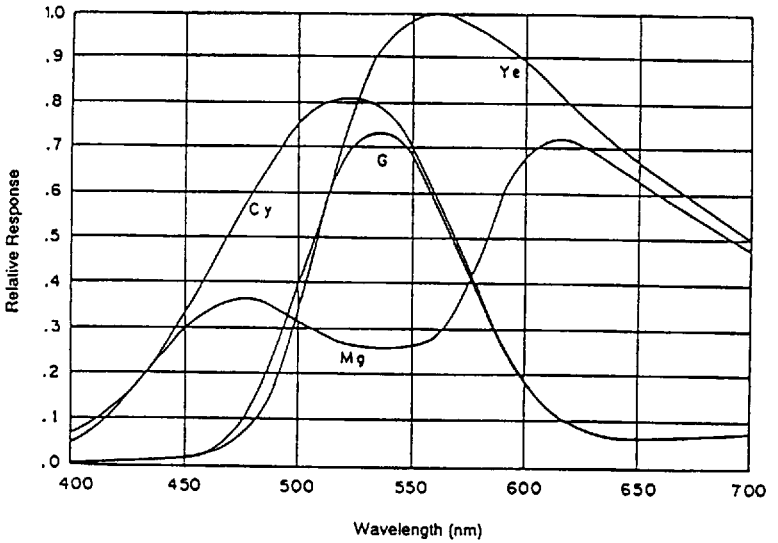
Drive Circuit



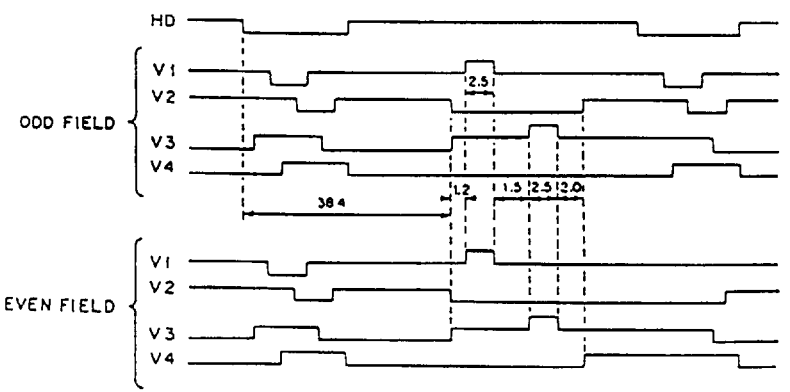
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Spectral Sensitivity Characteristics

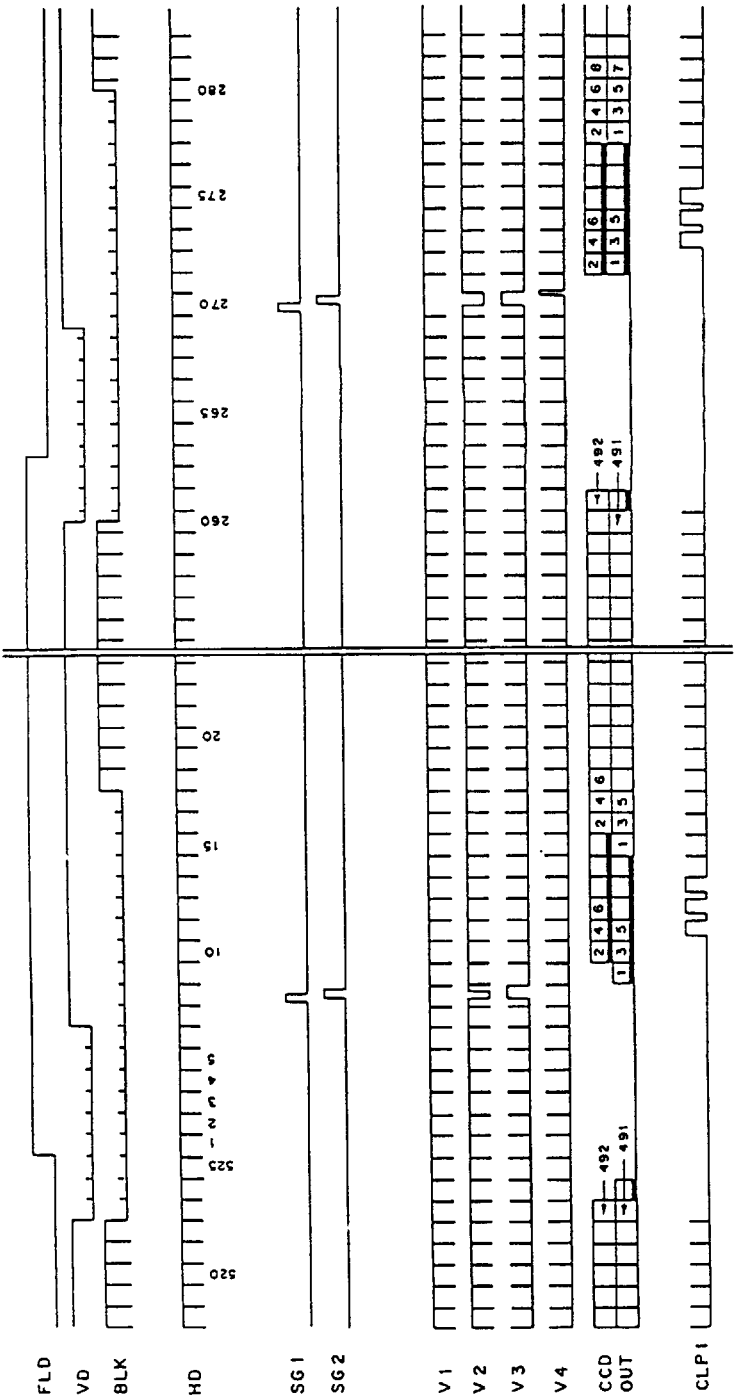
(Excluding light source characteristics, including lens characteristics)



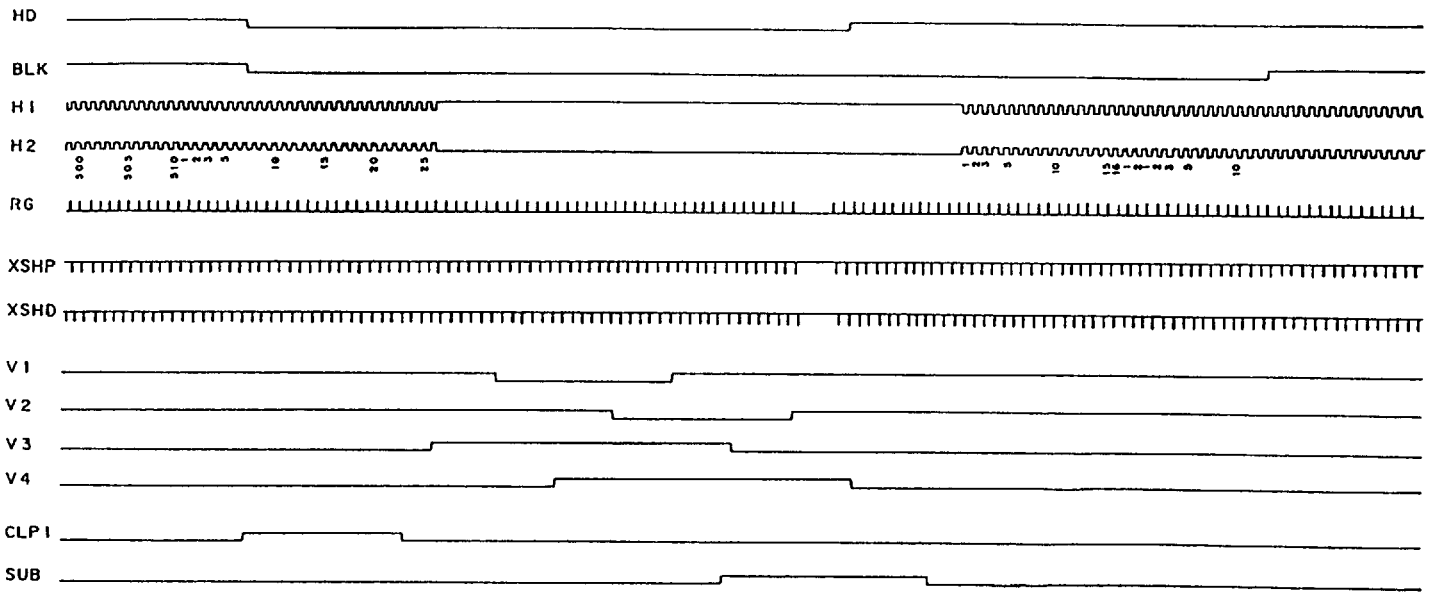
Sensor Read Out Clock Timing Chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80 °C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldenng tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
   a) Operate in clean environments (around class 1000 will be appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.