SONY®

ICX044BLA

1/3 inch CCD Image Sensor for EIA B/W Camera

Description

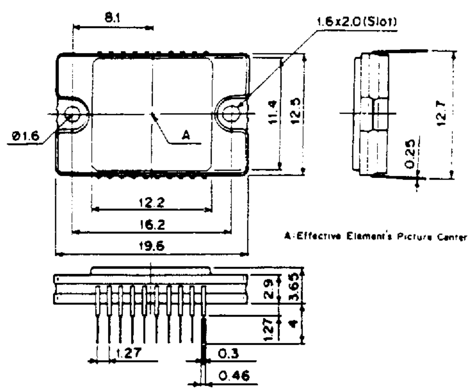
The ICX044BLA is an interline transfer CCD solid-state image sensor suitable for EIA 1/3 inch B/W video cameras. High sensitivity is achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20pin Cer-DIP Package.

Package Outline

Unit : mm

20 pin DIP (Cer-DIP)

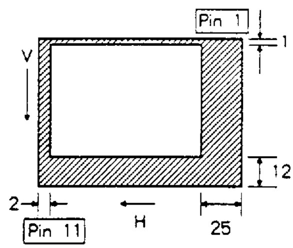


Features

- High sensitivity (+6dB compare with ICX044AL) and low dark current
- Consecutive various speed shutter 1/60s. (Typ.), 1/100s. to 1/10000s.
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

Device Structure

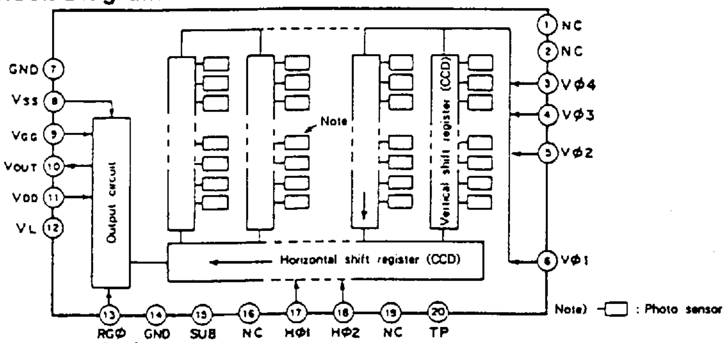
- Optical size 1/3 inch format
- Number of effective pixels
  510 (H) × 492 (V) Approx. 250k pixels
- Number of total pixels
  537 (H) × 505 (V) Approx. 270k pixels
- Interline transfer CCD image sensor
- Chip size 6.3mm (H) × 5.4mm (V)
- Unit cell size 9.6 μm (H) × 7.5 μm (V)
- Optical black Horizontal (H) direction Front 2 pixels Rear 25 pixels
  Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits Horizontal 16
  Vertical 1 (even field only)
- Substrate material silicon



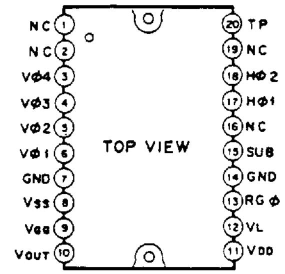
Optical black position (Top View)

8382383 0006535 198

Block Diagram



Pin Configuration



Pin Description

No.	Symbol	Description		No.	Symbol
1	NC		11	V_{DD}	Output amplifier drain supply
2	NC		12	V_L	Protective transistor bias
3	$V\phi_4$	Vertical register transfer clock	13	RG ϕ	Reset gate clock
4	$V\phi_3$	Vertical register transfer clock	14	GND	GND
5	$V\phi_2$	Vertical register transfer clock	15	SUB	Substrate (Overflow drain)
6	$V\phi_1$	Vertical register transfer clock	16	NC	
7	GND	GND	17	$H\phi_1$	Horizontal register transfer clock
8	Vss	Output amplifier source	18	$H\phi_2$	Horizontal register transfer clock
9	V_{GG}	Output amplifier gate bias	19	NC	
10	V_{OUT}	Signal output	20	TP	Input bias

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		–0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, Vss, TP – GND	–0.3 to +18	V	
	V_{DD}, V_{OUT}, Vss, TP – SUB	–55 to +10	V	
Clock input voltage	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$, $H\phi_2$ – GND	–15 to +20	V	
	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$, $H\phi_2$ – SUB	–65 to +10	V	
Voltage difference between vertical clock input pins		to+15	V	*
Voltage difference between horizontal clock input pins		to+17	V	
$H\phi_1$, $H\phi_2$ – $V\phi_4$		–17 to +17	V	
RG, V_{GG} – GND		–10 to +15	V	
RG, V_{GG} – SUB		–55 to +10	V	
V_L – SUB		–65 to +0.3	V	
Beside GND, SUB-V_L		–0.3 to +30	V	
Storage temperature		–30 to +80	℃	
Operating temperature		–10 to +60	℃	

* +27V (Max.) when clock width<10 μs, duty factor<0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	–3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*1
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	–3		+3	%	
Protective transistor bias	V_L		*2			
Input bias	TP	14.55	15.0	15.45	V	

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		3		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

*1 Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address–1 digit display
V_{RGL} code address–1 digit display

□ □
└ V_{SUB} address code
└ V_{RGL} address code

Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*2 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

*3 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, V_{SS}, SUB, and TP pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

*4 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

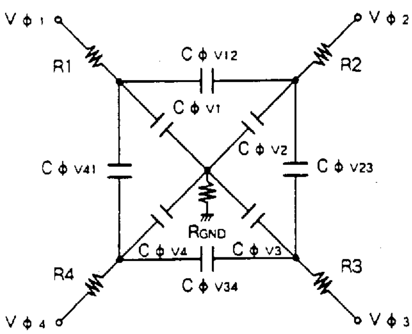
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2} V_{VH3}, V_{VH4}	–0.2	0	0.1	V	2	V_{VH}= (V_{VH1}+V_{VH2}) /2
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–9.6	–9.0	–8.5	V	2	V_{VL}= (V_{VL3}+V_{VL4}) /2
	$V\phi_V$	8.3	9.0	9.7	V	2	$V\phi_V$=V_{VHn}–V_{VLn} (n=1 to 4)
	$\|V_{VH1} - V_{VH2}\|$			0.1	V	2	
	$V_{VH3} - V_{VH}$	– 0.25		0.1	V	2	
	$V_{VH4} - V_{VH}$	– 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	4	*
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	Low level coupling
Substrate clock voltage	$V\phi_{SUB}$	23.0	24.0	25.0	V	5	

* No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

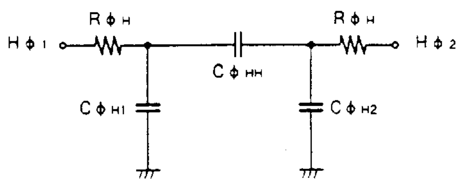
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	–0.1	0	0.1	V	4	
	$V\phi_{RG}$	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		820		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		1000		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		680		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		470		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		40		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		40		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		5		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		270		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R\phi_H$		20		Ω	



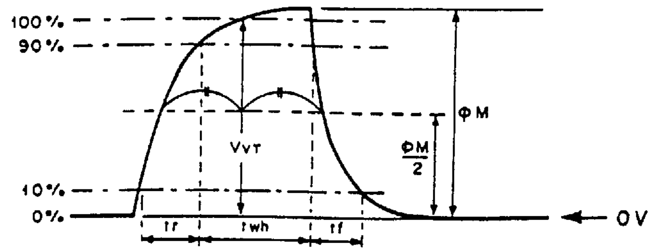
Vertical transfer clock equivalent circuit



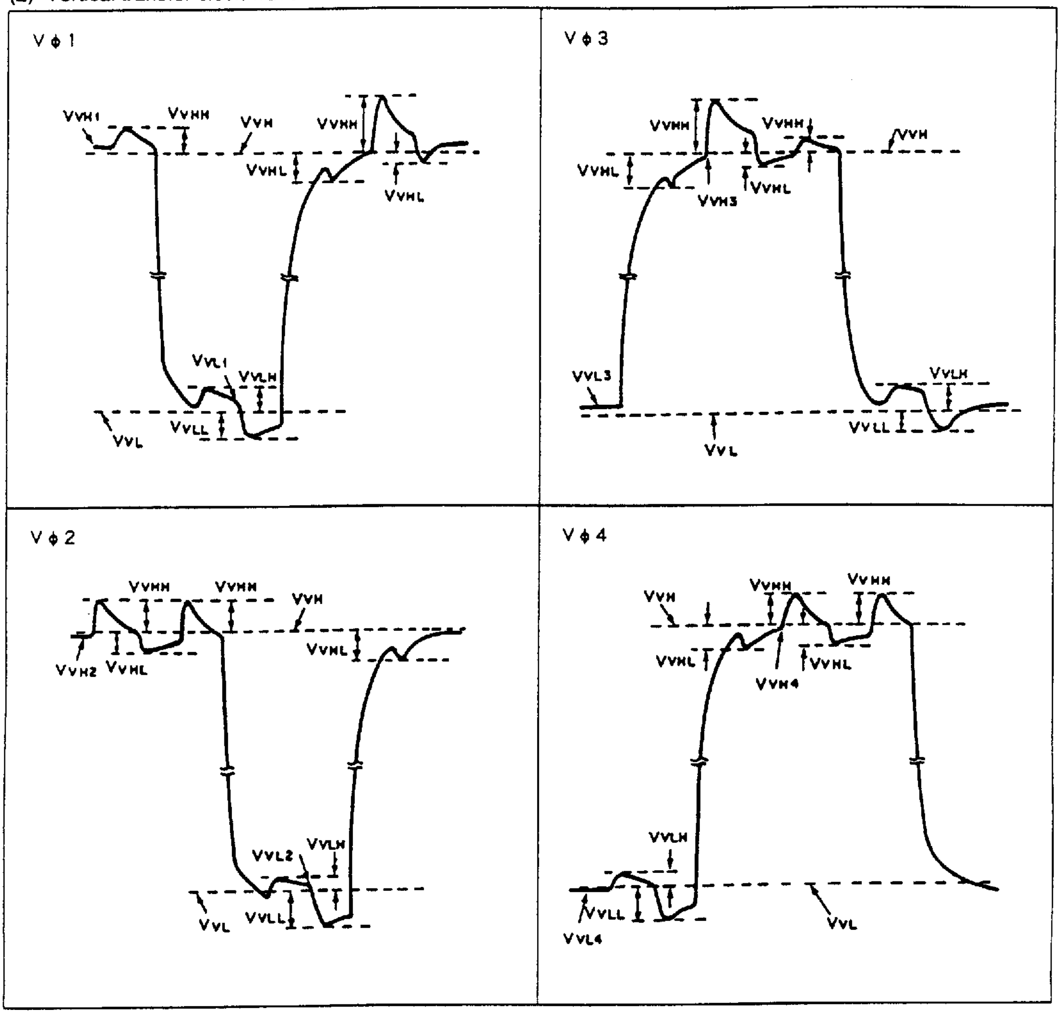
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Read out clock waveform

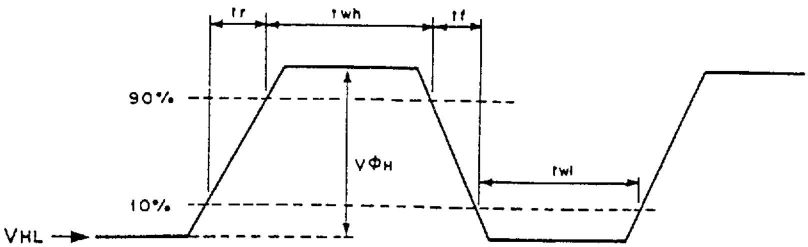


(2) Vertical transfer clock waveform

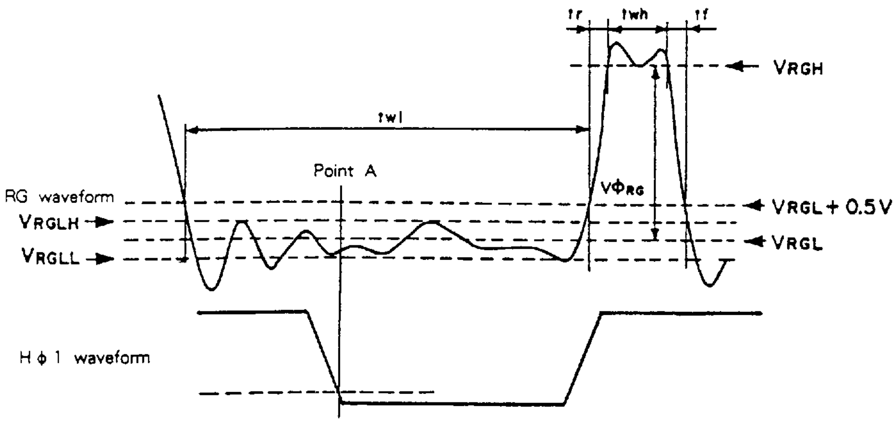


8382383 0006540 555

(3) Horizontal transfer clock waveform diagram



(4) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

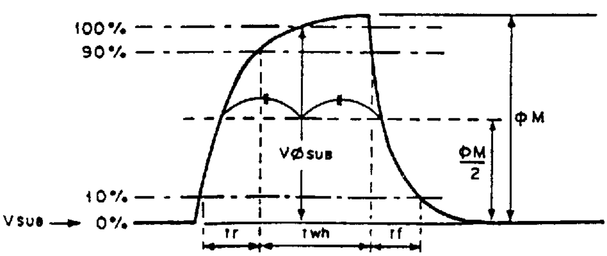
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$

V_{RGH} is the minimum value for twh period.

$V\phi_{RG} = V_{RGH} - V_{RGL}$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		µs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										0.015		0.25	µs	*1
Horizontal transfer clock	$H\phi$	37	41		38	42			12	15	*2	10	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.012		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.012		µs	
Reset gate clock	ϕ_{RG}	11	15		75	79			6.5			4.5		ns	
Substrate clock	ϕ_{SUB}	1.5	2.0							0.5			0.5	µs	During charge drain.

*1 When vertical transfer clock driver CXD1250 is in use.

*2 $tf \geqq tr - 2$ ns

Image Sensor Characteristics

(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	310	370		mV	1	
Saturation signal	Vsat	600			mV	2	Ta=60℃
Smear	Sm		0.007	0.012	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta=60℃
Dark signal shading	Δ Vdt			1	mV	6	Ta=60℃
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Chart of Video Signal Shading

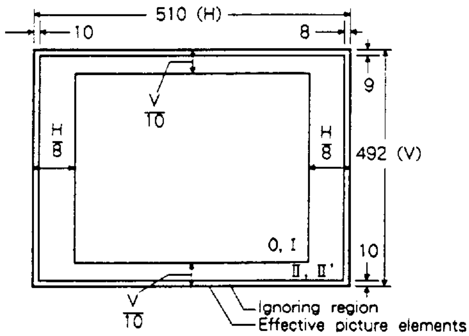


Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference for the signal output which is taken as the signal output or the chroma signal output of the testing system.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/㎡, color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F8.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
Set to standard image condition I. After selecting the electronic shutter mode at a 1/250s. shutter speed, measure the signal (Vs) at the center of the screen and substitute in the following formula.

$$S = Vs \times \frac{250}{60}$$

2. Saturation signal
Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value (V_A=180mV), then test signal minimum value.

3. Smear
Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A=180mV). Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value VSm of signal output.

$$Sm = \frac{VSm}{V_A} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A=180mV) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax) and minimum (Vmin) values of signal.

$$SH = (Vmax - Vmin) / V_A \times 100\ (\%)$$

5. Dark signal
Test signal output average value Vdt when the device ambient temperature is at 60℃ and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
Following 5, test maximum (Vdmax) and minimum (Vdmin) values of dark signal output.

$$\Delta Vdt = Vdmax - Vdmin$$

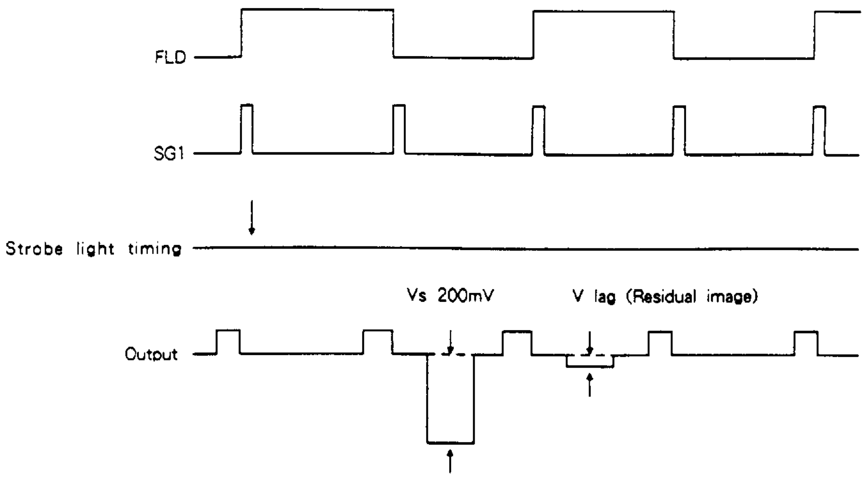
7. Flicker
Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A=180mV). Then test the signal difference (Δ Vf) between even field and odd field.

$$F = (\Delta Vf / V_A) \times 100\ (\%)$$

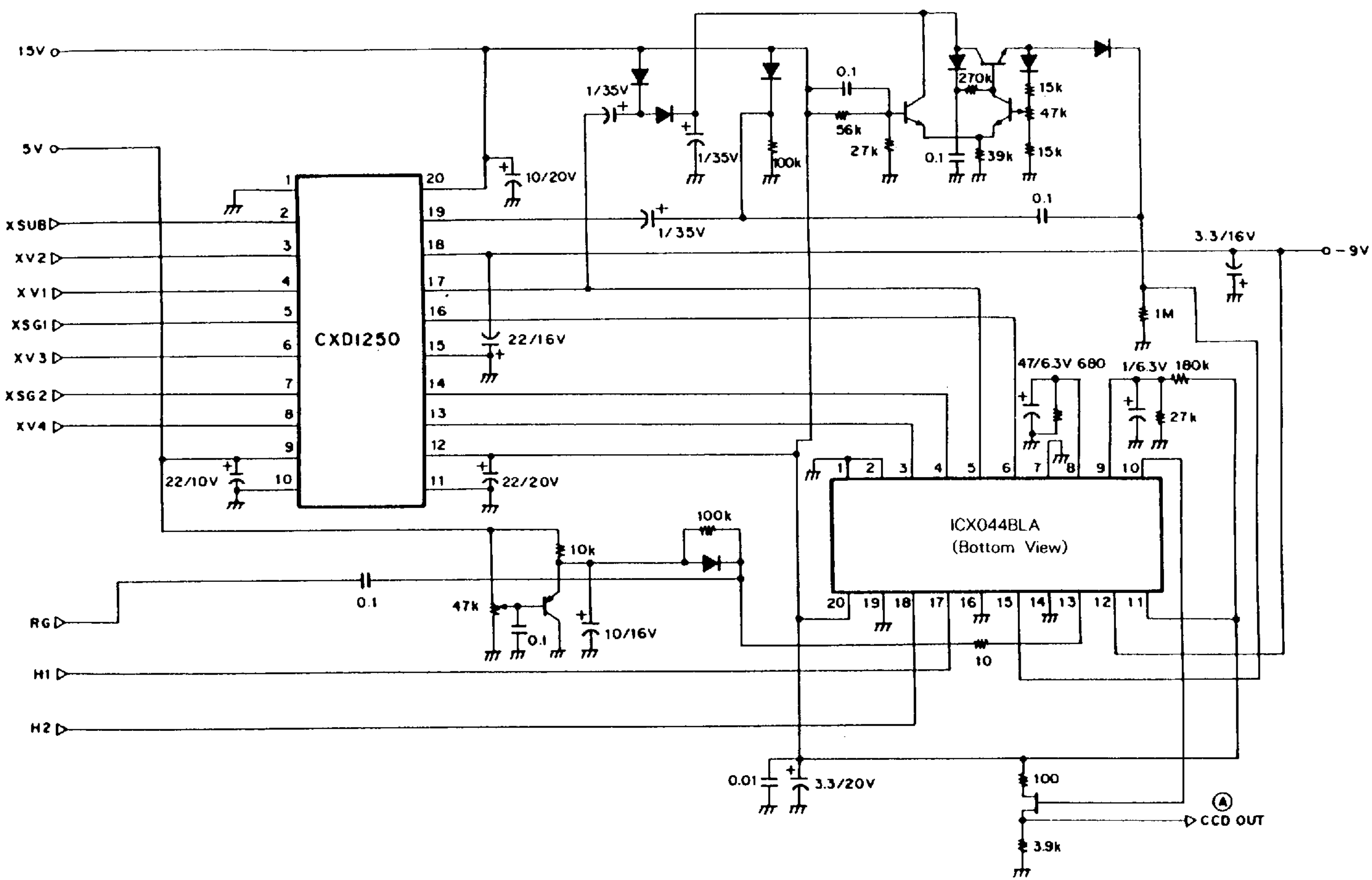
8. Residual image

Adjust signal output value (Vs) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

Lag = (Vlag/Vs) × 100 (%)



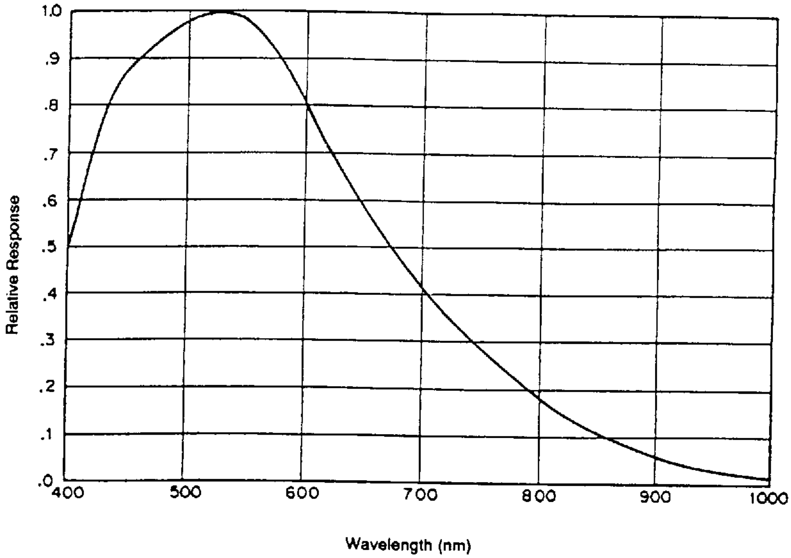
Drive Circuit



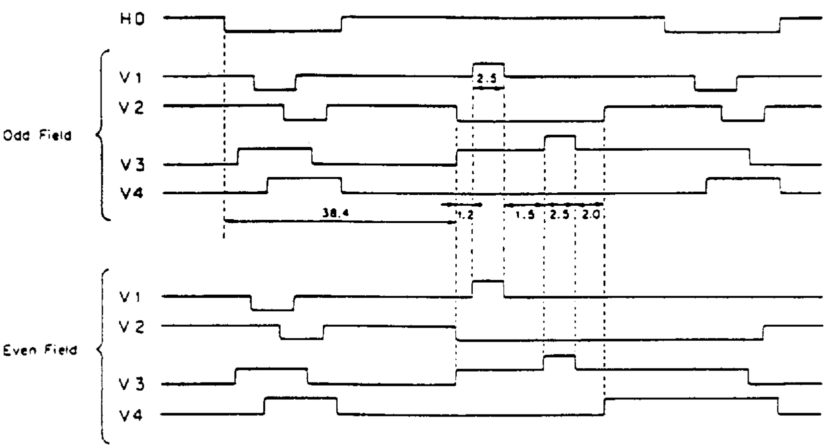
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)



Sensor Read Out Clock Timing Chart



Unit : μs

Drive Timing Chart (Vertical sync)