

Diagonal 8mm (Type 1/2) CCD Image Sensor for EIA B/W Video Cameras

**Description**

The ICX428ALB is an interline CCD solid-state image sensor suitable for EIA B/W video cameras with a diagonal 8mm (Type 1/2) system. Basic characteristics such as sensitivity, smear, dynamic range and S/N are improved drastically through the adoption of EXview HAD CCD™ technology.

This chip features a field period readout system and an electronic shutter with variable charge-storage time. Also, this outline is miniaturized by using original package. This chip is compatible with the pins of the ICX248ALB and has the same drive conditions.

EXview HAD CCD™ has different spectral characteristics from the current CCD.

**Features**

- High sensitivity
- Low smear
- High D range
- High S/N
- High resolution and low dark current
- Excellent antiblooming characteristics
- Continuous variable-speed shutter
- Substrate bias: Adjustment free (external adjustment also possible with 6 to 14V)
- Reset gate pulse: 5Vp-p adjustment free (drive also possible with 0 to 9V)
- Horizontal register: 5V drive
- Maximum package dimensions:  $\phi 13.2\text{mm}$

**Device Structure**

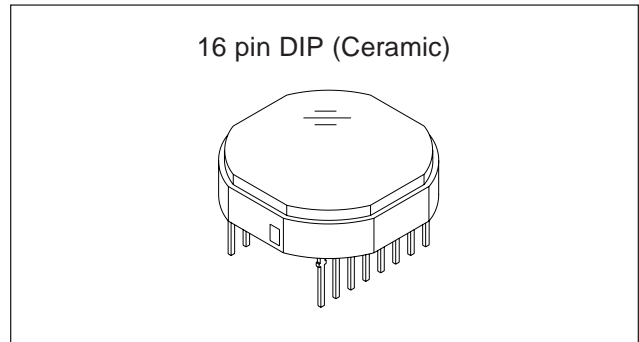
- Interline CCD image sensor
- Optical size: Diagonal 8mm (Type 1/2)
- Number of effective pixels: 768 (H)  $\times$  494 (V) approx. 380K pixels
- Total number of pixels: 811 (H)  $\times$  508 (V) approx. 410K pixels
- Chip size: 7.40mm (H)  $\times$  5.95mm (V)
- Unit cell size: 8.4 $\mu\text{m}$  (H)  $\times$  9.8 $\mu\text{m}$  (V)
- Optical black: Horizontal (H) direction: Front 3 pixels, rear 40 pixels  
Vertical (V) direction: Front 12 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 22  
Vertical 1 (even fields only)
- Substrate material: Silicon

**EXview HAD CCD™**

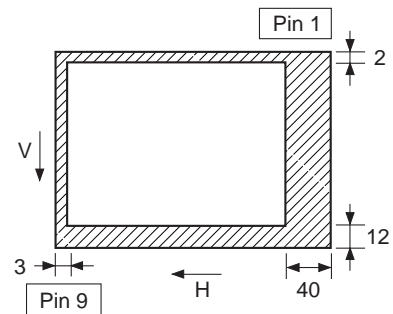
\* EXview HAD CCD is a trademark of Sony Corporation.

EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.



16 pin DIP (Ceramic)



Optical black position (Top View)

**USE RESTRICTION NOTICE (December 1, 2003 ver.)**

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the CCD products ("Products") set forth in this specifications book. Sony Corporation ("Sony") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a Sony subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of Sony on such a use restriction notice when you consider using the Products.

**Use Restrictions**

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications which may pose a life- or injury- threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your Sony sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

**Design for Safety**

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

**Export Control**

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

**No License Implied**

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that Sony and its licensors will license any intellectual property rights in such information by any implication or otherwise. Sony will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

**Governing Law**

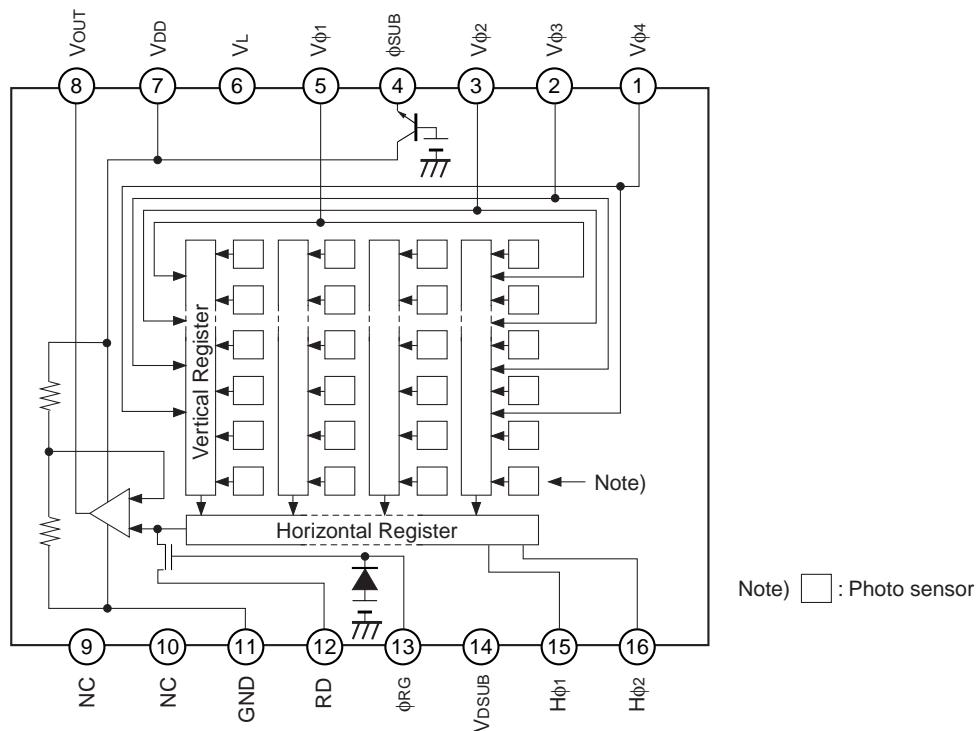
- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

**Other Applicable Terms and Conditions**

- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

**Block Diagram and Pin Configuration**

(Top View)



**Pin Description**

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	9	NC	
2	Vφ3	Vertical register transfer clock	10	NC	
3	Vφ2	Vertical register transfer clock	11	GND	GND
4	φSUB	Substrate clock	12	RD	Reset drain bias
5	Vφ1	Vertical register transfer clock	13	φRG	Reset gate clock
6	VL	Protective transistor bias	14	VDSUB	Substrate bias circuit supply voltage
7	VDD	Output circuit supply voltage	15	Hφ1	Horizontal register transfer clock
8	VOUT	Signal output	16	Hφ2	Horizontal register transfer clock

## Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate clock $\phi_{SUB} - GND$		-0.3 to +50	V	
Supply voltage	$V_{DD}, V_{RD}, V_{DSUB}, V_{OUT} - GND$	-0.3 to +18	V	
	$V_{DD}, V_{RD}, V_{DSUB}, V_{OUT} - \phi_{SUB}$	-55 to +10	V	
Clock input voltage	$V\phi_1, V\phi_2, V\phi_3, V\phi_4 - GND$	-15 to +20	V	
	$V\phi_1, V\phi_2, V\phi_3, V\phi_4 - \phi_{SUB}$	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*1
Voltage difference between horizontal clock input pins		to +17	V	
$H\phi_1, H\phi_2 - V\phi_4$		-17 to +17	V	
$\phi_{RG} - GND$		-10 to +15	V	
$\phi_{RG} - \phi_{SUB}$		-55 to +10	V	
$V_L - \phi_{SUB}$		-65 to +0.3	V	
Pins other than GND and $\phi_{SUB} - V_L$		-0.3 to +30	V	
Storage temperature		-30 to +80	°C	
Operating temperature		-10 to +60	°C	

\*1 +27V (Max.) when clock width < 10 $\mu$ s, clock duty factor < 0.1%.

**Bias Conditions 1 [when used in substrate bias internal generation mode]**

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit supply voltage	V <sub>DD</sub>	14.55	15.0	15.45	V	
Reset drain voltage	V <sub>RD</sub>	14.55	15.0	15.45	V	V <sub>RD</sub> = V <sub>DD</sub>
Protective transistor bias	V <sub>L</sub>	*1				
Substrate bias circuit supply voltage	V <sub>DSUB</sub>	14.55	15.0	15.45	V	
Substrate clock	φ <sub>SUB</sub>	*2				

\*1 V<sub>L</sub> setting is the V<sub>L</sub> voltage of the vertical transfer clock waveform, or the same supply voltage as the V<sub>L</sub> power supply for the V driver should be used. (When CXD1267AN is used.)

\*2 Do not apply a DC bias to the substrate clock pin, because a DC bias is generated within the CCD.

**Bias Conditions 2 [when used in substrate bias external adjustment mode]**

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit supply voltage	V <sub>DD</sub>	14.55	15.0	15.45	V	
Reset drain voltage	V <sub>RD</sub>	14.55	15.0	15.45	V	V <sub>RD</sub> = V <sub>DD</sub>
Protective transistor bias	V <sub>L</sub>	*3				
Substrate bias circuit supply voltage	V <sub>DSUB</sub>	*4				
Substrate voltage adjustment range	V <sub>SUB</sub>	6.0		14.0	V	*5
Substrate voltage adjustment precision	ΔV <sub>SUB</sub>	-3		+3	%	*5

\*3 V<sub>L</sub> setting is the V<sub>L</sub> voltage of the vertical transfer clock waveform, or the same supply voltage as the V<sub>L</sub> power supply for the V driver should be used. (When CXD1267AN is used.)

\*4 Connect to GND or leave open.

\*5 The setting value of the substrate voltage (V<sub>SUB</sub>) is indicated on the back of the image sensor by a special code. When adjusting the substrate voltage externally, adjust the substrate voltage to the indicated voltage. The adjustment precision is ±3%. However, this setting value has not significance when used in substrate bias internal generation mode.

V<sub>SUB</sub> code — one character indication

Code and optimal setting correspond to each other as follows.

V <sub>SUB</sub> code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W
Optimal setting	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0

<Example> "L" → V<sub>SUB</sub> = 9.0V

**DC Characteristics**

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit supply current	I <sub>DD</sub>		5.0	10.0	mA	

**Clock Voltage Conditions**

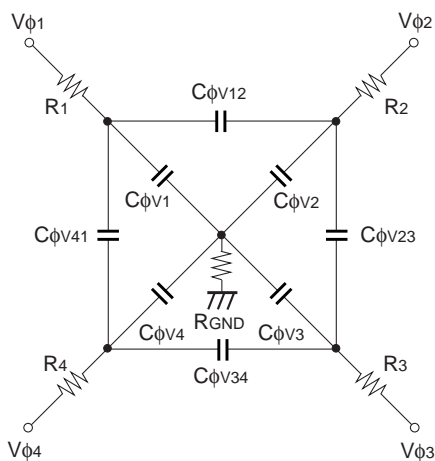
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V <sub>VT</sub>	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V <sub>VH1</sub> , V <sub>VH2</sub>	-0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V <sub>VH3</sub> , V <sub>VH4</sub>	-0.2	0	0.05	V	2	
	V <sub>VL1</sub> , V <sub>VL2</sub> , V <sub>VL3</sub> , V <sub>VL4</sub>	-9.6	-9.0	-8.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	V <sub>φV</sub>	8.3	9.0	9.65	Vp-p	2	$V_{φV} = V_{VHn} - V_{VLn} (n = 1 \text{ to } 4)$
	V <sub>VH1</sub> - V <sub>VH2</sub>			0.1	V	2	
	V <sub>VH3</sub> - V <sub>VH</sub>	-0.25		0.1	V	2	
	V <sub>VH4</sub> - V <sub>VH</sub>	-0.25		0.1	V	2	
	V <sub>VHH</sub>			0.5	V	2	High-level coupling
	V <sub>VHL</sub>			0.5	V	2	High-level coupling
	V <sub>VLH</sub>			0.5	V	2	Low-level coupling
	V <sub>VLL</sub>			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	V <sub>φH</sub>	4.75	5.0	5.25	Vp-p	3	
	V <sub>H</sub> L	-0.05	0	0.05	V	3	
Reset gate clock voltage*1	V <sub>RGL</sub>	*1			V	4	
	V <sub>φRG</sub>	4.5	5.0	5.5	Vp-p	4	
	V <sub>RGLH</sub> - V <sub>RGLL</sub>			0.8	V	4	Low-level coupling
Substrate clock voltage	V <sub>φSUB</sub>	23.0	24.0	25.0	Vp-p	5	

\*1 Input the reset gate clock without applying a DC bias. In addition, the reset gate clock can also be driven with the following specifications.

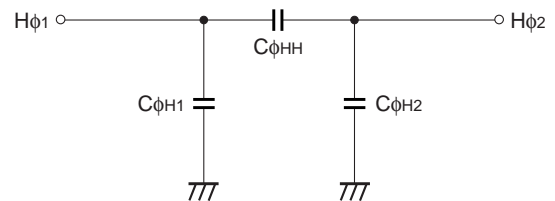
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V <sub>RGL</sub>	-0.2	0	0.2	V	4	
	V <sub>φRG</sub>	8.5	9.0	9.5	Vp-p	4	

**Clock Equivalent Circuit Constant**

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1, C\phi V3$		2700		pF	
	$C\phi V2, C\phi V4$		2700		pF	
Capacitance between vertical transfer clocks	$C\phi V12, C\phi V34$		820		pF	
	$C\phi V23, C\phi V41$		330		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1$		100		pF	
	$C\phi H2$		91		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		47		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		11		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		680		pF	
Vertical transfer clock series resistor	$R1, R3$		91		$\Omega$	
	$R2, R4$		100		$\Omega$	
Vertical transfer clock ground resistor	$R_{GND}$		68		$\Omega$	



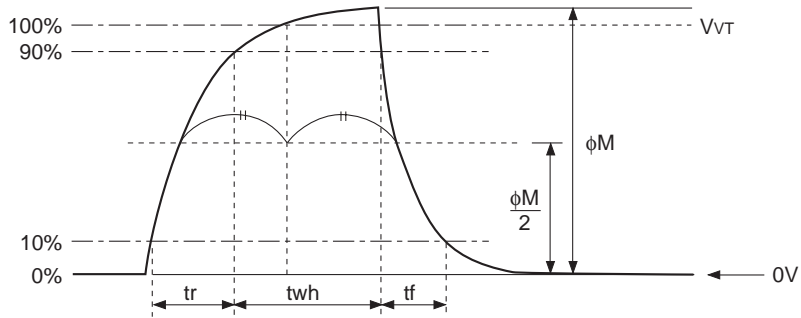
**Vertical transfer clock equivalent circuit**



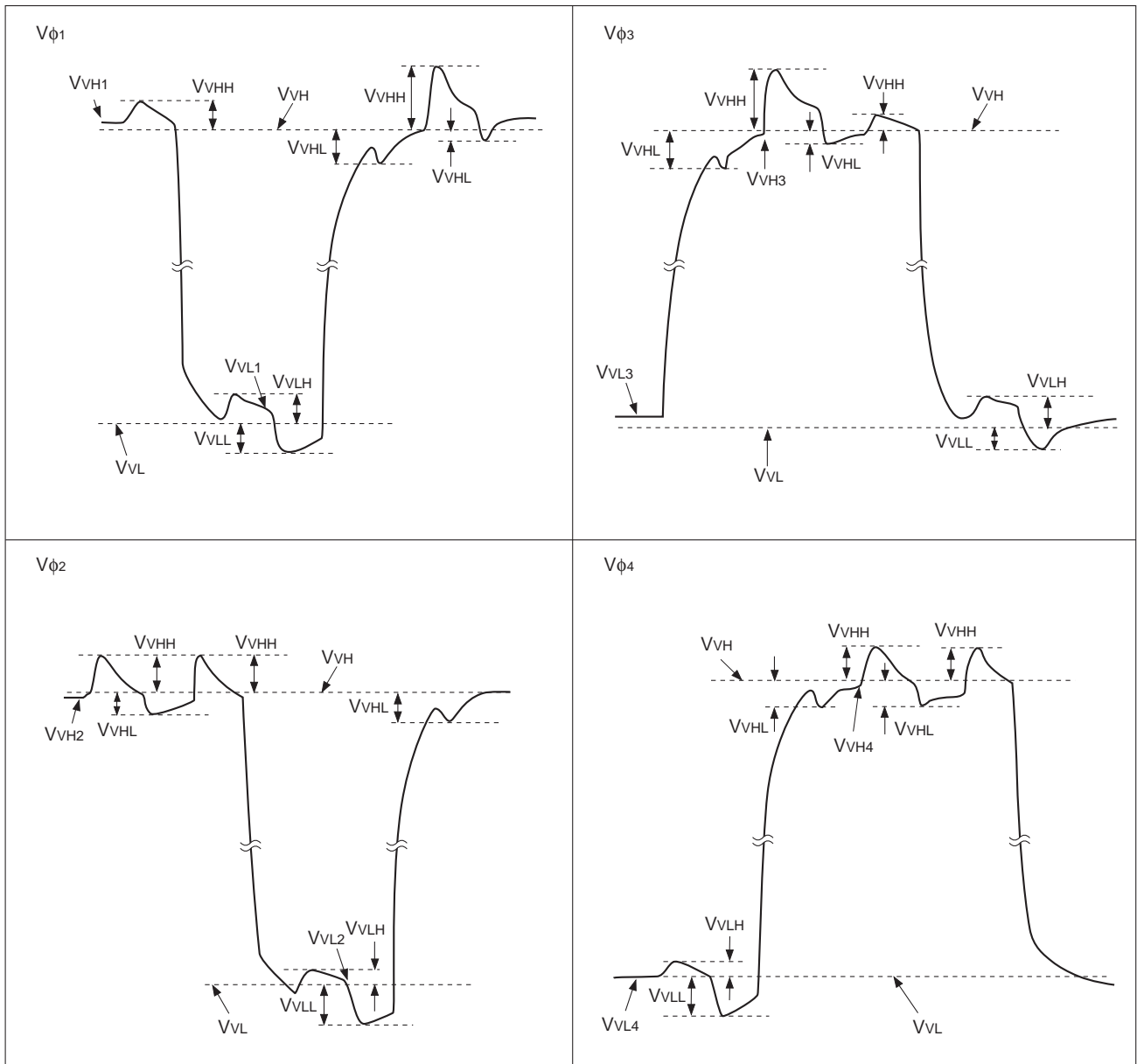
**Horizontal transfer clock equivalent circuit**

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform



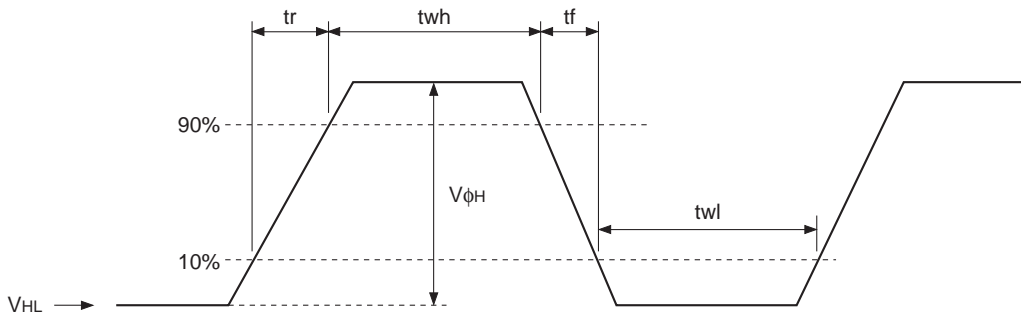
$$V_{vH} = (V_{vH1} + V_{vH2})/2$$

$$V_{vL} = (V_{vL3} + V_{vL4})/2$$

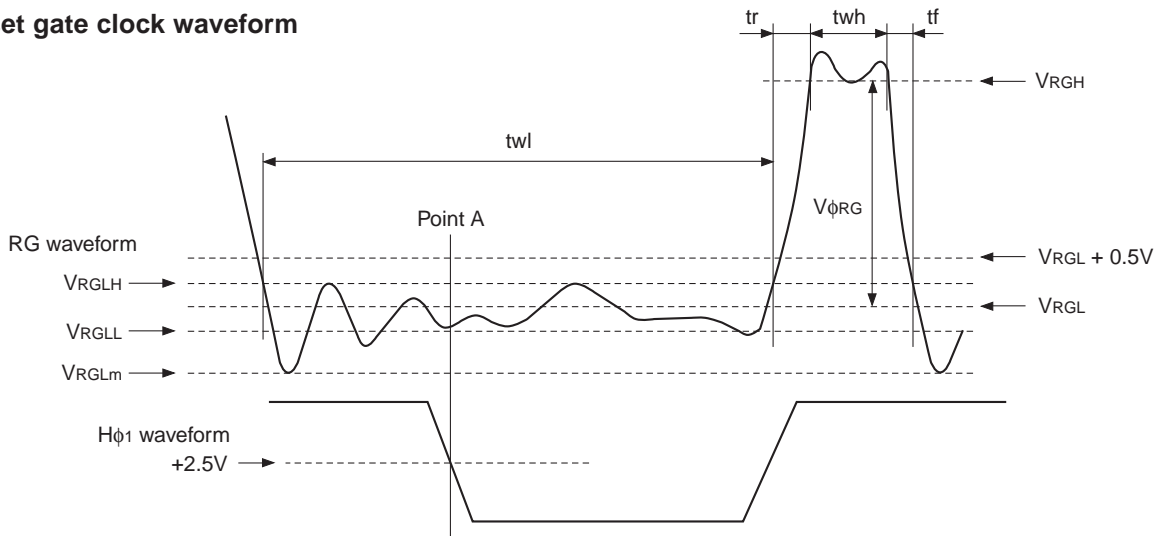
$$V_{\phi V} = V_{vHn} - V_{vLn} \quad (n = 1 \text{ to } 4)$$



**(3) Horizontal transfer clock waveform**



**(4) Reset gate clock waveform**



$V_{RGLH}$  is the maximum value and  $V_{RGLL}$  is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition,  $V_{RGL}$  is the average value of  $V_{RGLH}$  and  $V_{RGLL}$ .

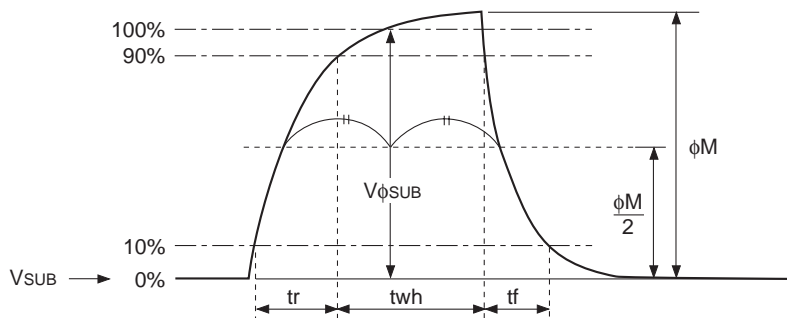
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming  $V_{RGH}$  is the minimum value during the period  $t_{wh}$ , then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is  $V_{RGLm}$ .

**(5) Substrate clock waveform**



**Clock Switching Characteristics**

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V <sub>T</sub>	2.3	2.5					0.5			0.5			μs	During readout
Vertical transfer clock	V <sub>φ1</sub> , V <sub>φ2</sub> , V <sub>φ3</sub> , V <sub>φ4</sub>										15		250	ns	*1
Horizontal transfer clock	During imaging	H <sub>φ</sub>	20			20			15	19		15	19	ns	*2
	During parallel-serial conversion	H <sub>φ1</sub>	5.38					0.01			0.01			μs	
		H <sub>φ2</sub>				5.38			0.01			0.01			
Reset gate clock	φ <sub>RG</sub>	11	13			51			3			3		ns	
Substrate clock	φ <sub>SUB</sub>	1.5	1.8							0.5			0.5	μs	When draining charge

\*1 When vertical transfer clock driver CXD1267AN is used.

\*2  $tf \geq tr - 2ns$ .

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H <sub>φ1</sub> , H <sub>φ2</sub>	16	20		ns	*3

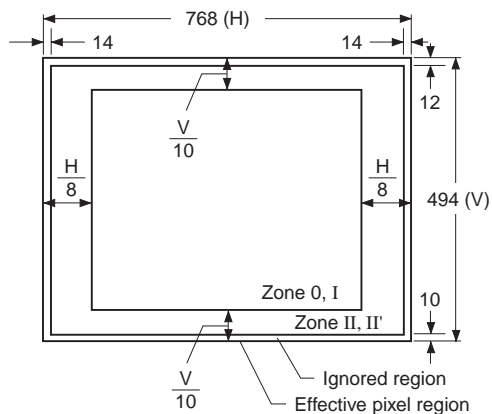
\*3 The overlap period for twh and twl of horizontal transfer clocks H<sub>φ1</sub> and H<sub>φ2</sub> is two.

**Image Sensor Characteristics**

(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity1	S1	1120	1400		mV	1	
Sensitivity2	S2	4500	5500		mV	2	
Saturation signal	Vsat	1000			mV	3	Ta = 60°C
Smear	Sm		-126	-115	dB	4	
Video signal shading	SH			20	%	5	Zone 0 and I
				25	%	5	Zone 0 to II'
Dark signal	Vdt			2	mV	6	Ta = 60°C
Dark signal shading	$\Delta Vdt$			1	mV	7	Ta = 60°C
Flicker	F			2	%	8	
Lag	Lag			0.5	%	9	

**Zone Definition of Video Signal Shading**



## Image Sensor Characteristics Measurement Method

### ◎ Measurement conditions

- 1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions. (when used with substrate bias external adjustment, set the substrate voltage to the value indicated on the device.)
- 2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of Y signal output or chroma signal output of the measurement system.

### ◎ Definition of standard imaging conditions

- 1) Standard imaging condition I:  
Use a pattern box (luminance 706cd/m<sup>2</sup>, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.4mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.
- 2) Standard imaging condition II:  
This indicates the standard imaging condition I with the IR cut filter removed.
- 3) Standard imaging condition III:  
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens and the luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm. (IR cut filter is not applicable.)

#### 1. Sensitivity1

Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output ( $V_{S1}$ ) at the center of the screen and substitute the value into the following formula.

$$S1 = V_{S1} \times \frac{250}{60} \text{ [mV]}$$

#### 2. Sensitivity2

Set to standard imaging condition II. After selecting the electronic shutter mode with a shutter speed of 1/1000s, measure the signal output ( $V_{S2}$ ) at the center of the screen and substitute the value into the following formula.

$$S2 = V_{S2} \times \frac{1000}{60} \text{ [mV]}$$

#### 3. Saturation signal

Set to standard imaging condition III. After adjusting the luminous intensity to 10 times the intensity with average value of the signal output, 200mV, measure the minimum value of the signal output.

4. Smear

Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of the signal output, 200mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value VSm [mV] of the signal output and substitute the value into the following formula.

$$S_m = 20 \times \log \left( \frac{V_{Sm}}{200} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB]} \text{ (1/10V method conversion value)}$$

5. Video signal shading

Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 200mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (V_{max} - V_{min}) / 200 \times 100 \text{ [%]}$$

6. Dark signal

Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading

After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta V_{dt} = V_{dmax} - V_{dmin} \text{ [mV]}$$

8. Flicker

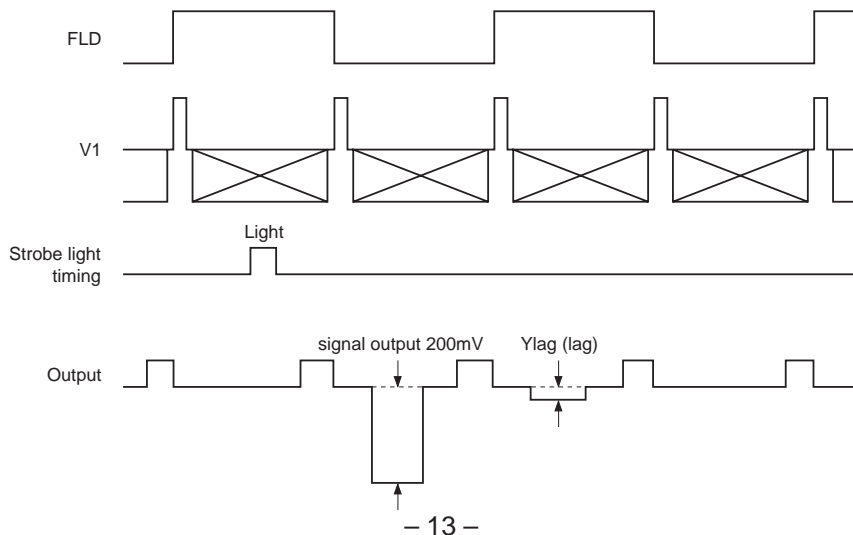
Set to standard imaging condition III. Adjust the luminous intensity so that the average value of the signal output is 200mV, and then measure the difference in the signal level between fields ( $\Delta V_f$  [mV]). Then substitute the value into the following formula.

$$F_y = (\Delta V_f / 200) \times 100 \text{ [%]}$$

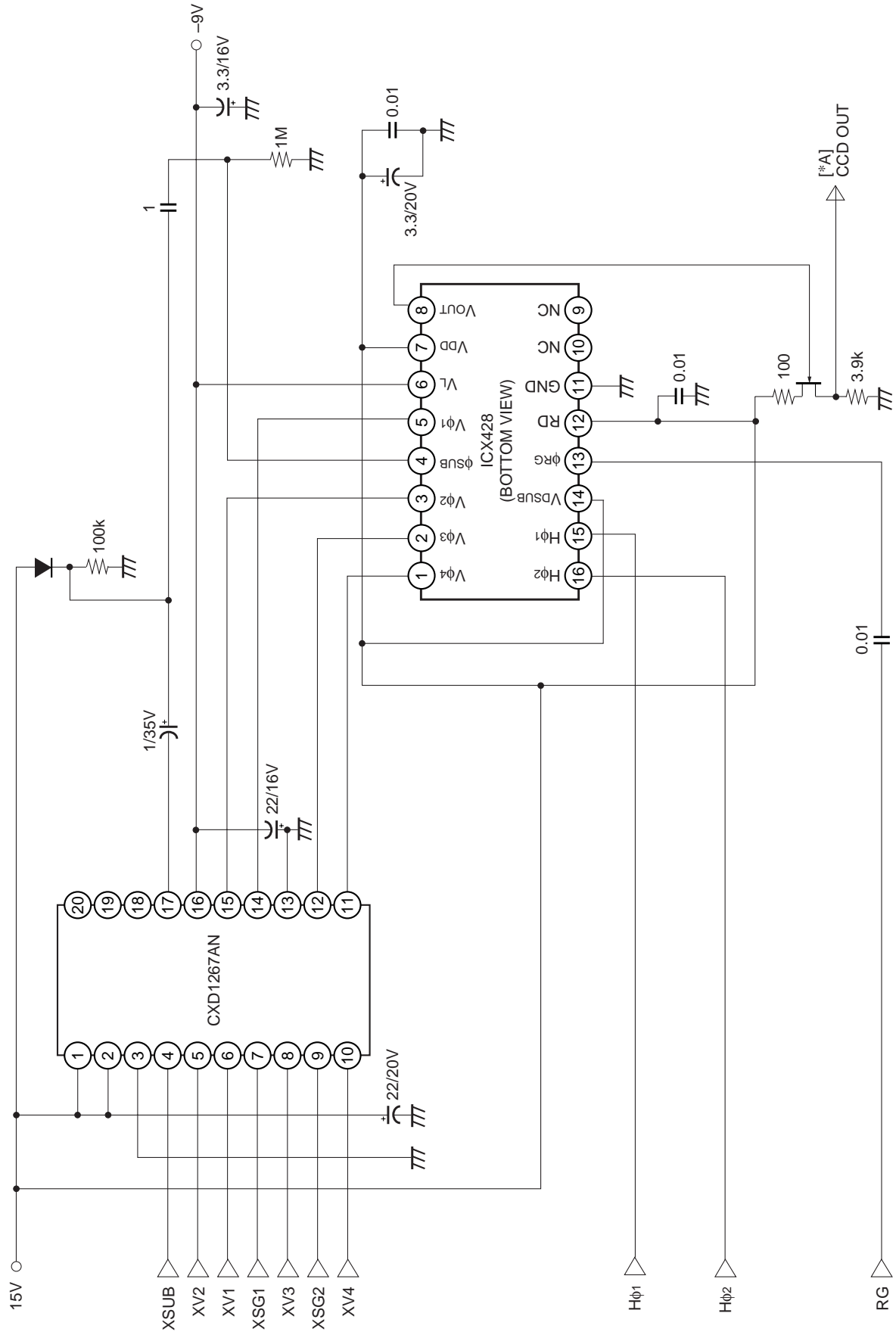
9. Lag

Adjust the signal output value generated by strobe light to 200mV. After setting the strobe light so that it strobos with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

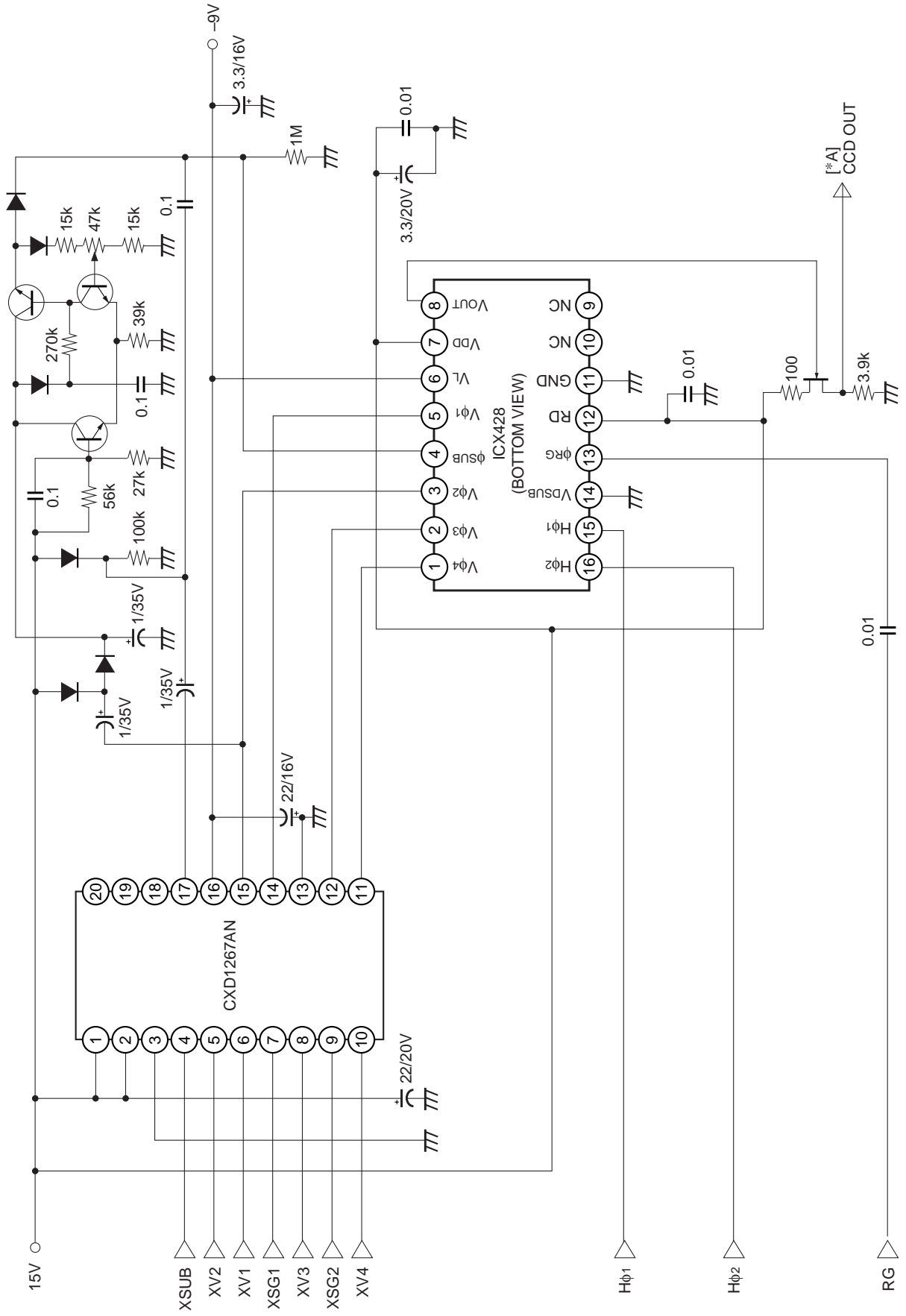
$$Lag = (V_{lag} / 200) \times 100 \text{ [%]}$$



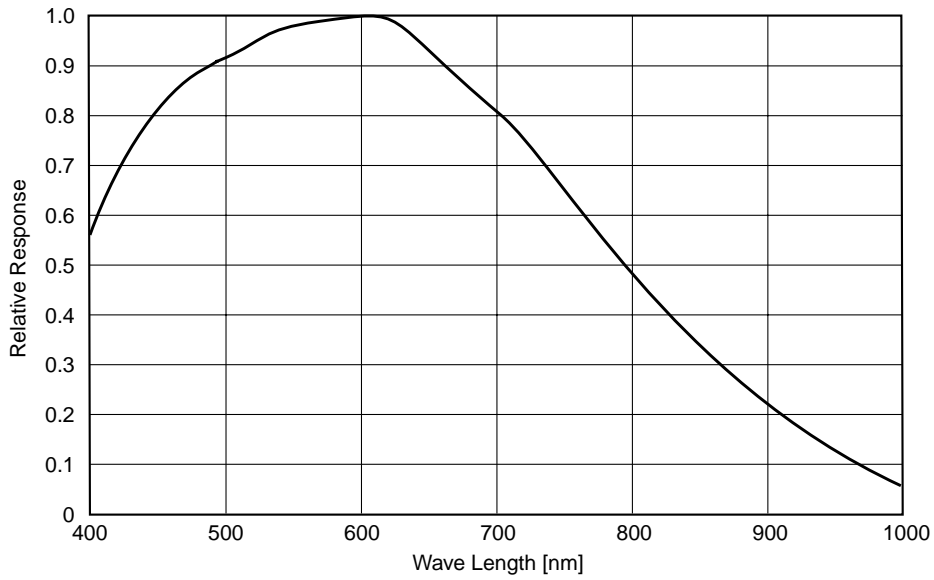
Drive Circuit 1 (substrate bias internal generation mode)



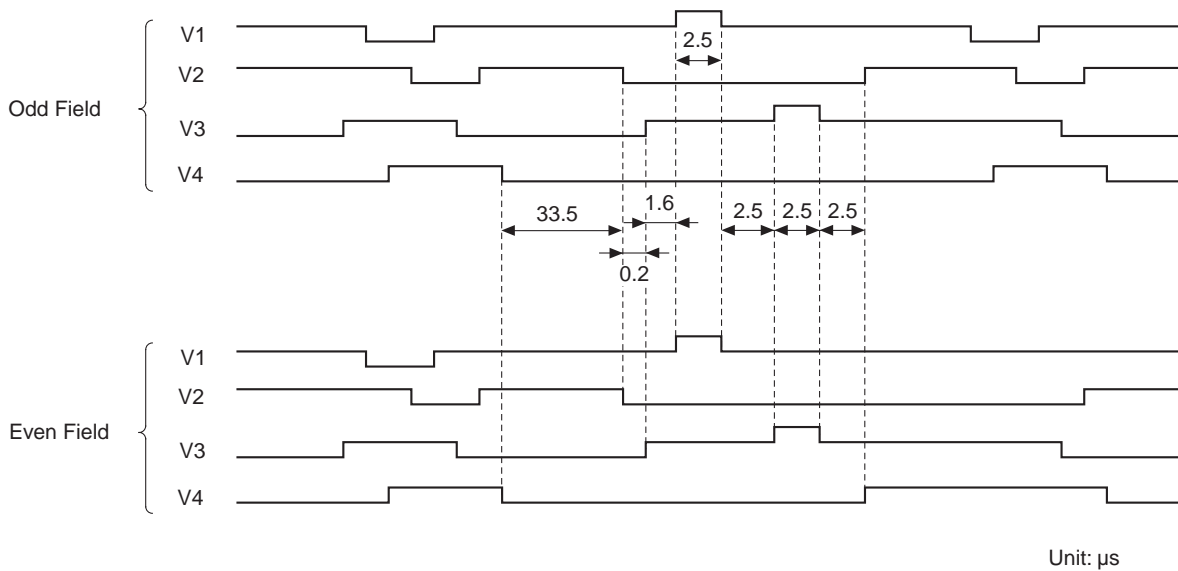
Drive Circuit 2 (substrate bias external adjustment mode)



**Spectral Sensitivity Characteristics** (Excludes lens characteristics and light source characteristics)

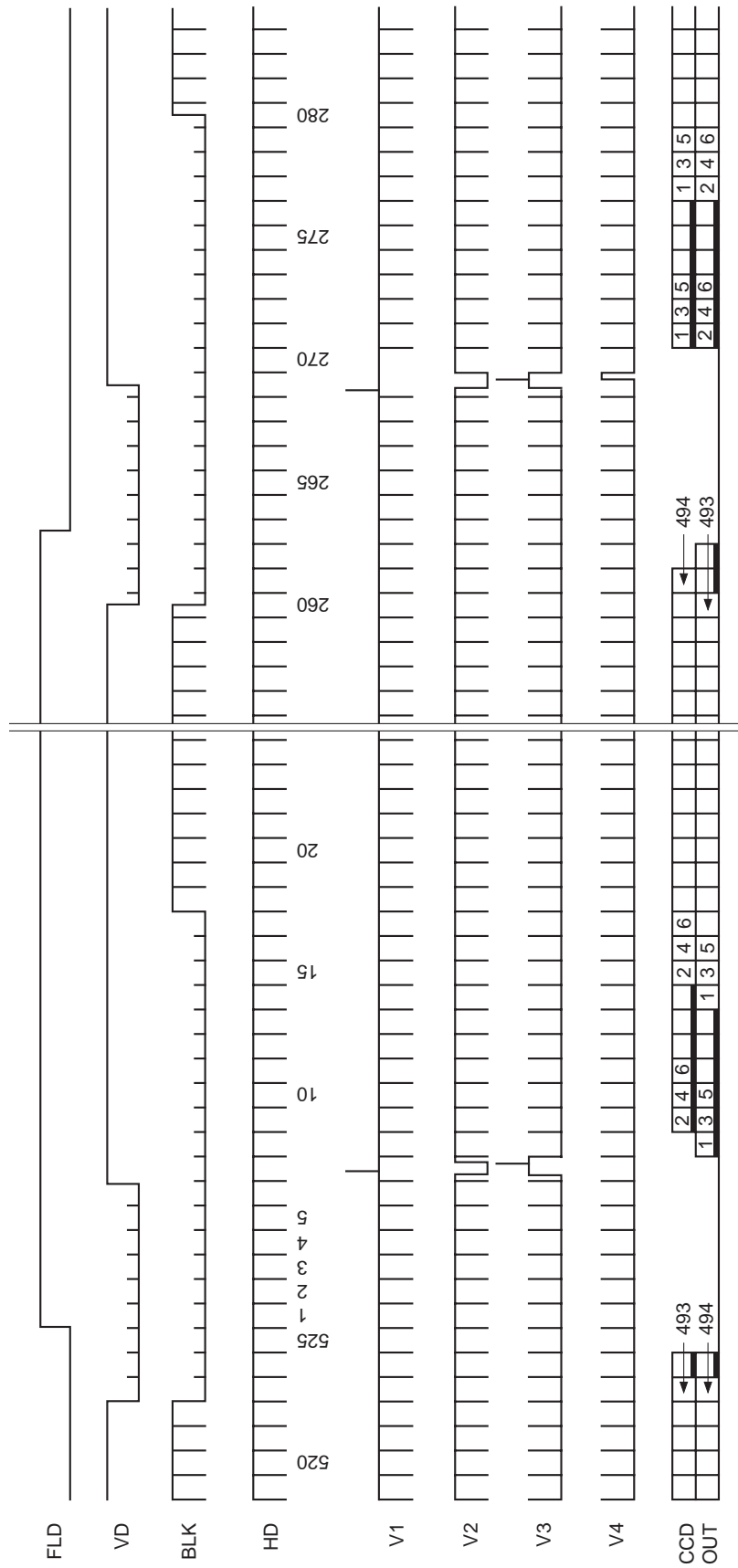


**Sensor Readout Clock Timing Chart**

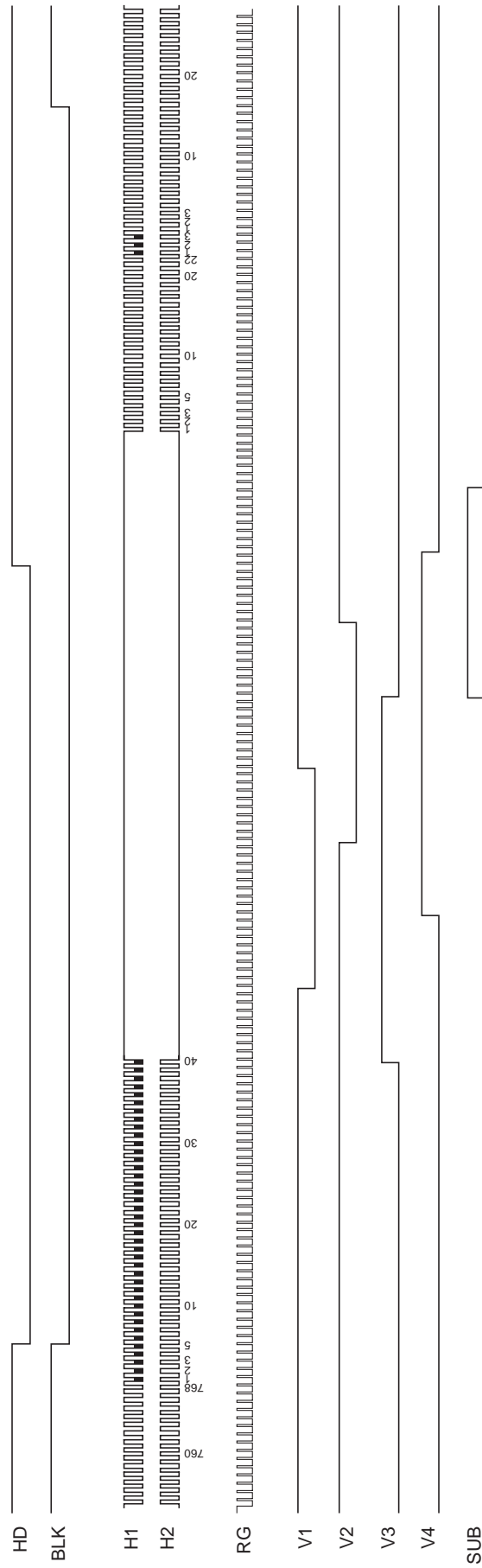




Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



## Notes on Handling

### 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material.  
Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

### 2) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

### 3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.

- a) Perform all assembly operations in a clean room (class 1000 or less).
- b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

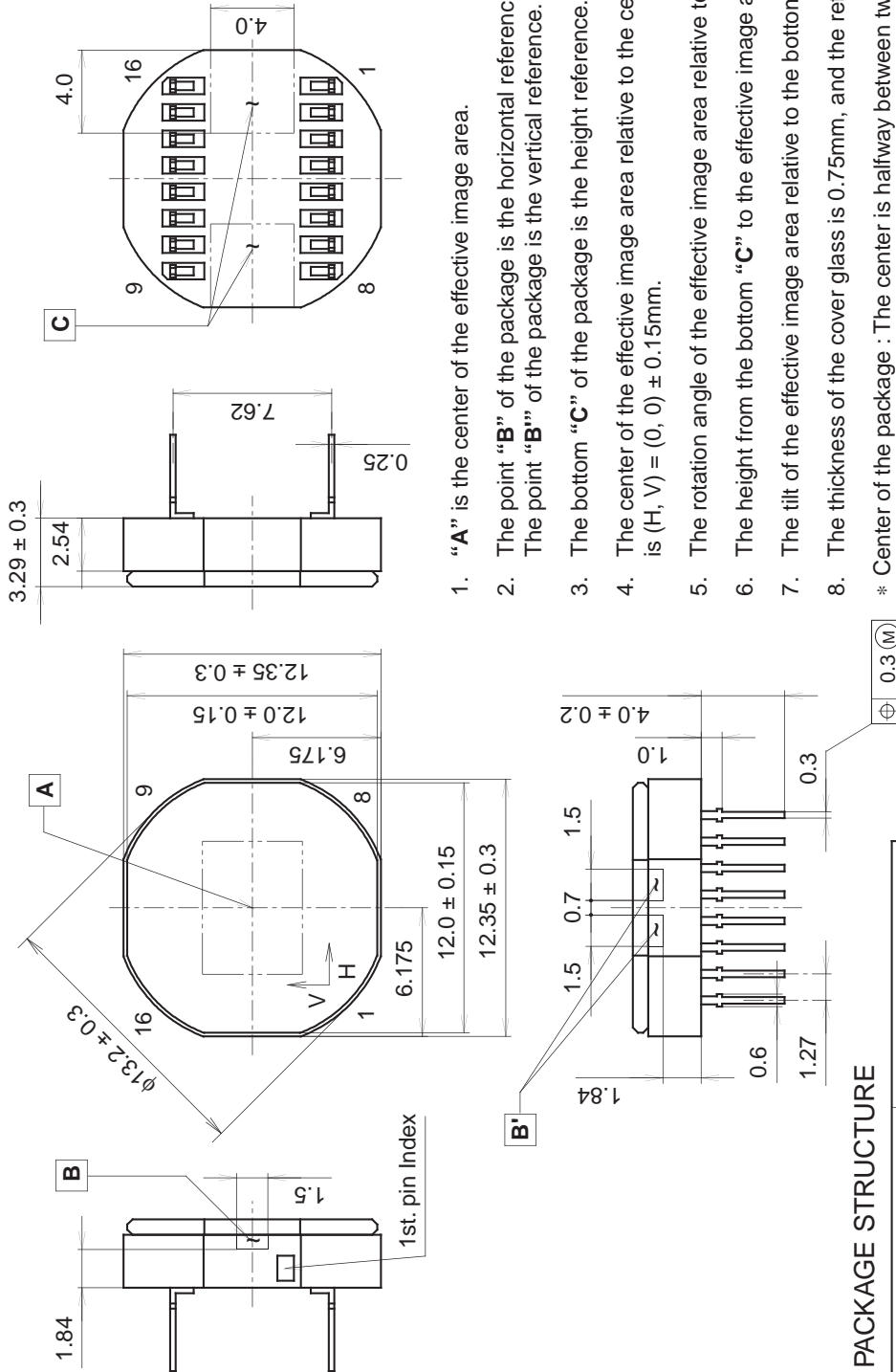
4) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm

16 pin DIP (300mil)



1. "A" is the center of the effective image area.
2. The point "B" of the package is the horizontal reference. The point "B'" of the package is the vertical reference.
3. The bottom "C" of the package is the height reference.
4. The center of the effective image area relative to the center of the package (\*) is  $(H, V) = (0, 0) \pm 0.15$ mm.
5. The rotation angle of the effective image area relative to H and V is  $\pm 1^\circ$ .
6. The height from the bottom "C" to the effective image area is  $1.41 \pm 0.15$ mm.
7. The tilt of the effective image area relative to the bottom "C" is less than  $60\mu$ m.
8. The thickness of the cover glass is  $0.75$ mm, and the refractive index is  $1.5$ .

\* Center of the package : The center is halfway between two pairs of opposite sides, as measured from "B", "B'".

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.90g
DRAWING NUMBER	AS-B4-01(E)