SONY

Diagonal 6.0mm (Type 1/3) Progressive Scan CCD Image Sensor for Color Cameras

ICX445AQA

Description

The ICX445AQA is a diagonal 6.0mm (Type 1/3) interline CCD solid-state image sensor with a square pixel array and 1.25M effective pixels.
Progressive scan enables all pixel signals to be output separately within 1/22.5 second.
The sensitivity and smear are improved drastically through the adoption of EXview HAD CCD technology.

Features

- ◆ Supports following modes
  All-pixel scan mode (15 frame/s, 12.5 frame/s, 22.5 frame/s: MAX)
  Center cut-out mode (30 frame/s, 25 frame/s)
- ◆ Horizontal drive frequency: 36.0MHz, 29.0MHz
- ◆ R, G, B primary color filters on chip
- ◆ High resolution, high sensitivity, low dark current, low smear
- ◆ Excellent anti-blooming characteristics
- ◆ No voltage adjustments (Reset gate and substrate bias need no adjustment.)
- ◆ 24-pin high precision plastic package (Dual-surface reference available)

Package

24-pin DIP (Plastic)

EXview HAD CCD™

* EXview HAD CCD is a trademark of Sony Corporation. The EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a basic structure of HAD (Hole-Accumulation Diode) sensor.

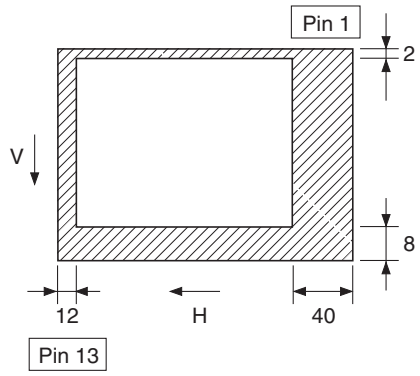
E06228D0X

Element Structure

- ◆ Interline CCD image sensor
- ◆ Image size
  Diagonal 6.0mm (Type 1/3)
- ◆ Total number of pixels
  1348 (H) × 976 (V) approx. 1.32M pixels
- ◆ Number of effective pixels
  1296 (H) × 966 (V) approx. 1.25M pixels
- ◆ Number of active pixels
  1280 (H) × 960 (V) approx. 1.23M pixels
- ◆ Chip size
  6.26mm (H) × 5.01mm (V)
- ◆ Unit cell size
  3.75μm (H) × 3.75μm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 12 pixels, rear 40 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- ◆ Number of dummy bits
  Horizontal (H) direction: Front 4 pixels
  Vertical (V) direction: Front 2 pixels
- ◆ Substrate material
  Silicon

Optical Black Position

(Top View)



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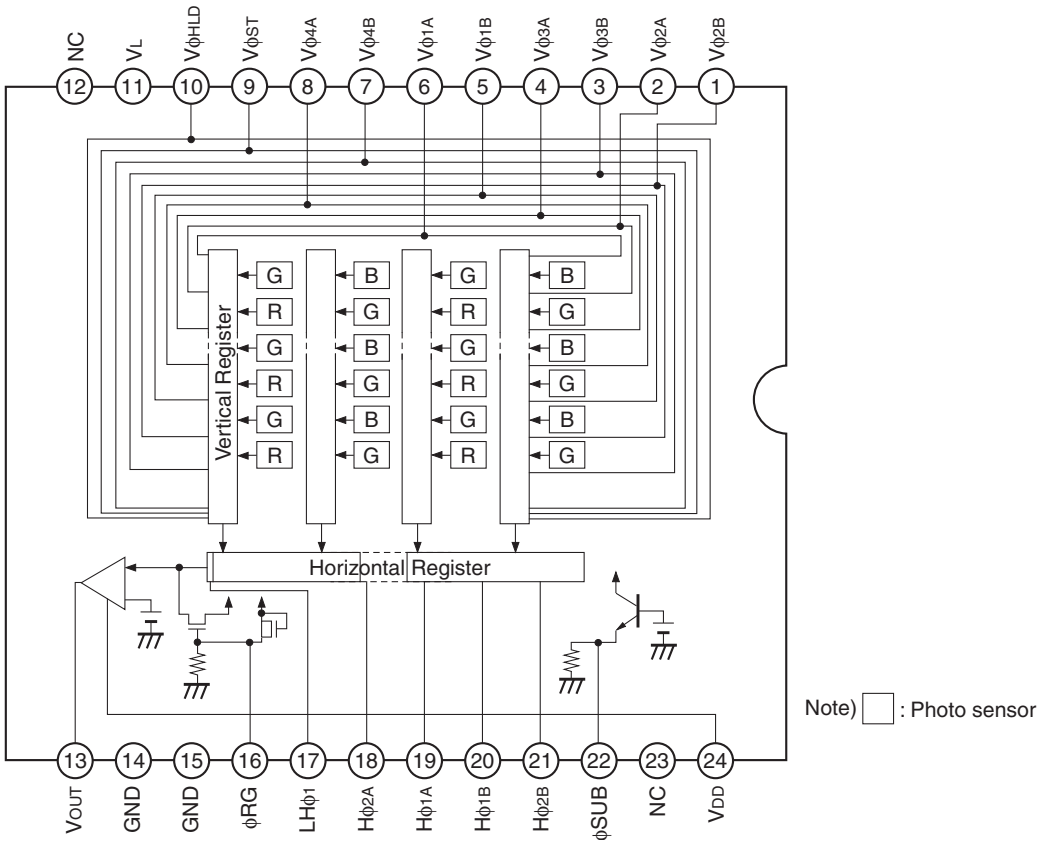
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ2B	Vertical register transfer clock	13	VOUT	Signal output
2	Vφ2A	Vertical register transfer clock	14	GND	GND
3	Vφ3B	Vertical register transfer clock	15	GND	GND
4	Vφ3A	Vertical register transfer clock	16	φRG	Reset gate clock
5	Vφ1B	Vertical register transfer clock	17	LHφ1	Horizontal register final stage transfer clock
6	Vφ1A	Vertical register transfer clock	18	Hφ2A	Horizontal register transfer clock
7	Vφ4B	Vertical register transfer clock	19	Hφ1A	Horizontal register transfer clock
8	Vφ4A	Vertical register transfer clock	20	Hφ1B	Horizontal register transfer clock
9	VφST	Horizontal addition control clock	21	Hφ2B	Horizontal register transfer clock
10	VφHLD	Horizontal addition control clock	22	φSUB	Substrate clock
11	VL	Protective transistor bias	23	NC	
12	NC		24	VDD	Supply voltage

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against ϕSUB	V_{DD}, V_{OUT}, ϕRG – ϕSUB	–39 to +12	V	
	$V\phi_{2A}$, $V\phi_{2B}$, $V\phi_{3A}$, $V\phi_{3B}$ – ϕSUB	–46 to +17	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{4A}$, $V\phi_{4B}$, $V\phi_{ST}$, $V\phi_{HLD}$, V_L – ϕSUB	–46 to +0.3	V	
	$H\phi_{1A}$, $H\phi_{1B}$, $H\phi_{2A}$, $H\phi_{2B}$, $LH\phi_1$, GND – ϕSUB	–39 to +0.3	V	
Against GND	V_{DD}, V_{OUT}, ϕRG – GND	–0.3 to +20	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_{4A}$, $V\phi_{4B}$, $V\phi_{ST}$, $V\phi_{HLD}$ – GND	–9.0 to +17	V	
	$H\phi_{1A}$, $H\phi_{1B}$, $H\phi_{2A}$, $H\phi_{2B}$, $LH\phi_1$ – GND	–9.0 to +4.2	V	
Against V_L	$V\phi_{2A}$, $V\phi_{2B}$, $V\phi_{3A}$, $V\phi_{3B}$ – V_L	–0.3 to +25	V	
	$V\phi_{1A}$, $V\phi_{1B}$, $V\phi_{4A}$, $V\phi_{4B}$, $V\phi_{ST}$, $V\phi_{HLD}$, $H\phi_{1A}$, $H\phi_{1B}$, $H\phi_{2A}$, $H\phi_{2B}$, $LH\phi_1$, GND – V_L	–0.3 to +13	V	
Between input clock pins	Potential difference between vertical clock input pins	to +13	V	*1
	$H\phi_{1A}$, $H\phi_{1B}$ – $H\phi_{2A}$, $H\phi_{2B}$	–5 to +5	V	
	$H\phi_{1A}$, $H\phi_{1B}$, $H\phi_{2A}$, $H\phi_{2B}$ – $V\phi_{4B}$, $V\phi_{HLD}$	–13 to +13	V	
Storage temperature		–30 to +80	℃	
Operating temperature		–10 to +60	℃	

*1 +25V (Max.) is guaranteed when clock width < 10μs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1			V	
Substrate clock	ϕSUB	*2				
Reset gate clock	ϕRG	*2				

*1 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and the reset gate clock pin, because a DC bias is generated internally.

DC Characteristics

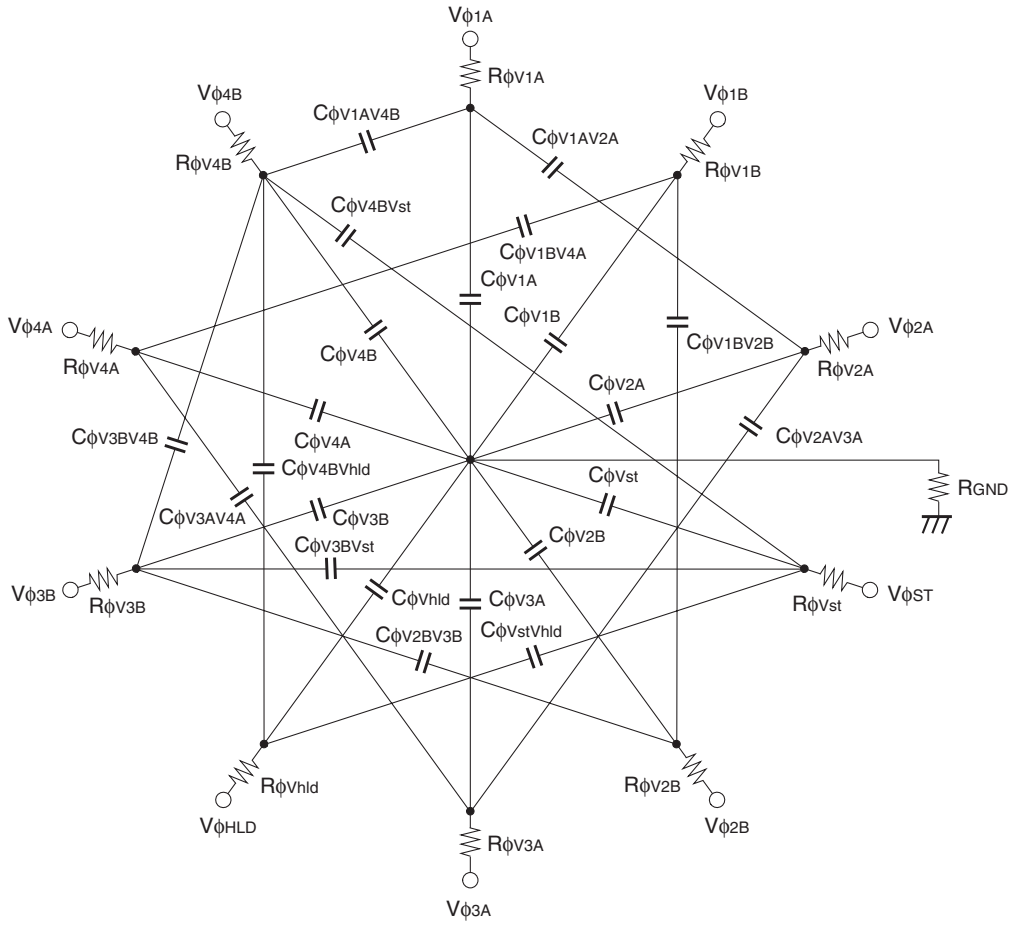
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		10.0		mA	

Clock Voltage Conditions

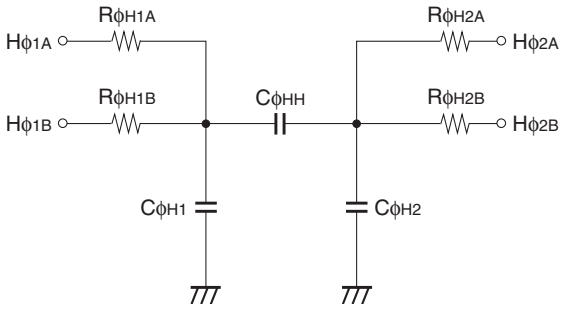
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH2}, V_{VH3}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH2} + V_{VH3})/2$
	V_{VH1}, V_{VH4}, V_{VHSTR}, V_{VHHLD}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}, V_{VLSTR}, V_{VLHLD}	–8.8	–8.5	–8.2	V	2	$V_{VL} = (V_{VL1} + V_{VL4})/2$
	$V\phi_V$	8.0	8.5	8.85	V	2	$V\phi_V = V_{VHn} – V_{VLn}$ (n = 1 to 4)
	$V_{VH1} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High-level coupling
	V_{VHL}			0.5	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	3.4	3.6	3.8	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	$V\phi_H/2$			V	3	Cross-point voltage
Reset gate clock voltage	$V\phi_{RG}$	3.4	3.6	3.8	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi_{SUB}$	22.5	23.5	24.5	V	5	

Clock Equivalent Circuit Constants

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1A}$, $C_{\phi V1B}$		1200		pF	
	$C_{\phi V2A}$, $C_{\phi V2B}$		2700		pF	
	$C_{\phi V3A}$, $C_{\phi V3B}$		680		pF	
	$C_{\phi V4A}$, $C_{\phi V4B}$		1800		pF	
	$C_{\phi Vst}$, $C_{\phi Vhld}$		1		pF	
Capacitance between vertical transfer clocks	$C_{\phi V1AV2A}$, $C_{\phi V1BV2B}$		220		pF	
	$C_{\phi V1AV4B}$, $C_{\phi V1BV4A}$		47		pF	
	$C_{\phi V2AV3A}$, $C_{\phi V2BV3B}$		220		pF	
	$C_{\phi V3AV4A}$, $C_{\phi V3BV4B}$		390		pF	
	$C_{\phi V3BVst}$, $C_{\phi V4BVhld}$		47		pF	
	$C_{\phi V4BVst}$, $C_{\phi VstVhld}$		47		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$		32		pF	
	$C_{\phi H2}$		30		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		56		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		1		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		330		pF	
Capacitance between horizontal final stage transfer clock and GND	$C_{\phi LH1}$		1		pF	
Vertical transfer clock series resistor	$R_{\phi V1A}$, $R_{\phi V1B}$, $R_{\phi V4A}$, $R_{\phi V4B}$, $R_{\phi Vst}$, $R_{\phi Vhld}$		39		Ω	
	$R_{\phi V2A}$, $R_{\phi V2B}$, $R_{\phi V3A}$, $R_{\phi V3B}$		82		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock series resistor	$R_{\phi H1A}$, $R_{\phi H1B}$		18		Ω	
	$R_{\phi H2A}$, $R_{\phi H2B}$		16		Ω	
Substrate clock series resistor	$R_{\phi SUB}$		300		kΩ	



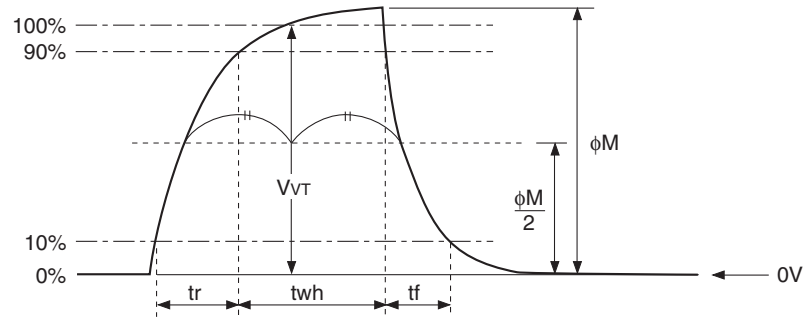
Vertical transfer clock equivalent circuit



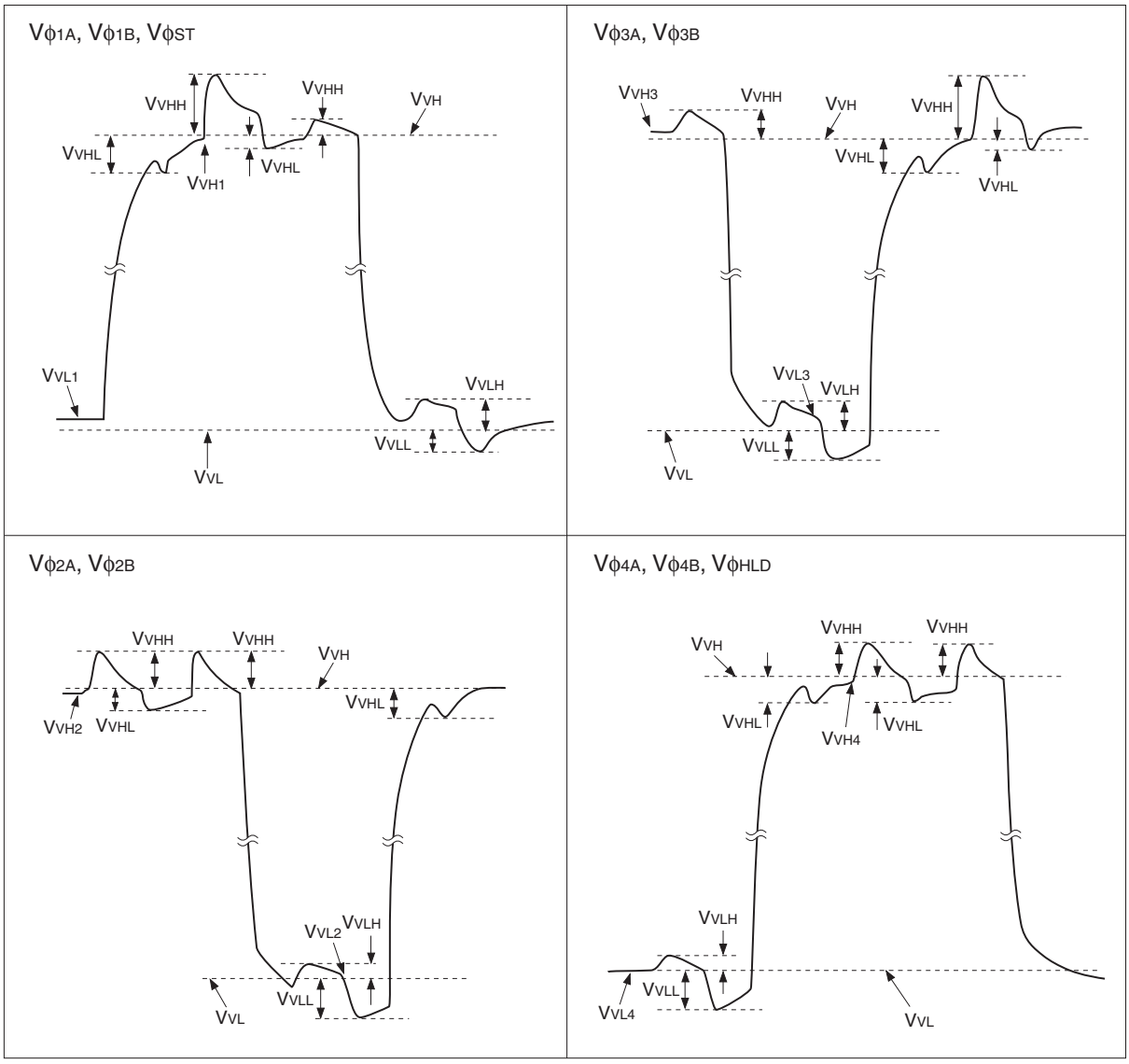
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Readout clock waveform

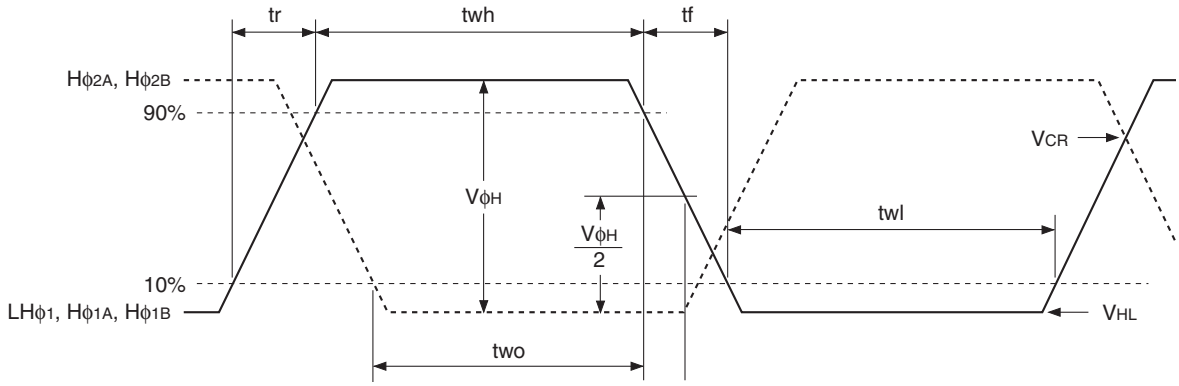


2. Vertical transfer clock waveform



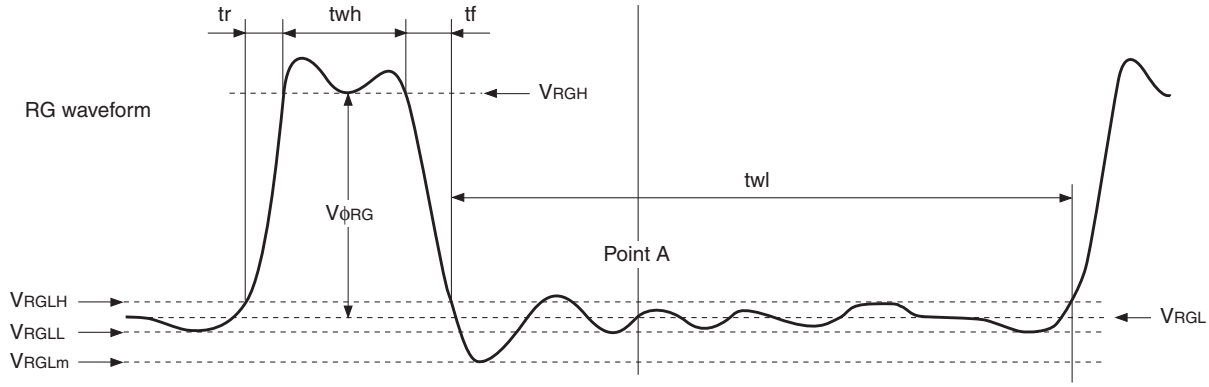
$V_{VH} = (V_{VH2} + V_{VH3})/2$
$V_{VL} = (V_{VL1} + V_{VL4})/2$
$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)

3. Horizontal transfer clock waveform



Cross-point voltage for the Hφ1A, Hφ1B and LHφ1 rising side of the horizontal transfer clocks Hφ1A, Hφ1B, LHφ1 and Hφ2A, Hφ2B waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hφ1A, Hφ1B, LHφ1 and Hφ2A, Hφ2B is "two".

4. Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

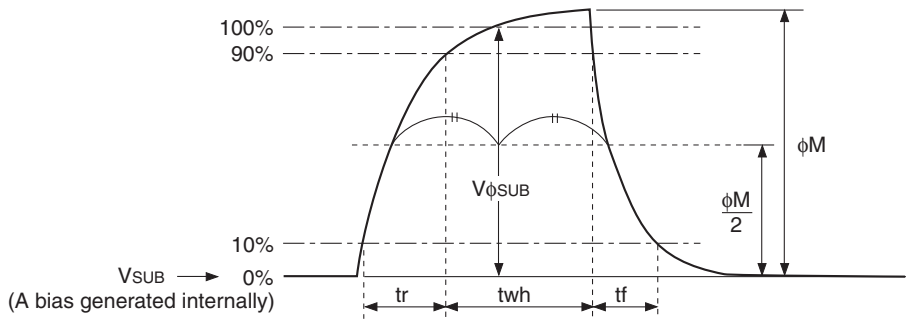
$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$

Assuming VRGH is the minimum value during the interval twh, then:

$V_{\phi RG} = V_{RGH} - V_{RGL}$

Negative overshoot level during the falling edge of RG is VRGLm.

5. Substrate clock waveform



Clock Switching Characteristics

(Horizontal drive frequency: 36.0MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	VT	1.52	1.72						0.5			0.5		μs	During readout
Vertical transfer clock	Vφ1A, Vφ1B, Vφ2A, Vφ2B, Vφ3A, Vφ3B, Vφ4A, Vφ4B, VφST, VφHLD										15		250	ns	When using CXD3400N
Horizontal transfer clock	LHφ1, Hφ1A, Hφ1B	8	9		8	9			5	6		5	6	ns	When driving at 3.6V during imaging, tf ≥ tr – 2ns
	Hφ2A, Hφ2B	8	9		8	9			5	6		5	6		
Reset gate clock	φRG	4	5.5			17.2			2			3		ns	
Substrate clock	φSUB	0.9	1.8							0.25			0.25	μs	When draining charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	LHφ1, Hφ1A, Hφ1B, Hφ2A, Hφ2B	8	9		ns	

Spectral Sensitivity Characteristics

(excludes lens characteristics and light source characteristics)

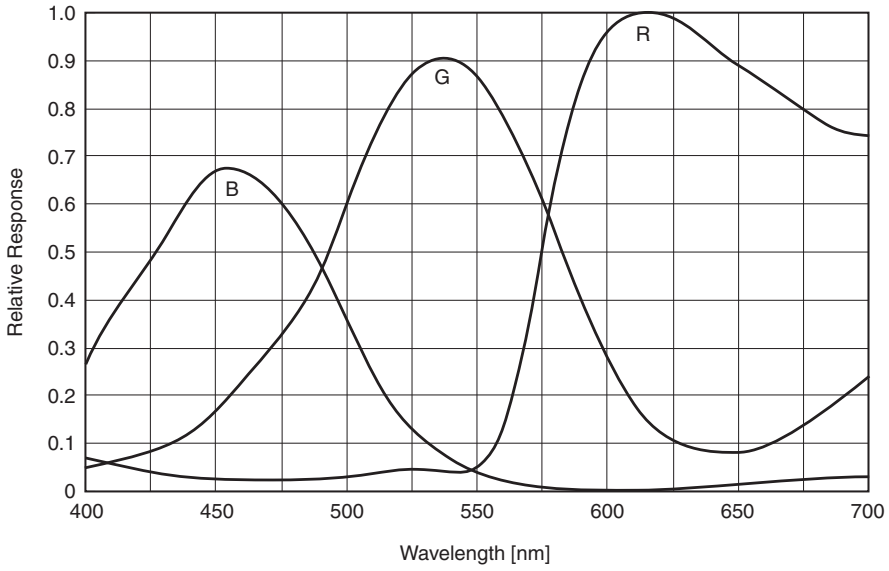


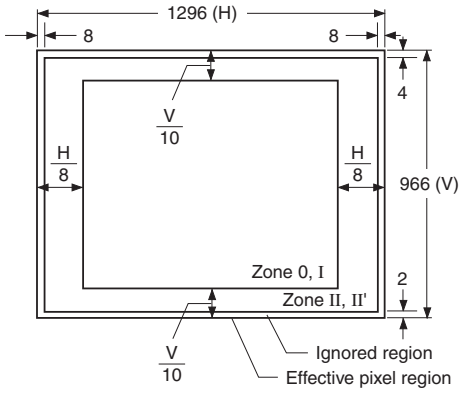
Image Sensor Characteristics (Center cut-out drive, 30 frame/s)

(Ta = 25℃)

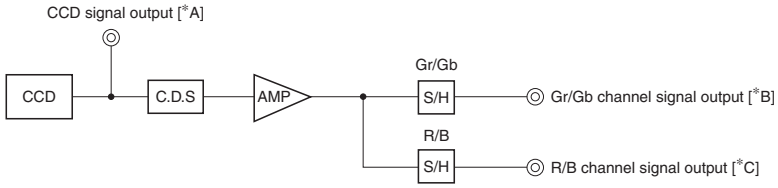
Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		Sg	300	380		mV	1	1/30s accumulation
Sensitivity ratio	R	Rr	0.55		0.81		1	
	B	Rb	0.23		0.49		1	
Saturation signal		Ysat	350			mV	2	Ta = 60℃
Smear		Sm		–104	–96	dB	3	
Video signal shading		SHg			20	%	4	Zone 0 and I
					25	%	4	Zone 0 to II'
Uniformity between video signal channels		ΔSrg			8	%	5	
		ΔSbg			8	%	5	
Dark signal		Vdt			2	mV	6	Ta = 60℃, 1/30s accumulation
Dark signal shading		ΔVdt			1	mV	7	Ta = 60℃, 1/30s accumulation*1
Line crawl R		Lcr			3.8	%	8	
Line crawl B		Lcb			3.8	%	8	
Lag		Lag			0.5	%	9	

*1 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System



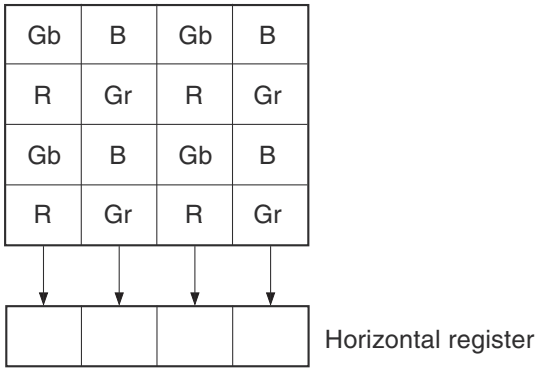
Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

Image Sensor Characteristics Measurement Method

Measurement conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

Color coding of this image sensor & Readout



Color Coding Diagram

The primary color filters of this image sensor are arranged in the layout shown in the figure above (Bayer array). Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.

The R signal and Gr signal lines and Gb signal and B signal lines are output successively.

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance : 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, sensitivity ratio
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{Gr}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

$V_G = (V_{Gr} + V_{Gb})/2$
$Sg = V_G \times (100/30)$ [mV]
$Rr = V_R/V_G$
$Rb = V_B/V_G$

2. Saturation signal
Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (VSm) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

$Sm = 20 \times \log \{Vsm \div ((Gra + Gba + Ra + Ba)/4) \times (1/500) \times (1/10)\}$ [dB]

4. Video signal shading
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum value (Grmax) and minimum value (Grmin) of the Gr signal and substitute the values into the following formula.

$SHg = (Gmax - Gmin)/150 \times 100$ [%]

5. Uniformity between video signal channels
After the measurement item 4, measure the maximum (Rmax) and minimum (Rmin) values of the R signal and the maximum (Bmax) and minimum (Bmin) values of the B signal, and substitute the values into the following formula.

$\Delta Srg = (Rmax - Rmin)/150 \times 100$ [%]
$\Delta Sbg = (Bmax - Bmin)/150 \times 100$ [%]

6. Dark signal
Measure the average value of the signal output (Vdt) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
   After the measurement item 6, measure the maximum (Vdmax) and minimum (Vdmin) values of the dark signal output and substitute the values into the following formula.

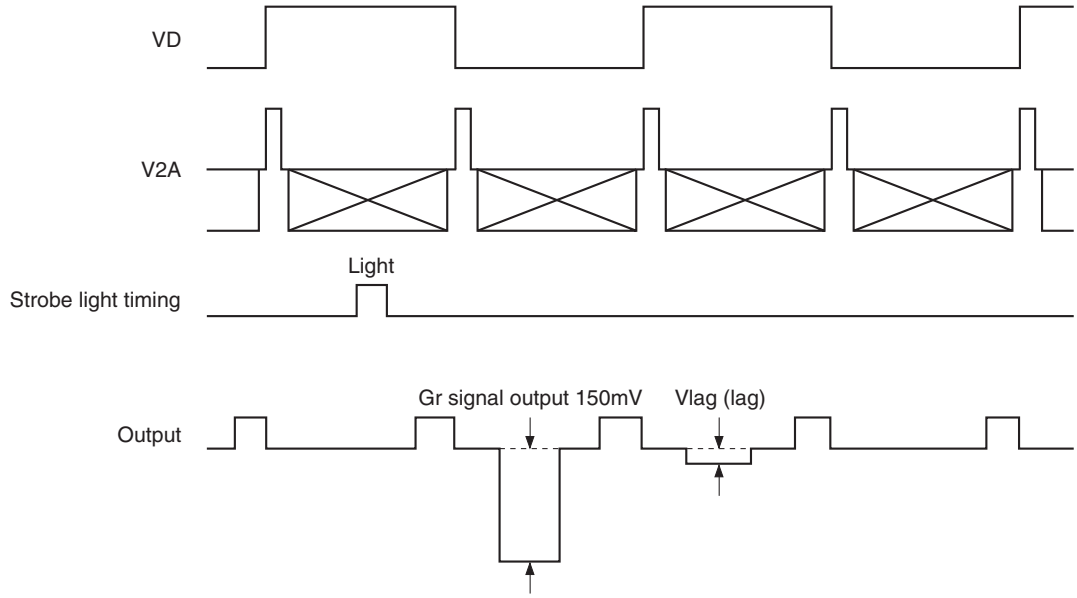
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

8. Line crawl
   Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

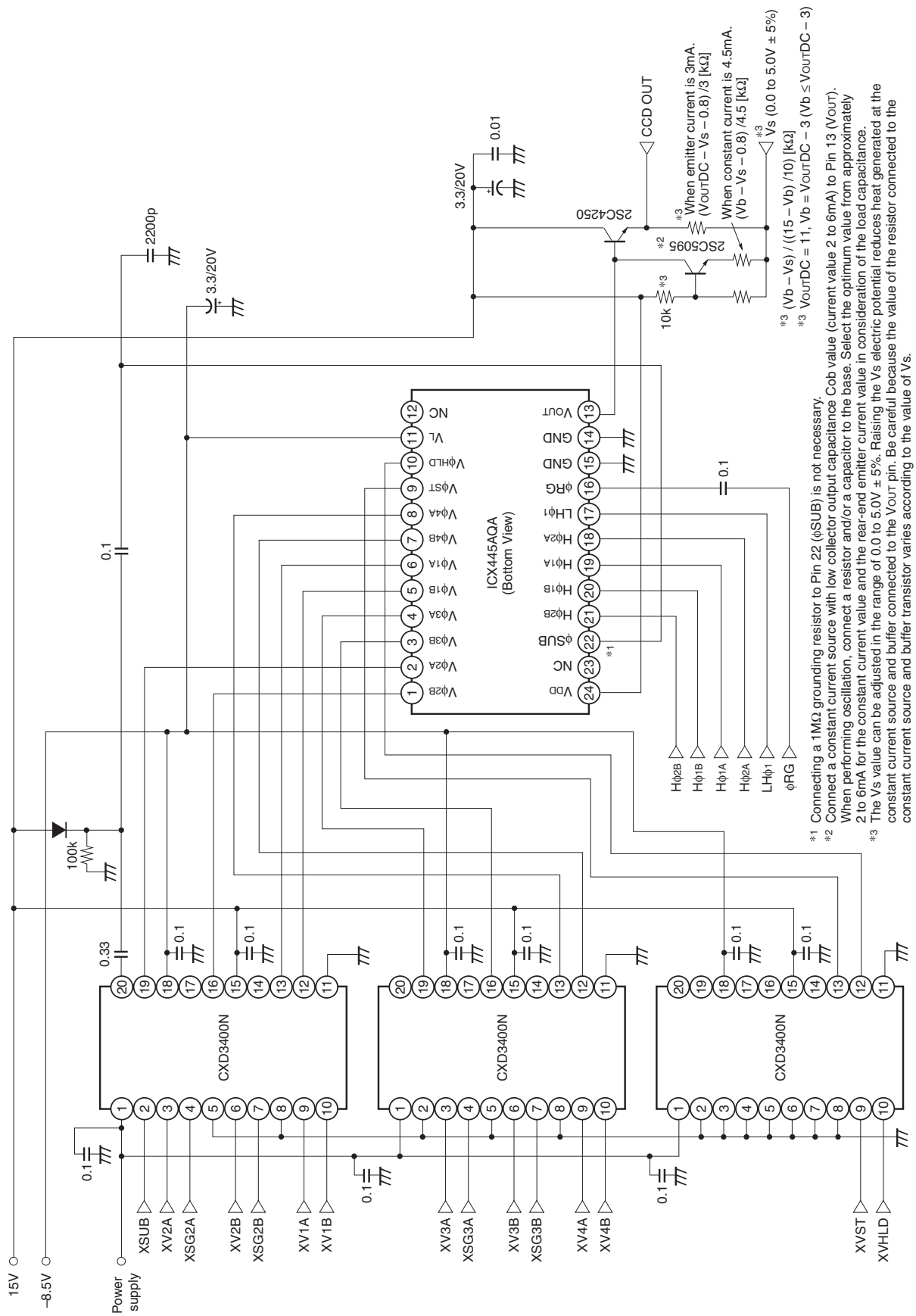
   $Lc_i = (\Delta Gl_i / Ga_i) \times 100$ [%] (i = r, g, b)

9. Lag
   Adjust the Gr signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/150) \times 100$ [%]

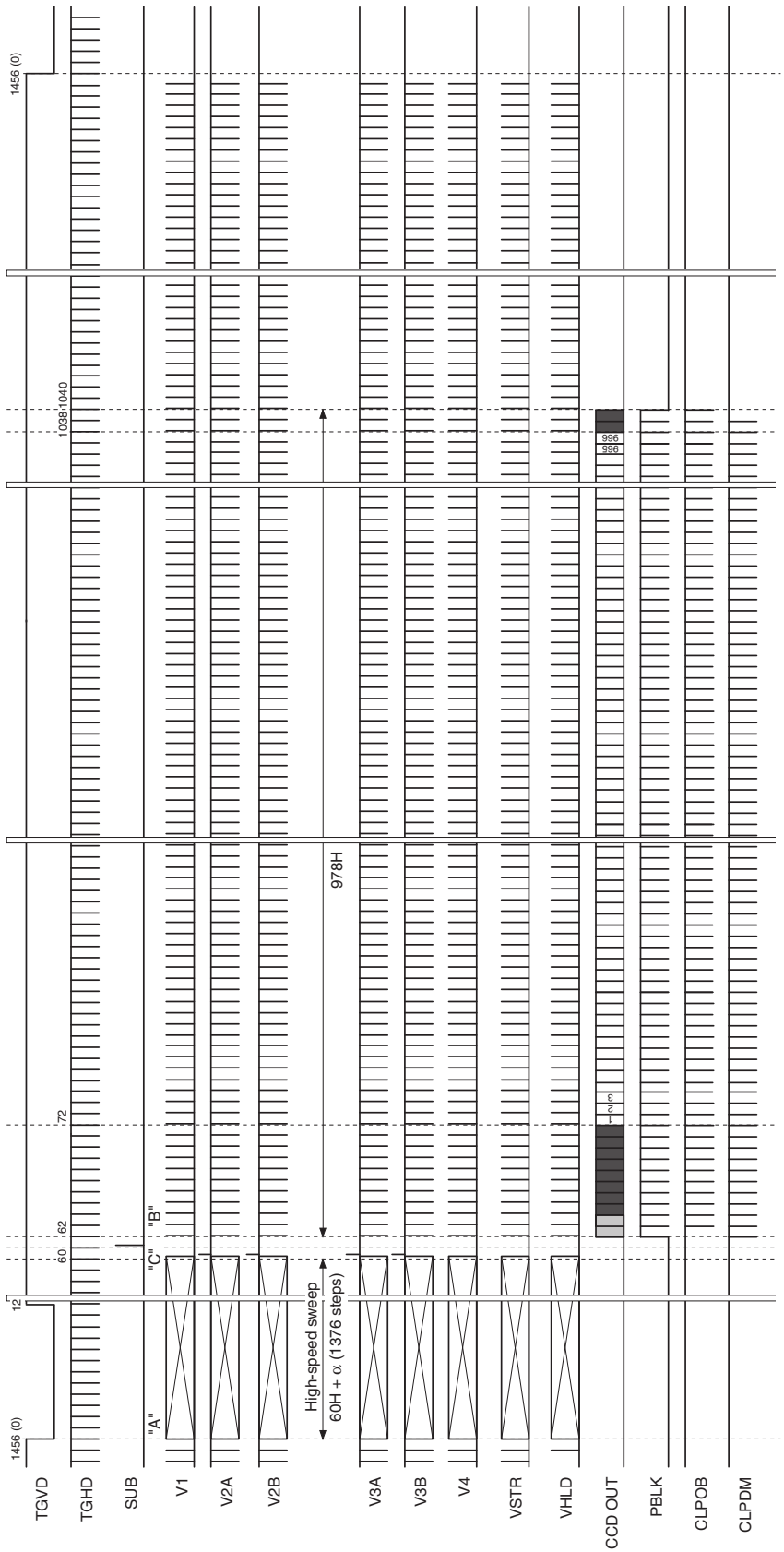


Drive Circuit



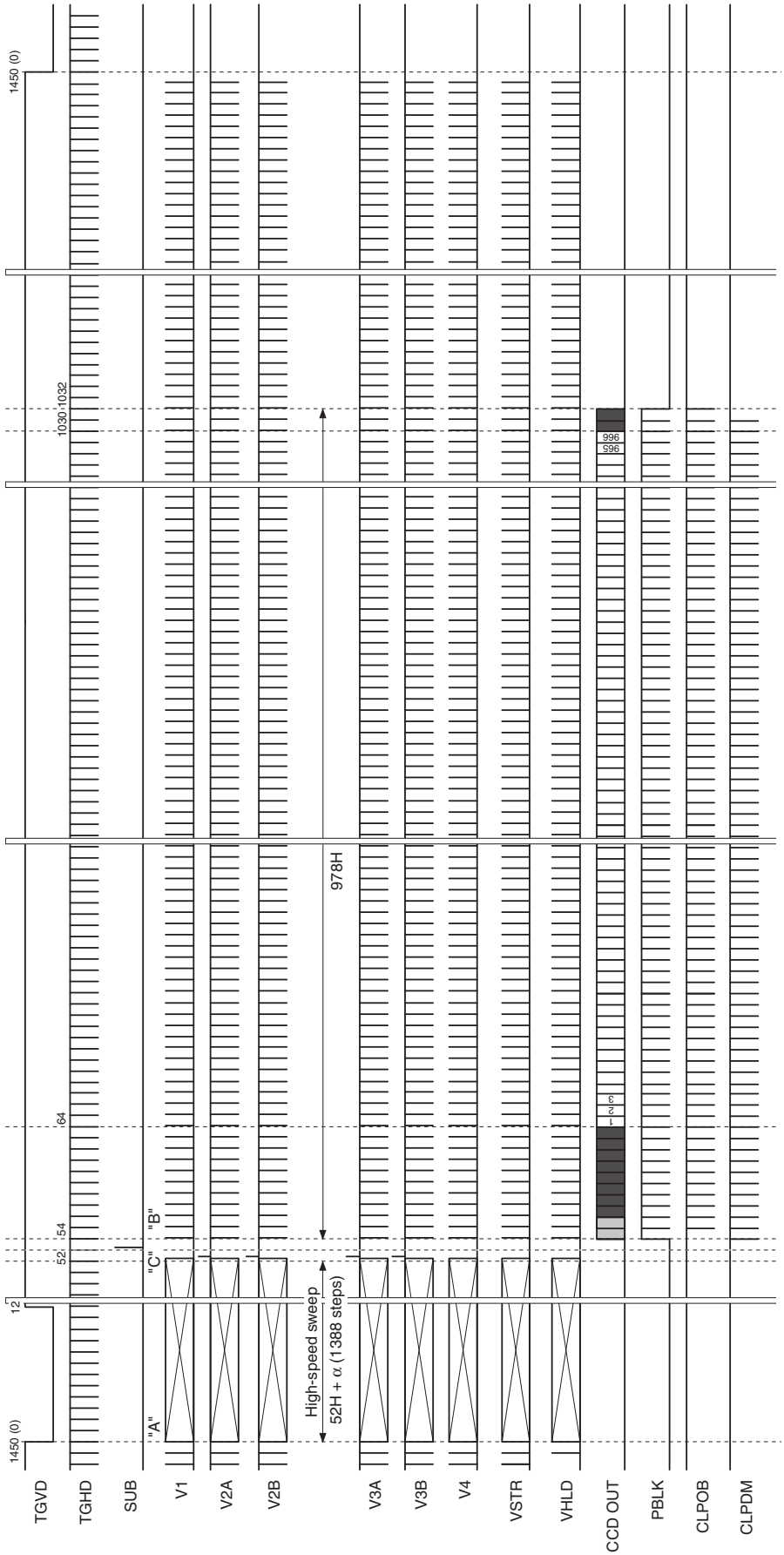
Drive Timing Chart

All-pixel Scan Mode (15 frame/s) Vertical Direction



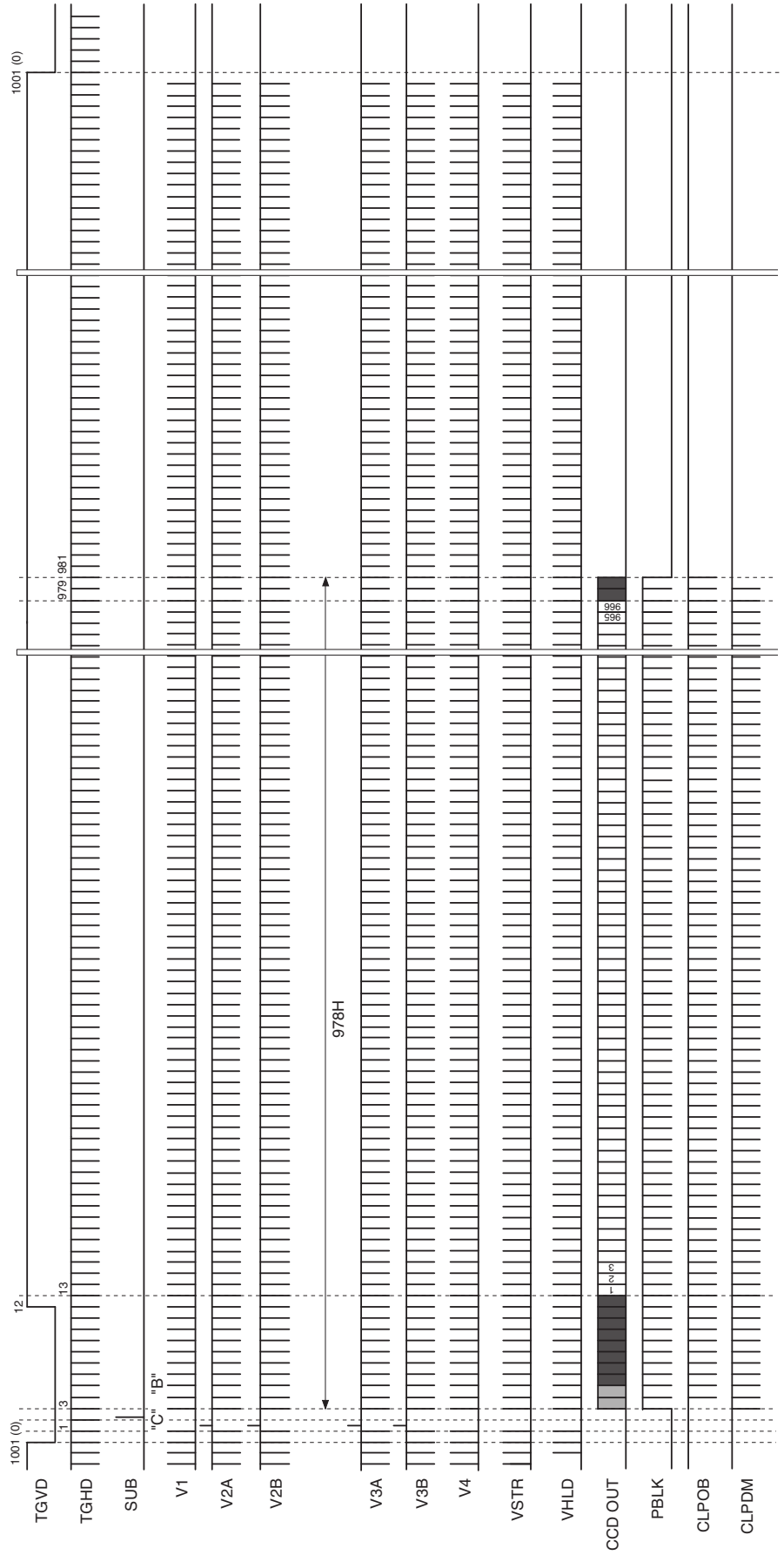
* The TGVD in this chart is noted at 1456H (1H: 1650 clocks). (1 clock = 36.0MHz)

All-pixel Scan Mode (12.5 frame/s) Vertical Direction



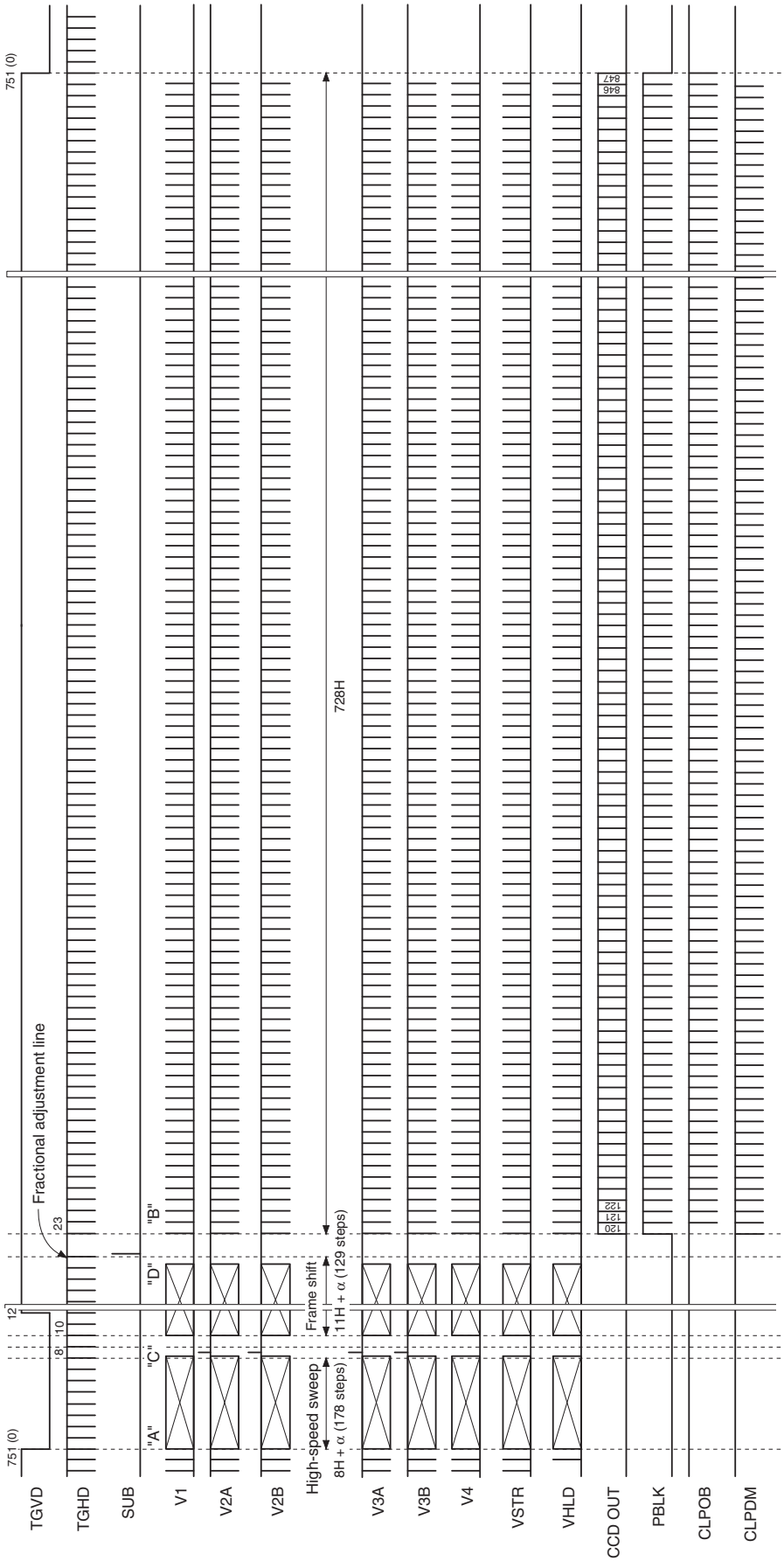
* The TGVD in this chart is noted at 1450H (1H: 1600 clocks). (1 clock = 29.0MHz)

All-pixel Scan Mode (22.5 frame/s) Vertical Direction



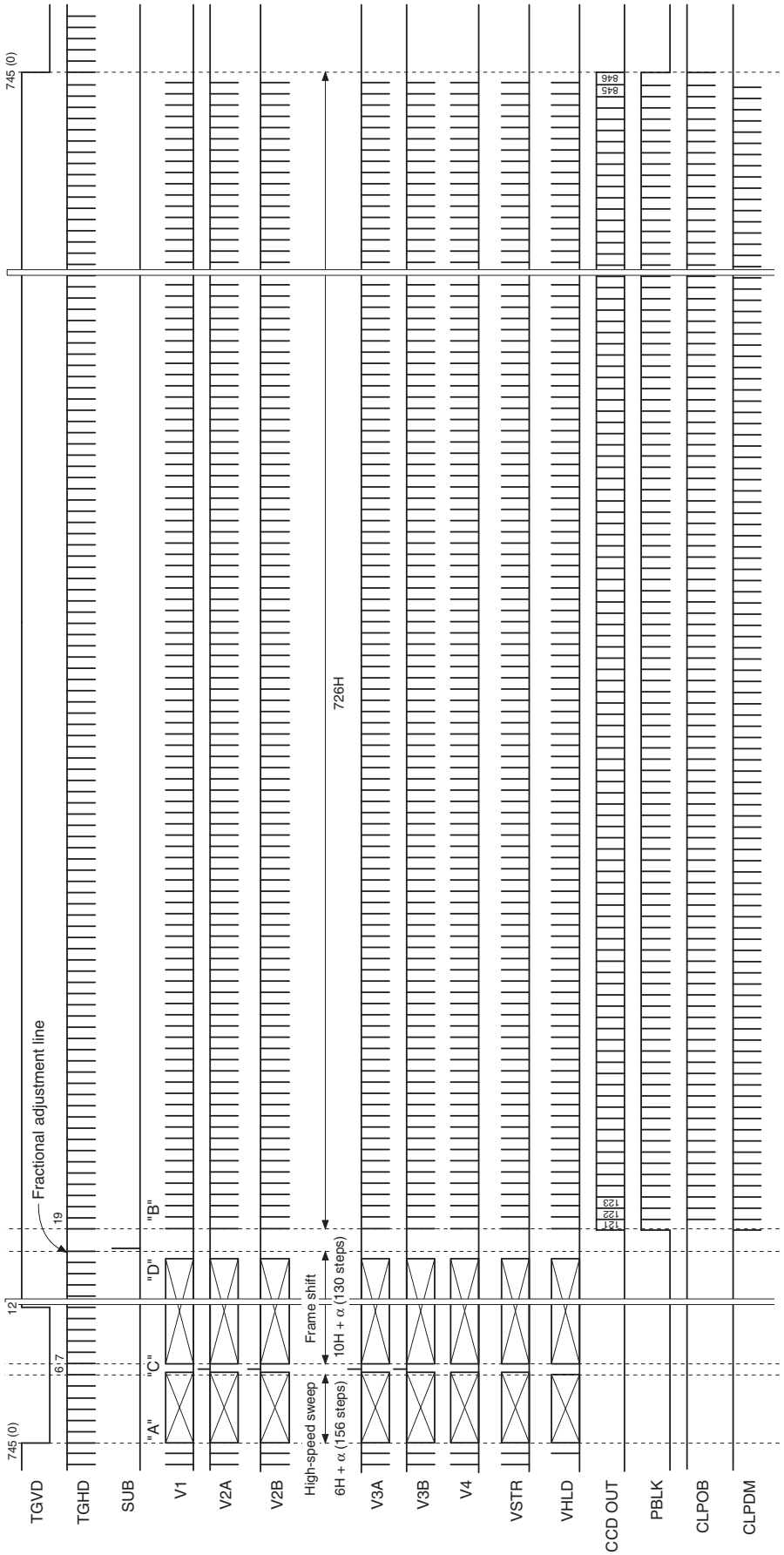
* The TGVD in this chart is noted at 1001H (1H: 1600 clocks). (1 clock = 36.0MHz)

Center Cut-out Mode (30 frame/s) Vertical Direction



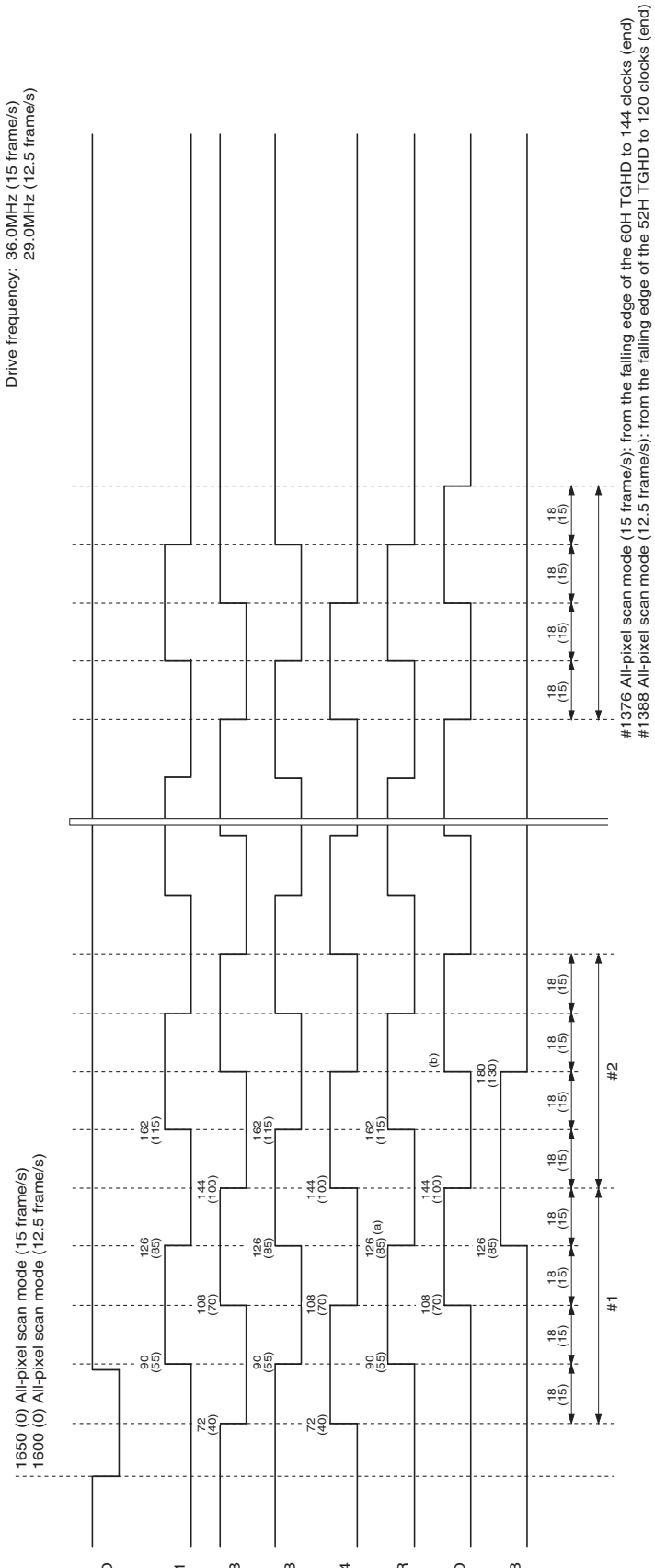
* The TGVD in this chart is noted at 750H (1H: 1598 clocks) + 1H (2700 clocks: fractional adjustment line). (1 clock = 36.0MHz)

Center Cut-out Mode (25 frame/s) Vertical Direction



* The TGVD in this chart is noted at 744H (1H: 1556 clocks) + 1H (2336 clocks: fractional adjustment line). (1 clock = 29.0MHz)

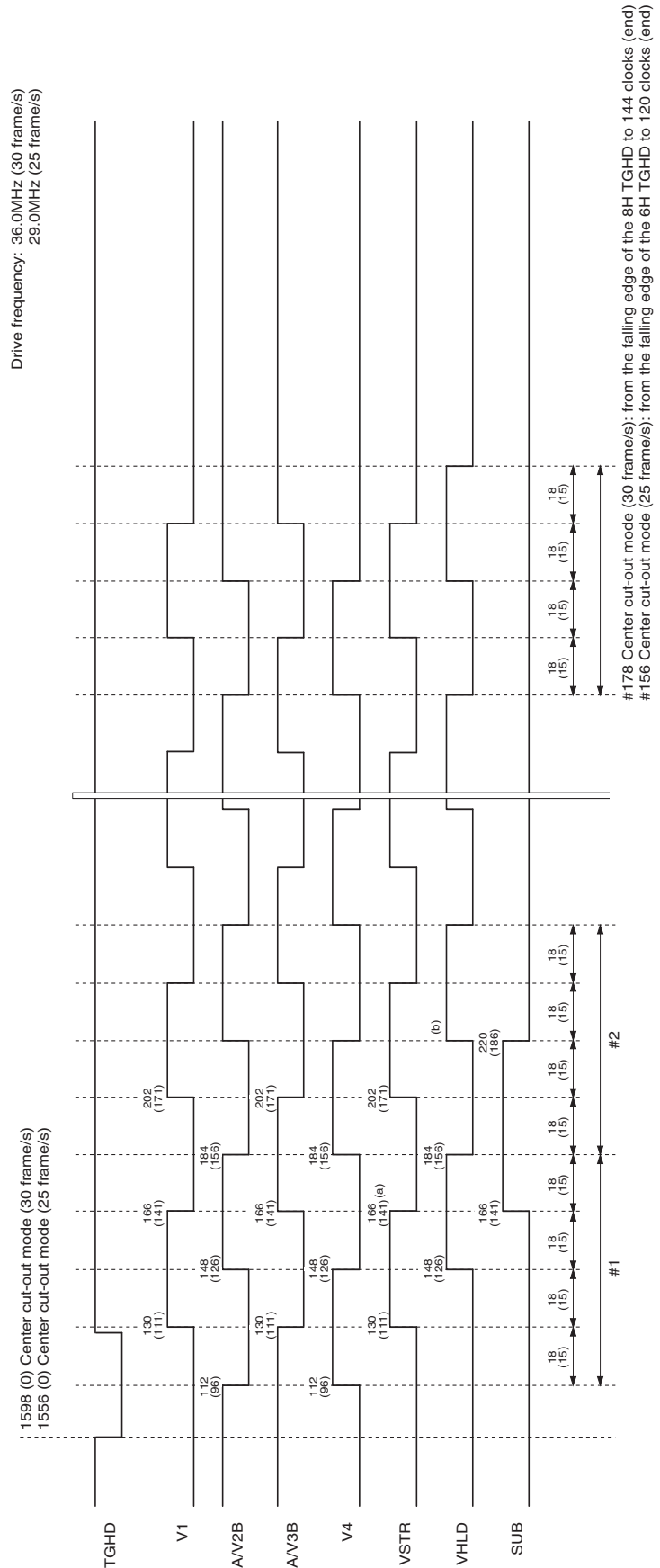
All-pixel Scan Mode (15 frame/s, 12.5 frame/s)
Horizontal Direction High-speed sweep block [A]



* Synchronize the rising edge of SUB with the first falling edge of VSTR (a) counting from the falling edge of TGHD and synchronize the falling edge of SUB with the first rising edge of VHLD counting from (a).

* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD. The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.

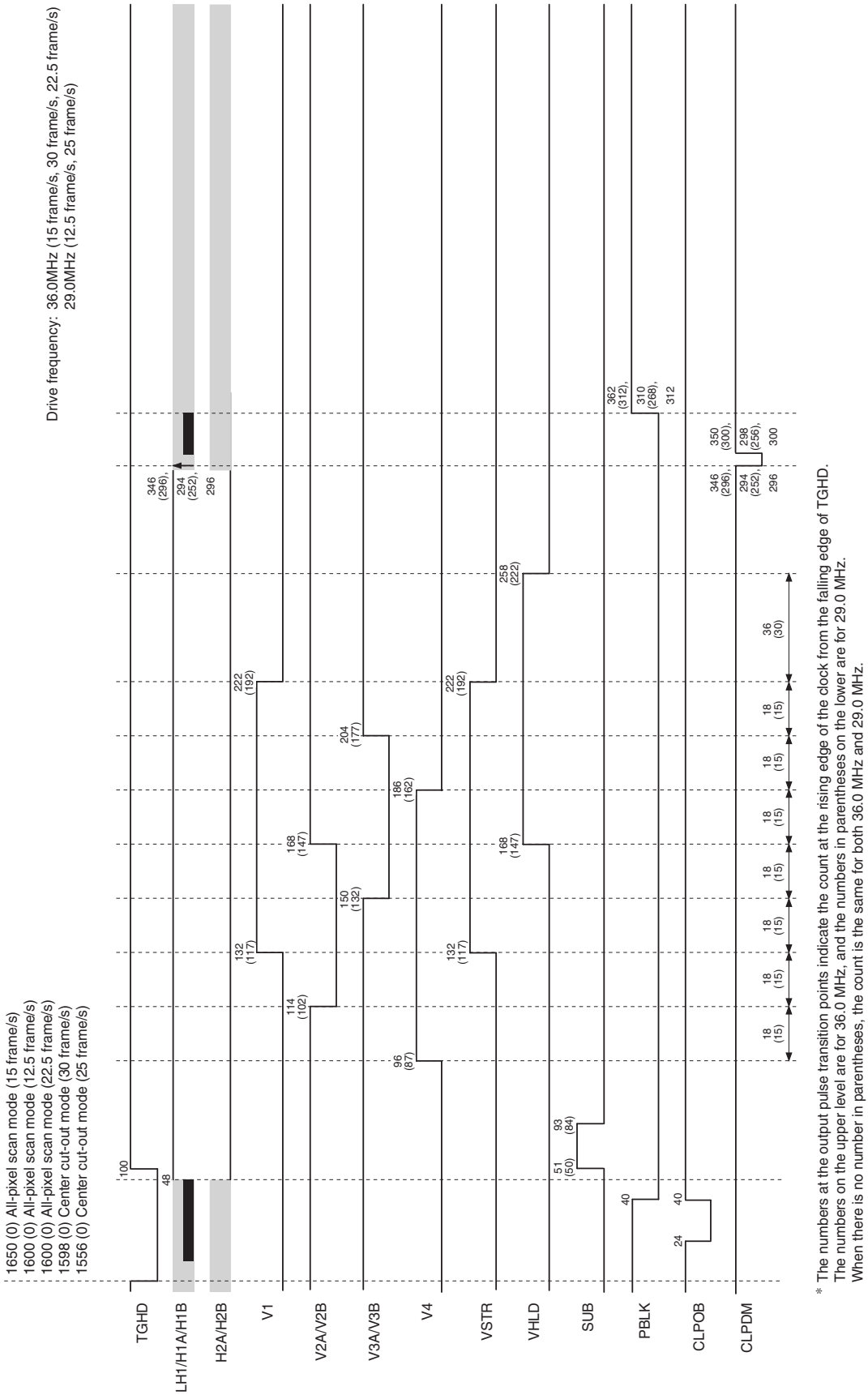
Center cut-out Mode (30 frame/s, 25 frame/s)
Horizontal Direction High-speed sweep block [A]



* Synchronize the rising edge of SUB with the first falling edge of VSTR (a) counting from the falling edge of TGHD and synchronize the falling edge of SUB with the first rising edge of VHLD counting from (a).

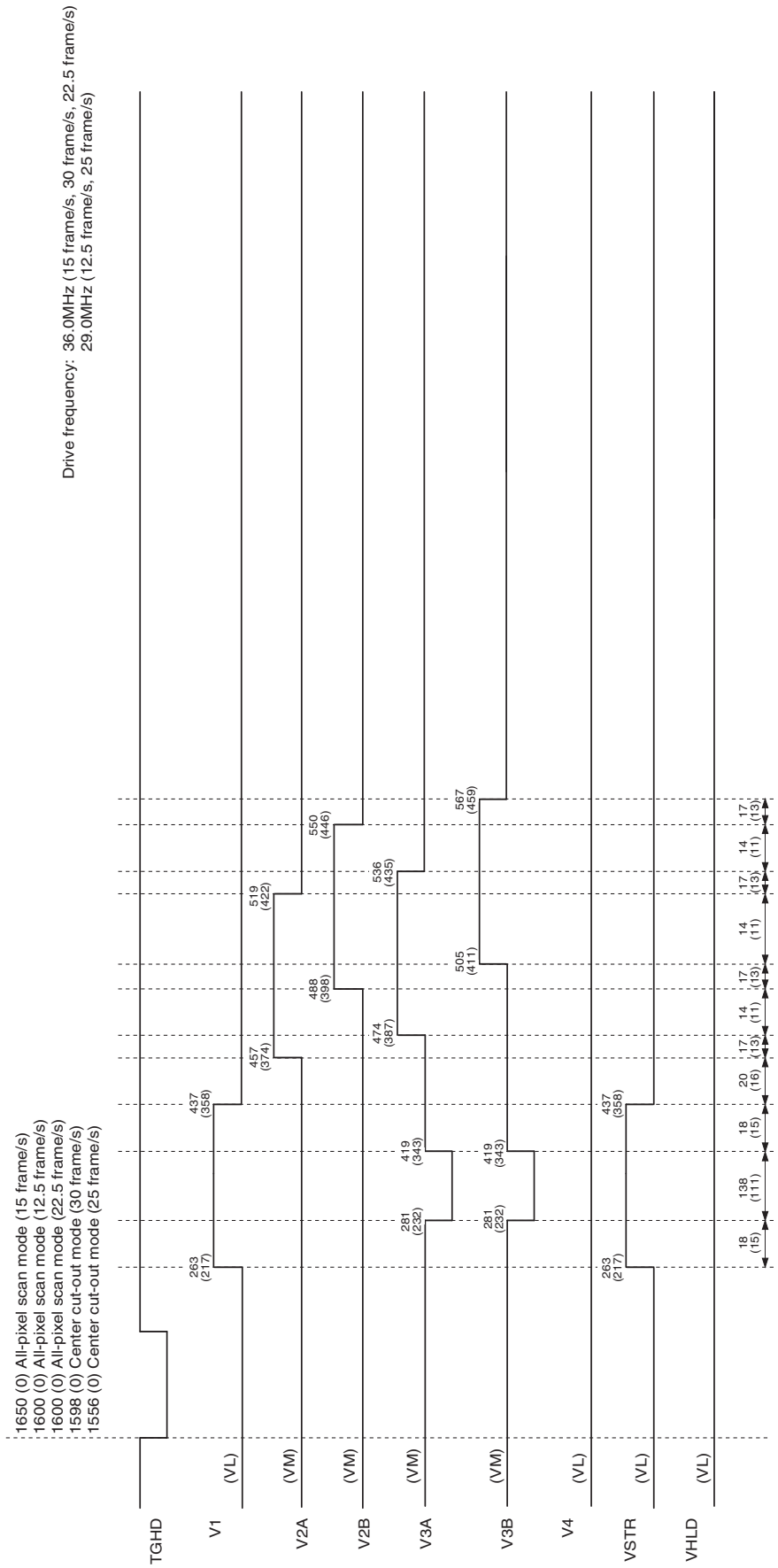
* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD. The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.

All-pixel Scan Mode (15 frame/s, 12.5 frame/s, 22.5 frame/s)/Center Cut-out Mode (30 frame/s, 25 frame/s)
Horizontal Direction Normal Transfer Block [B]



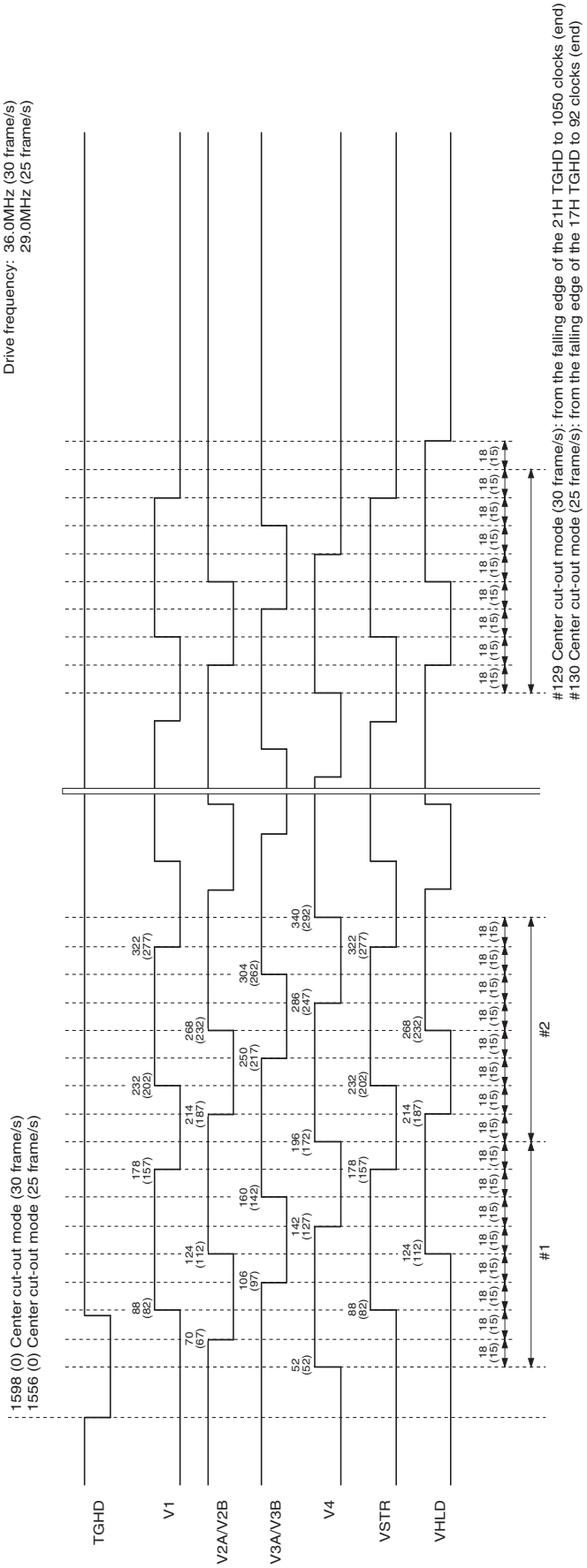
* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.
The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.
When there is no number in parentheses, the count is the same for both 36.0 MHz and 29.0 MHz.

All-pixel Scan Mode (15 frame/s, 12.5 frame/s, 22.5 frame/s)/ Center Cut-out Mode (30 frame/s, 25 frame/s)
Horizontal Direction Readout Block [C]



* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.
The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.

Center Cut-out Mode (30 frame/s, 25 frame/s)
Horizontal Direction Frame Shift Block [D]



* SUB pulse generation is prohibited during the frame shift period.

* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.
The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.

Notes On Handling

1. Static charge prevention

   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

   (1) Either handle bare handed or use non-chargeable gloves, clothes or material.
   Also use conductive shoes.

   (2) Use a wrist strap when handling directly.

   (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.

   (4) Ionized air is recommended for discharge when handling CCD image sensors.

   (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Soldering

   (1) Make sure the package temperature does not exceed 80℃.

   (2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in 2 seconds or less. For repairs and remount, cool sufficiently.

   (3) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3. Protection from dust and dirt

   Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

   (1) Perform all lens assembly and other work in a clean room (class 1000 or less).

   (2) Do not touch the glass surface with hand and make any object contact with it. If dust or other is stuck to a glass surface, blow it off with an air blower. (For dust stuck through static electricity, ionized air is recommended.)

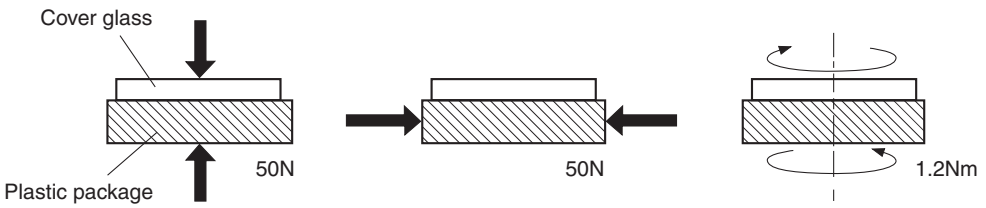
   (3) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.

   (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

   (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

4. Installing (attaching)

   (1) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional strength**

   (2) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

   (3) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.

(4) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

(5) If the lead bend repeatedly and the metal, etc., clash or rub against the package, dust may be generated by the fragments of resin.

(6) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5. Others

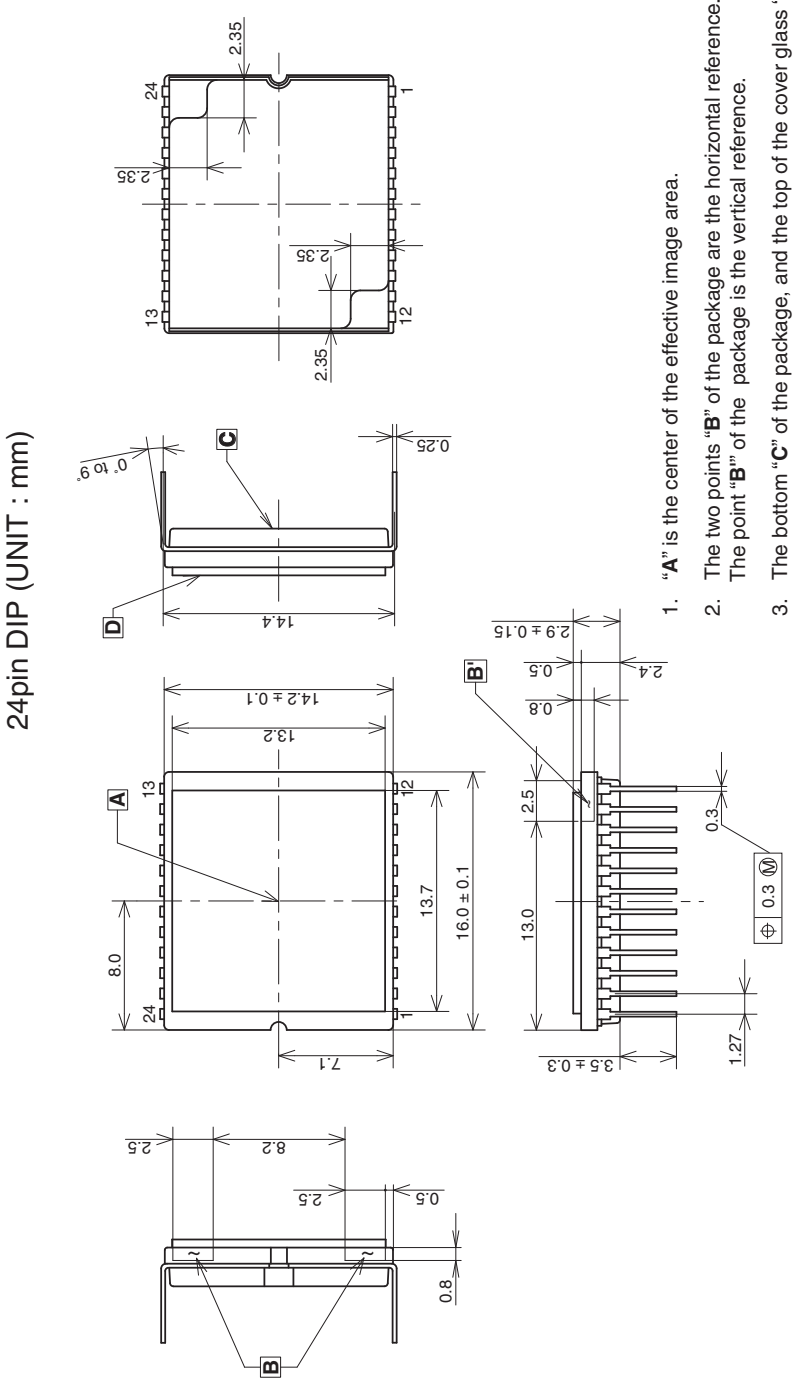
(1) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloration of the color filters may be accelerated. In such a case, arrangements such as using an automatic iris with the imaging lens or automatically closing the shutter during power-off are advisable. For continuous use under harsh conditions exceeding the normal conditions of use, consult your Sony representative.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

(3) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

Package Outline

(Unit: mm)



1. "**A**" is the center of the effective image area.
2. The two points "**B**" of the package are the horizontal reference.
   The point "**B'**" of the package is the vertical reference.
3. The bottom "**C**" of the package, and the top of the cover glass "**D**" are the height reference.
4. The center of the effective image area relative to "**B**" and "**B'**" is (H, V) = (8.0, 7.1) ± 0.075mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°
6. The height from the bottom "**C**" to the effective image area is 1.41mm ± 0.1mm.
   The height from the top of the cover glass "**D**" to the effective image area is 1.49mm ± 0.15mm
7. The tilt of the effective image area relative to the bottom "**C**" is less than 35µm.
   The tilt of the effective image area relative to the top "**D**" of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.20g
DRAWING NUMBER	AS-A16(E)