SONY

Diagonal 4.5mm (Type 1/4) Progressive Scan CCD Image Sensor
with Square Pixel for Color Cameras

# ICX614AQA

## Description

The ICX614AQA is a diagonal 4.5mm (Type 1/4) interline CCD solid-state image sensor with a square pixel array which supports VGA format. Progressive scan enables all pixel signals to be output separately within approximately 1/60 second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter. High resolution and high color reproducibility are achieved through the use of R, G, B primary color mosaic filters.
Further, high sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.
This chip is suitable for applications such as security cameras and network cameras.

## Features

- ◆ High sensitivity (+2.0dB compared with the ICX098BQ)
- ◆ High saturation signal (+2.5dB compared with the ICX098BQ)
- ◆ Progressive scan enables individual readout of the image signals from all pixels.
- ◆ Square pixel
- ◆ Supports VGA format
- ◆ Horizontal drive frequency: Supports 24.54MHz
- ◆ No voltage adjustments (Reset gate and substrate bias need no adjustment.)
- ◆ R, G, B primary color mosaic filters on chip
- ◆ High resolution, high color reproducibility, high sensitivity, low dark current
- ◆ Continuous variable-speed shutter
- ◆ Low smear
- ◆ Excellent anti-blooming characteristics
- ◆ Horizontal register: 3.3V drive
- ◆ 14-pin high accuracy plastic package (dual-surface reference available)

WfineCCD TM

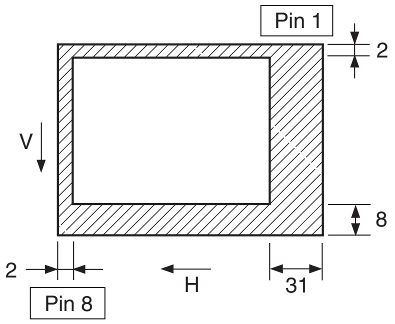
* Wfine CCD is a trademark of Sony Corporation.
Represents a CCD adopting progressive scan, primary color filter and square pixel.

## Element Structure

- Interline CCD image sensor
- Image size:
  Diagonal 4.5mm (Type 1/4)
- Number of effective pixels:
  659 (H) × 494 (V) approx. 330K pixels
- Total number of pixels:
  692(H) × 504 (V) approx. 350K pixels
- Chip size:
  4.46mm (H) × 3.80mm (V)
- Unit cell size:
  5.6µm (H) × 5.6µm (V)
- Optical black:
  Horizontal (H) direction: Front 2 pixels, rear 31 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits:
  Horizontal: 16
  Vertical: 4
- Substrate material:
  Silicon

## Optical Black Position

(Top View)



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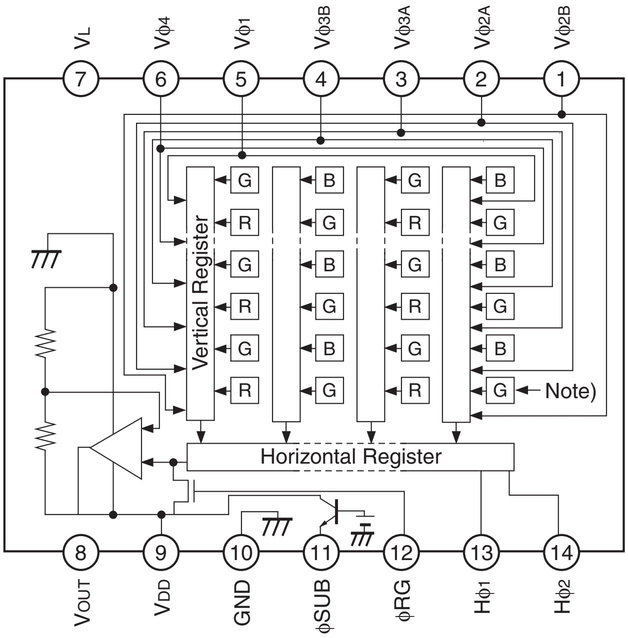
## Block Diagram and Pin Configuration

(Top View)




Note) □ : Photo sensor

## Pin Description

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | Vφ2B | Vertical register transfer clock |
| 2 | Vφ2A | Vertical register transfer clock |
| 3 | Vφ3A | Vertical register transfer clock |
| 4 | Vφ3B | Vertical register transfer clock |
| 5 | Vφ1 | Vertical register transfer clock |
| 6 | Vφ4 | Vertical register transfer clock |
| 7 | VL | Protective transistor bias |
| 8 | VOUT | Signal output |
| 9 | VDD | Supply voltage |
| 10 | GND | GND |
| 11 | φSUB | Substrate clock |
| 12 | φRG | Reset gate clock |
| 13 | Hφ1 | Horizontal register transfer clock |
| 14 | Hφ2 | Horizontal register transfer clock |

## Absolute Maximum Ratings

| Item | | Ratings | Unit | Remarks |
|---|---|---|---|---|
| Against $\phi$SUB | $V_{DD}$, $V_{OUT}$, $\phi$RG – $\phi$SUB | –40 to +13 | V | |
| | $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 3A}$, $V_{\phi 3B}$ – $\phi$SUB | –50 to +15 | V | |
| | $V_{\phi 1}$, $V_{\phi 4}$ – $\phi$SUB | –50 to +0.3 | V | |
| | $H_{\phi 1}$, $H_{\phi 2}$, GND – $\phi$SUB | –40 to +0.3 | V | |
| Against GND | $V_{DD}$, $V_{OUT}$, $\phi$RG – GND | –0.3 to +18 | V | |
| | $V_{\phi 1}$, $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 3A}$, $V_{\phi 3B}$, $V_{\phi 4}$ – GND | –10 to +18 | V | |
| | $H_{\phi 1}$, $H_{\phi 2}$ – GND | –10 to +5 | V | |
| Against $V_L$ | $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 3A}$, $V_{\phi 3B}$ – $V_L$ | –0.3 to +28 | V | |
| | $V_{\phi 1}$, $V_{\phi 4}$, $H_{\phi 1}$, $H_{\phi 2}$ – $V_L$ | –0.3 to +15 | V | |
| Between input clock pins | Potential difference between vertical clock input pins | to +15 | V | *1 |
| | $H_{\phi 1}$ – $H_{\phi 2}$ | –5 to +5 | V | |
| | $H_{\phi 1}$, $H_{\phi 2}$ – $V_{\phi 3}$ | –13 to +13 | V | |
| Storage temperature | | –30 to +80 | °C | |
| Operating temperature | | –10 to +60 | °C | |

*1 +24V (Max.) is guaranteed when clock width < 10μs, clock duty factor < 0.1%.

## Bias Conditions

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 14.55 | 15.0 | 15.45 | V | |
| Protective transistor bias | $V_L$ | | *1 | | | |
| Substrate clock | $\phi$SUB | | *2 | | | |
| Reset gate clock | $\phi$RG | | *2 | | | |

*1 $V_L$ setting is the $V_{VL}$ voltage of the vertical clock waveform, or the same voltage as the $V_L$ power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated internally.

## DC Characteristics

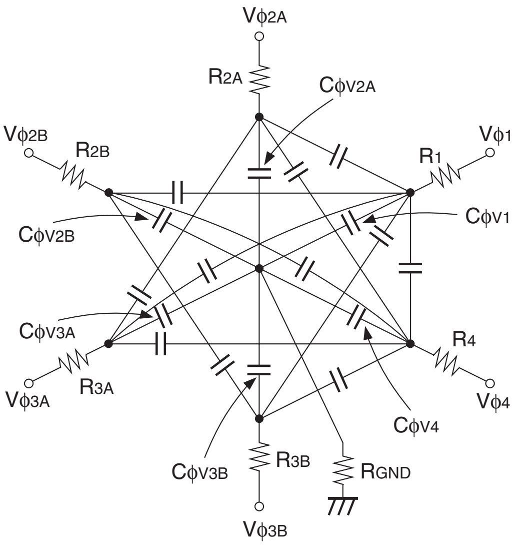
| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Supply current | $I_{DD}$ | | 6.0 | | mA | |

## Clock Voltage Conditions

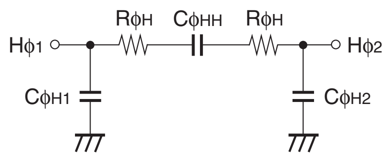
| Item | Symbol | Min. | Typ. | Max. | Unit | Waveform diagram | Remarks |
|---|---|---|---|---|---|---|---|
| Readout clock voltage | $V_{VT}$ | 14.55 | 15.0 | 15.45 | V | 1 | |
| Vertical transfer clock voltage | $V_{VH02A}$ | –0.05 | 0 | 0.05 | V | 2 | $V_{VH} = V_{VH02A}$ |
| | $V_{VH1}$, $V_{VH2\ (A,\ B)}$, $V_{VH3\ (A,\ B)}$, $V_{VH4}$ | –0.2 | 0 | 0.05 | V | 2 | |
| | $V_{VL1}$, $V_{VL2\ (A,\ B)}$, $V_{VL3\ (A,\ B)}$, $V_{VL4}$ | –5.8 | –5.5 | –5.2 | V | 2 | $V_{VL} = (V_{VL1} + V_{VL3\ (A,\ B)})/2$ |
| | $V_{\phi 1}$, $V_{\phi 2\ (A,\ B)}$, $V_{\phi 3\ (A,\ B)}$, $V_{\phi 4}$ | 5.0 | 5.5 | 5.85 | V | 2 | |
| | $\vert V_{VL3\ (A,\ B)}, V_{VL4} - V_{VL} \vert$ | | | 0.1 | V | 2 | |
| | $V_{VHH}$ | | | 0.3 | V | 2 | High-level coupling |
| | $V_{VHL}$ | | | 1.0 | V | 2 | High-level coupling |
| | $V_{VLH}$ | | | 0.5 | V | 2 | Low-level coupling |
| | $V_{VLL}$ | | | 0.5 | V | 2 | Low-level coupling |
| Horizontal transfer clock voltage | $V_{\phi H}$ | 3.0 | 3.3 | 5.25 | V | 3 | |
| | $V_{HL}$ | –0.05 | 0 | 0.05 | V | 3 | |
| Reset gate clock voltage | $V_{\phi RG}$ | 3.0 | 3.3 | 5.5 | V | 4 | |
| | $V_{RGLH} - V_{RGLL}$ | | | 0.4 | V | 4 | Low-level coupling |
| | $V_{RGL} - V_{RGLm}$ | | | 0.5 | V | 4 | Low-level coupling |
| Substrate clock voltage | $V_{\phi SUB}$ | 19.75 | 20.5 | 21.25 | V | 5 | |

## Clock Equivalent Circuit Constants

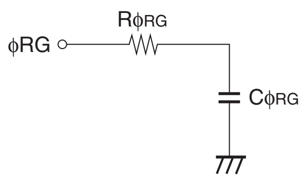
| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Capacitance between vertical transfer clock and GND | $C_{\phi V1}$ | | 1000 | | pF | |
| | $C_{\phi V2A}$, $C_{\phi V2B}$ | | 820 | | pF | |
| | $C_{\phi V3A}$, $C_{\phi V3B}$ | | 390 | | pF | |
| | $C_{\phi V4}$ | | 1500 | | pF | |
| Capacitance between vertical transfer clocks | $C_{\phi V12A}$, $C_{\phi V12B}$ | | 56 | | pF | |
| | $C_{\phi V13A}$, $C_{\phi V13B}$ | | 2 | | pF | |
| | $C_{\phi V14}$ | | 180 | | pF | |
| | $C_{\phi V2A3A}$, $C_{\phi V2B3B}$ | | 220 | | pF | |
| | $C_{\phi V2A4}$, $C_{\phi V2B4}$ | | 270 | | pF | |
| | $C_{\phi V3A4}$, $C_{\phi V3B4}$ | | 180 | | pF | |
| Capacitance between horizontal transfer clock and GND | $C_{\phi H1}$ | | 15 | | pF | |
| | $C_{\phi H2}$ | | 15 | | pF | |
| Capacitance between horizontal transfer clocks | $C_{\phi HH}$ | | 47 | | pF | |
| Capacitance between reset gate clock and GND | $C_{\phi RG}$ | | 5 | | pF | |
| Capacitance between substrate clock and GND | $C_{\phi SUB}$ | | 270 | | pF | |
| Vertical transfer clock series resistor | $R_1$ | | 47 | | Ω | |
| | $R_{2A}$, $R_{2B}$ | | 91 | | Ω | |
| | $R_{3A}$, $R_{3B}$ | | 68 | | Ω | |
| | $R_4$ | | 24 | | Ω | |
| Vertical transfer clock ground resistor | $R_{GND}$ | | 47 | | Ω | |
| Horizontal transfer clock series resistor | $R_{\phi H1}$, $R_{\phi H2}$ | | 15 | | Ω | |
| Reset gate clock series resistor | $R_{\phi RG}$ | | 56 | | Ω | |




Vertical transfer clock equivalent circuit



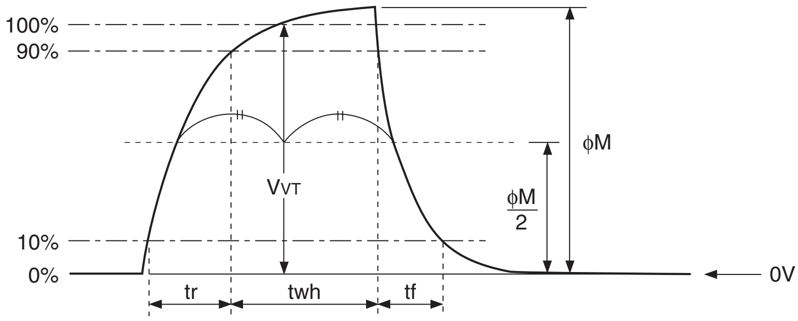

Horizontal transfer clock equivalent circuit



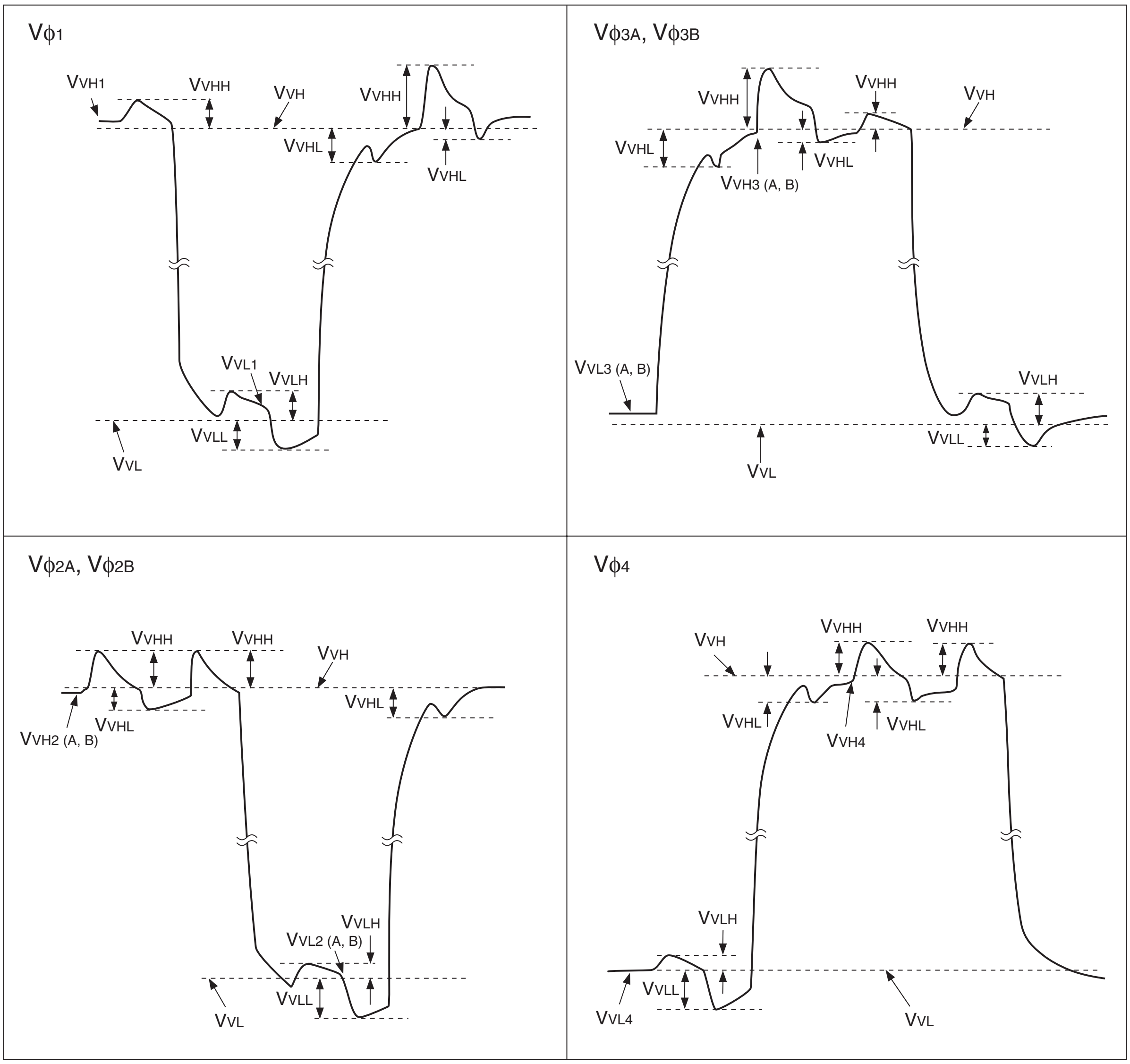

Reset gate clock equivalent circuit

## Drive Clock Waveform Conditions

### 1. Readout clock waveform

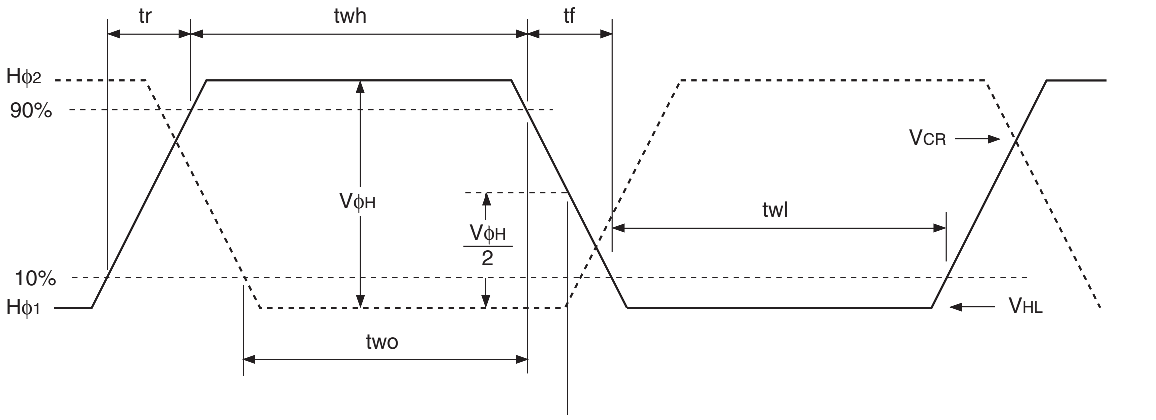



### 2. Vertical transfer clock waveform



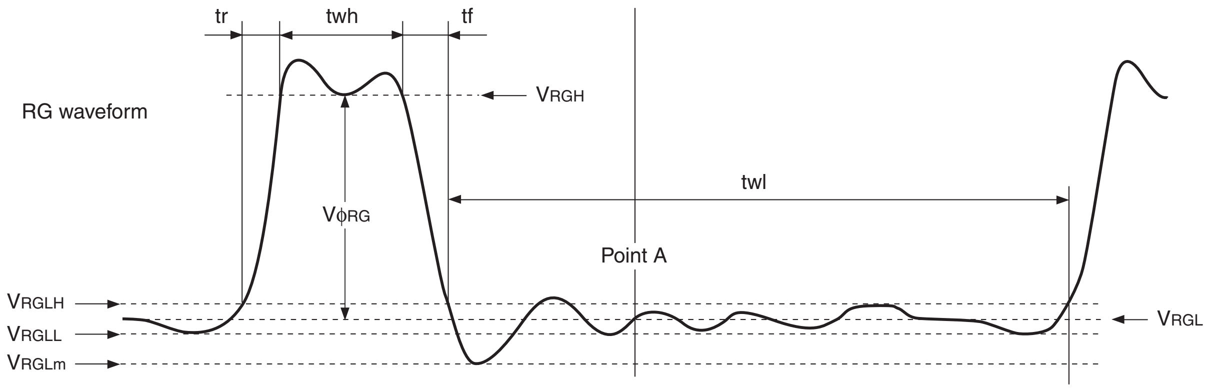

$V_{VH} = (V_{VH1} + V_{VH2\,(A,\,B)})/2$
$V_{VL} = (V_{VL3\,(A,\,B)} + V_{VL4})/2$
$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 4)

### 3. Horizontal transfer clock waveform




Cross-point voltage for the $H\phi_1$ rising side of the horizontal transfer clocks $H\phi_1$ and $H\phi_2$ waveforms is $V_{CR}$.
The overlap period for twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is "two".

### 4. Reset gate clock waveform




$V_{RGLH}$ is the maximum value and $V_{RGLL}$ is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, $V_{RGL}$ is the average value of $V_{RGLH}$ and $V_{RGLL}$.

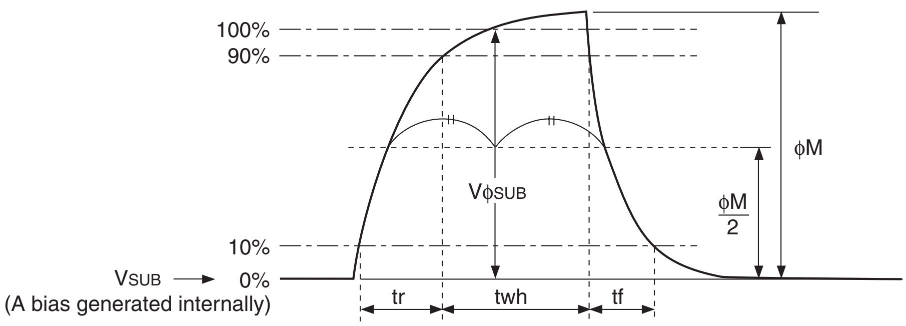
$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$

Assuming $V_{RGH}$ is the minimum value during the interval twh, then:

$V\phi_{RG} = V_{RGH} - V_{RGL}$

Negative overshoot level during the falling edge of RG is $V_{RGLm}$.

### 5. Substrate clock waveform



## Clock Switching Characteristics

| Item | | Symbol | twh | | | twl | | | tr | | | tf | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Readout clock | | VT | 1.8 | 2.0 | | | | | | 0.5 | | | 0.5 | | µs | During readout |
| Vertical transfer clock | | Vφ1, Vφ2 (A, B), Vφ3 (A, B), Vφ4 | | | | | | | | | | 15 | | 250 | ns | *1 |
| Horizontal transfer clock | During imaging | Hφ1 | 10.5 | 14.6 | | 10.5 | 14.6 | | | 6.4 | 10.5 | | 6.4 | 10.5 | ns | *2 |
| | | Hφ2 | 10.5 | 14.6 | | 10.5 | 14.6 | | | 6.4 | 10.5 | | 6.4 | 10.5 | | |
| | During parallel-serial conversion | Hφ1 | | | | | | | | 0.001 | | | | | µs | |
| | | Hφ2 | | | | | | | | 0.001 | | | | | | |
| Reset gate clock | | φRG | 6 | 8 | | | 25.8 | | | 4 | | | 3 | | ns | |
| Substrate clock | | φSUB | 0.63 | 0.73 | | | | | | | 0.5 | | | 0.5 | µs | When draining charge |

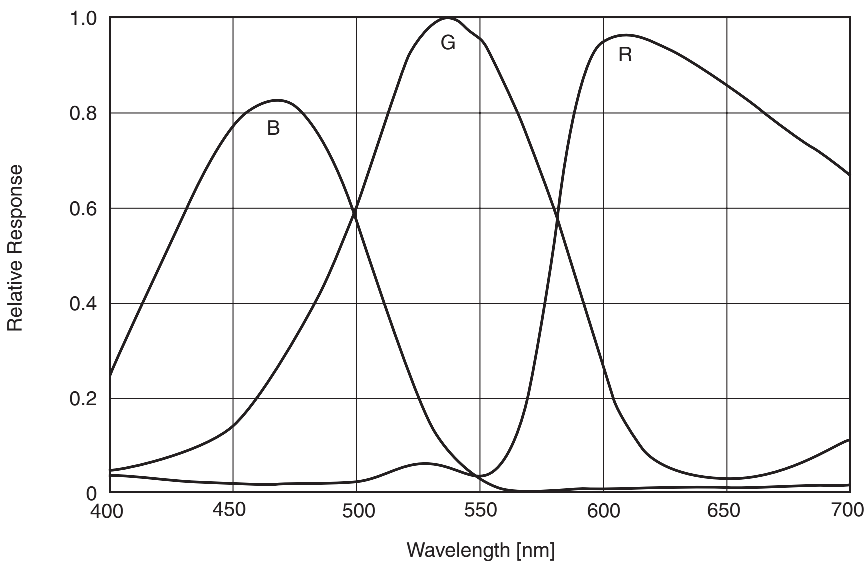
*1 When vertical transfer clock driver CXD1267AN is used.

*2 tf ≥ tr – 2ns, and the cross-point voltage (VCR) for the Hφ1 rising side of the Hφ1 and Hφ2 waveforms must be at least VφH/2 [V].

| Item | Symbol | two | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Horizontal transfer clock | Hφ1, Hφ2 | 10.5 | 14.6 | | ns | |

## Spectral Sensitivity Characteristics

(excludes lens characteristics and light source characteristics)

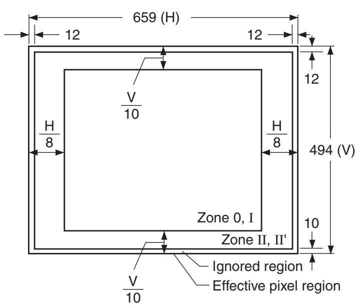


## Image Sensor Characteristics

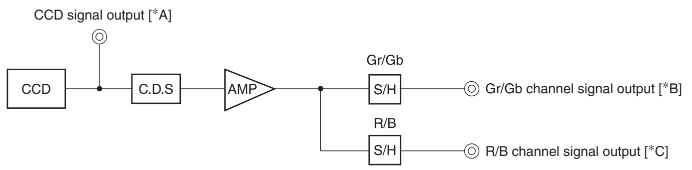
(Ta = 25°C)

| Item | | Symbol | Min. | Typ. | Max. | Unit | Measure-ment method | Remarks |
|---|---|---|---|---|---|---|---|---|
| G Sensitivity | | Sg | 600 | 750 | | mV | 1 | 1/30s accumulation |
| Sensitivity ratio | R | Rr | 0.4 | | 0.7 | | 1 | |
| | B | Rb | 0.3 | | 0.6 | | 1 | |
| Saturation signal | | Ysat | 650 | | | mV | 2 | Ta = 60°C |
| Smear | | Sm | | –102 | –92 | dB | 3 | |
| Video signal shading | | SHg | | | 20 | % | 4 | Zone 0 and I |
| | | | | | 25 | % | 4 | Zone 0 to II' |
| Uniformity between video signal channels | | ΔSrg | | | 8 | % | 5 | |
| | | ΔSbg | | | 8 | % | 5 | |
| Dark signal | | Vdt | | | 4 | mV | 6 | Ta = 60°C, 1/30s accumulation |
| Dark signal shading | | ΔVdt | | | 1 | mV | 7 | Ta = 60°C, 1/30s accumulation |
| Line crawl G | | Lcg | | | 3.8 | % | 8 | |
| Line crawl R | | Lcr | | | 3.8 | % | 8 | |
| Line crawl B | | Lcb | | | 3.8 | % | 8 | |
| Lag | | Lag | | | 0.5 | % | 9 | |

## Zone Definition of Video Signal Shading




## Measurement System



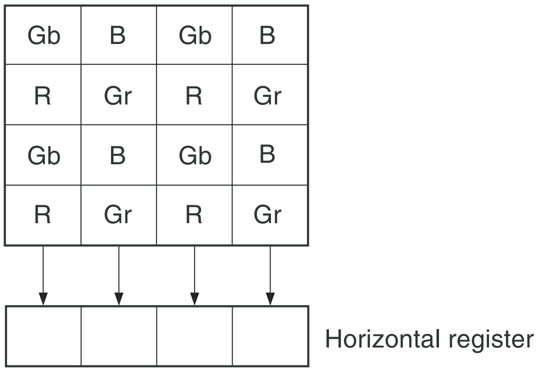

Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] to [*C] equals 1.

## Image Sensor Characteristics Measurement Method

### Measurement conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

### Color coding of this image sensor & Readout




**Color Coding Diagram**

The primary color filters of this image sensor are arranged in the layout shown in the figure above (Bayer array). Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.

All pixel signals are output successively in a 1/60s period.
The R signal and Gr signal lines and Gb signal and B signal lines are output successively.

**Definition of standard imaging conditions**

◆ Standard imaging condition I:
Use a pattern box (luminance: 706cd/$m^2$, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, sensitivity ratio
   Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs ($V_{Gr}$, $V_{Gb}$, $V_R$ and $V_B$) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

   $V_G = (V_{Gr} + V_{Gb})/2$
   $Sg = V_G \times (100/30)$ [mV]
   $Rr = V_R/V_G$
   $Rb = V_B/V_G$

2. Saturation signal
   Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
   Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV.
   After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (VSm [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

   $Sm = 20 \times \log \{Vsm \div ((Gra + Gb + Ra + Ba)/4) \times (1/500) \times (1/10)\}$ (1/10V method conversion value)

4. Video signal shading
   Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum value (Grmax [mV]) and minimum value (Grmin [mV]) of the Gr signal and substitute the values into the following formula.

   $SHg = (Gmax – Gmin)/150 \times 100$ [%]

5. Uniformity between video signal channels
   After the measurement item 4, measure the maximum (Rmax [mV]) and minimum (Rmin [mV]) values of the R signal and the maximum (Bmax [mV]) and minimum (Bmin [mV]) values of the B signal, and substitute the values into the following formula.

   $\Delta Srg = (Rmax – Rmin)/150 \times 100$ [%]
   $\Delta Sbg = (Bmax – Bmin)/150 \times 100$ [%]

6. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
   After the measurement item 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

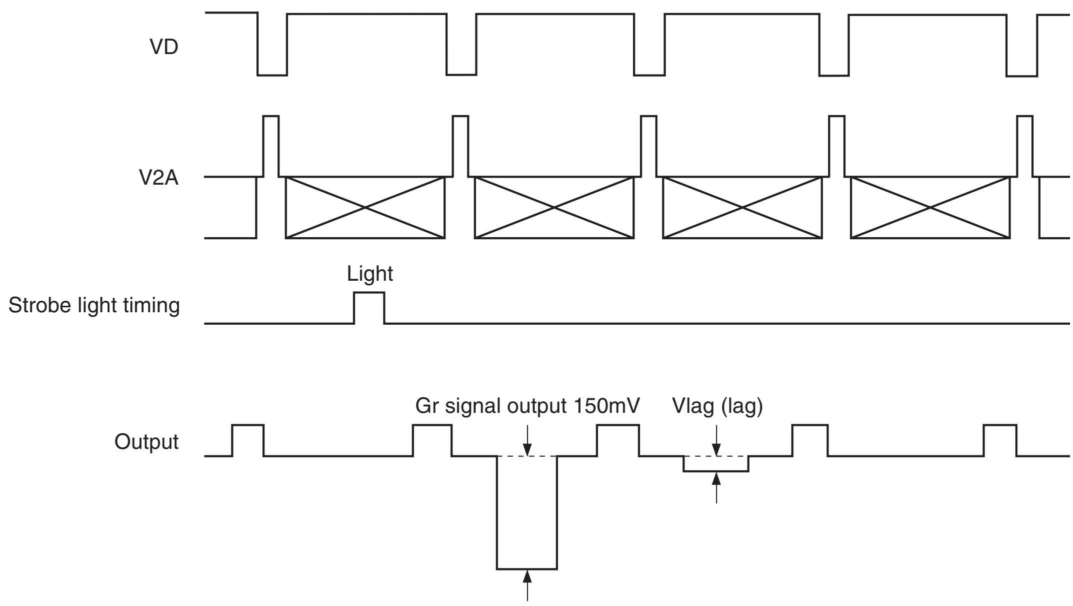
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

8. Line crawl
   Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb [mV]) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

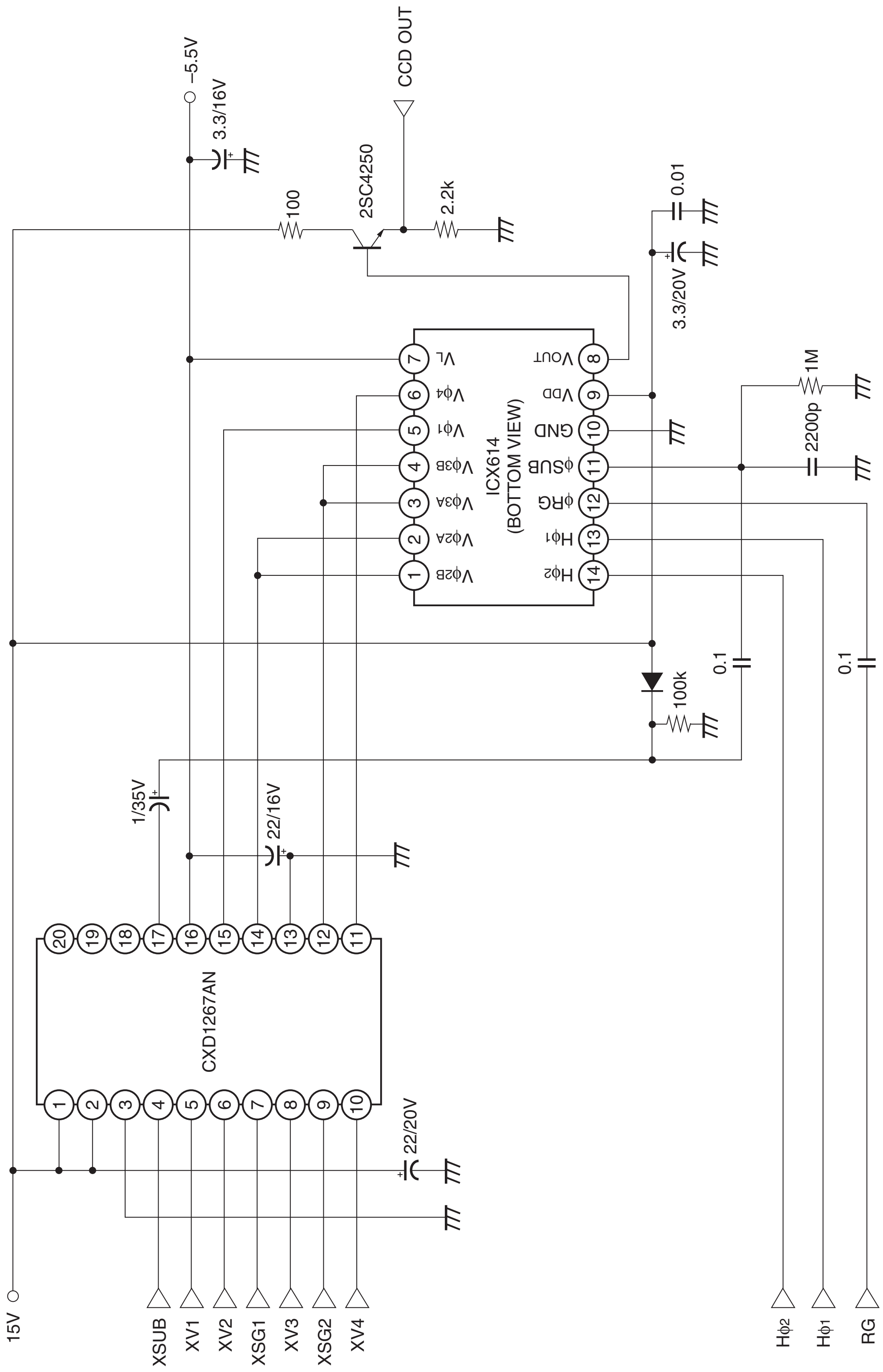
   $Lci = (\Delta Gli/Gai) \times 100$ [%]   (i = r, g, b)

9. Lag
   Adjust the Gr signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/150) \times 100$ [%]

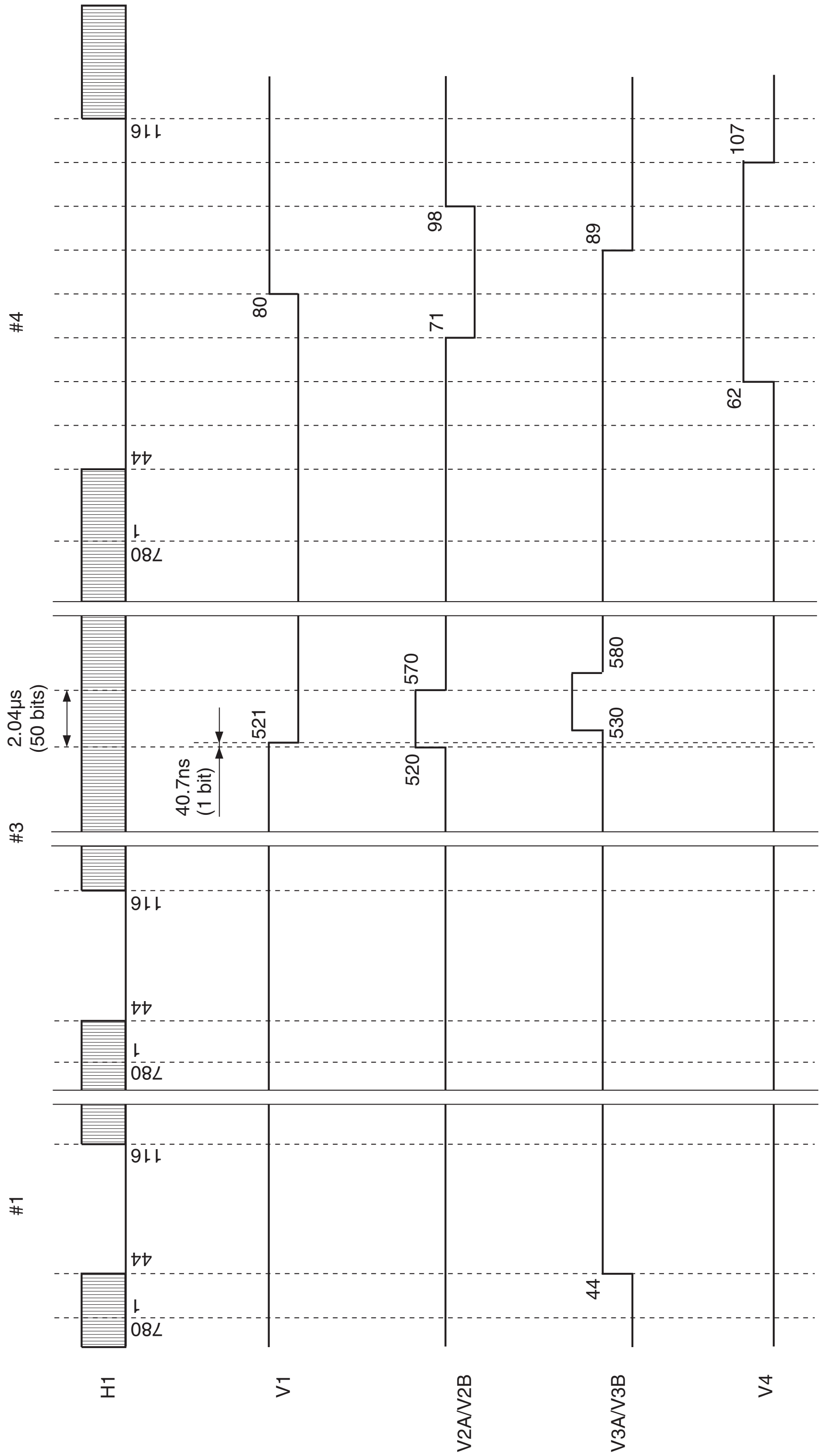


## Driving Circuit



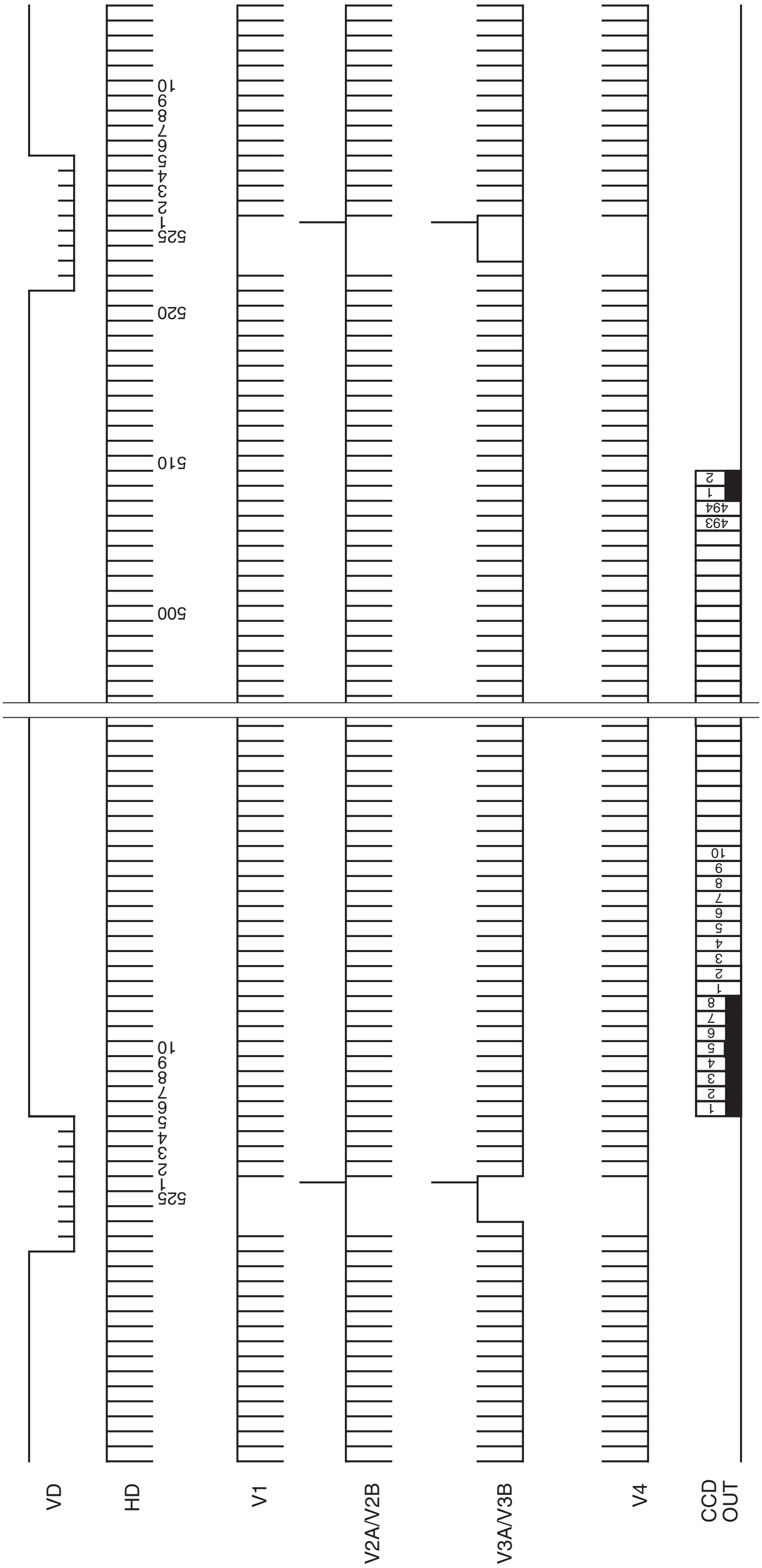
## Drive Timing Chart

### Readout Portion



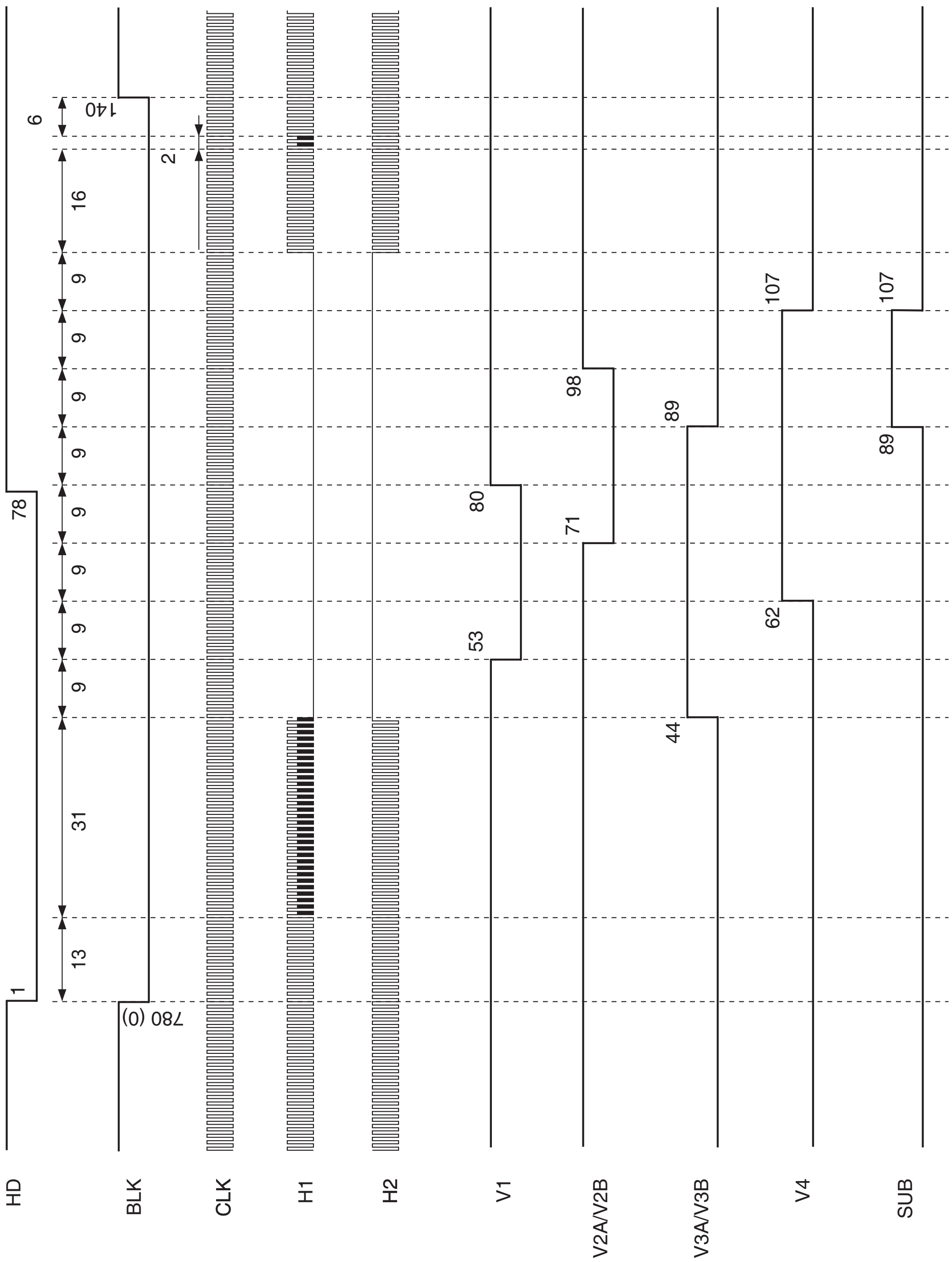
## Drive Timing Chart

### Vertical Sync



## Drive Timing Chart

### Horizontal Sync



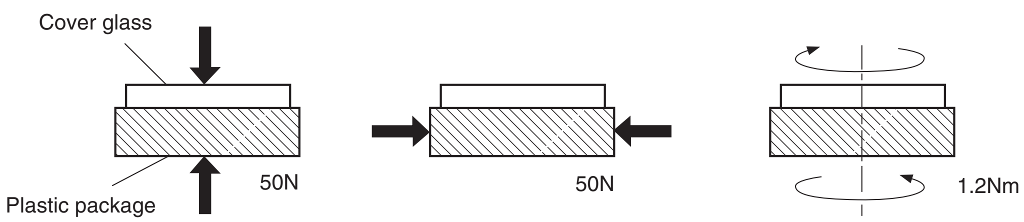
## Notes On Handling

1. Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   (1) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
   (2) Use a wrist strap when handling directly.
   (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
   (4) Ionized air is recommended for discharge when handling CCD image sensors.
   (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Soldering
   (1) Make sure the package temperature does not exceed 80°C.
   (2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in 2 seconds or less. For repairs and remount, cool sufficiently.
   (3) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3. Protection from dust and dirt
   Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.
   (1) Perform all lens assembly and other work in a clean room (class 1000 or less).
   (2) Do not touch the glass surface with hand and make any object contact with it. If dust or other is stuck to a glass surface, blow it off with an air blower. (For dust stuck through static electricity, ionized air is recommended.)
   (3) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

4. Installing (attaching)
   (1) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)




**Compressive strength** **Torsional strength**

   (2) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
   (3) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
   (4) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

(5) If the lead bend repeatedly and the metal, etc., clash or rub against the package, dust may be generated by the fragments of resin.

(6) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

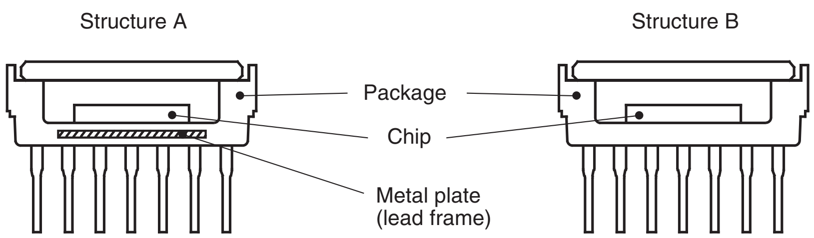
5. Others

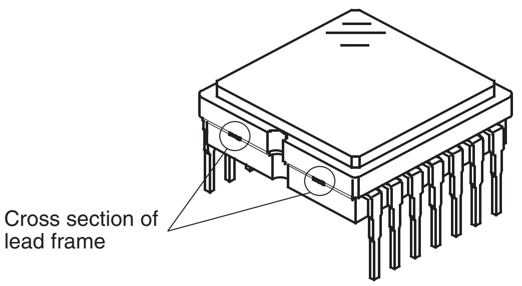
(1) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminance objects are imaged with the exposure level controlled by electronic-iris, the luminance of the image-plane may become excessive and discoloration of the color filters may be accelerated. In such a case, arrangements such as using an automatic iris with the imaging lens or automatically closing the shutter during power-off are advisable. For continuous use under harsh conditions exceeding the normal conditions of use, consult your Sony representative.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

(3) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

(4) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.



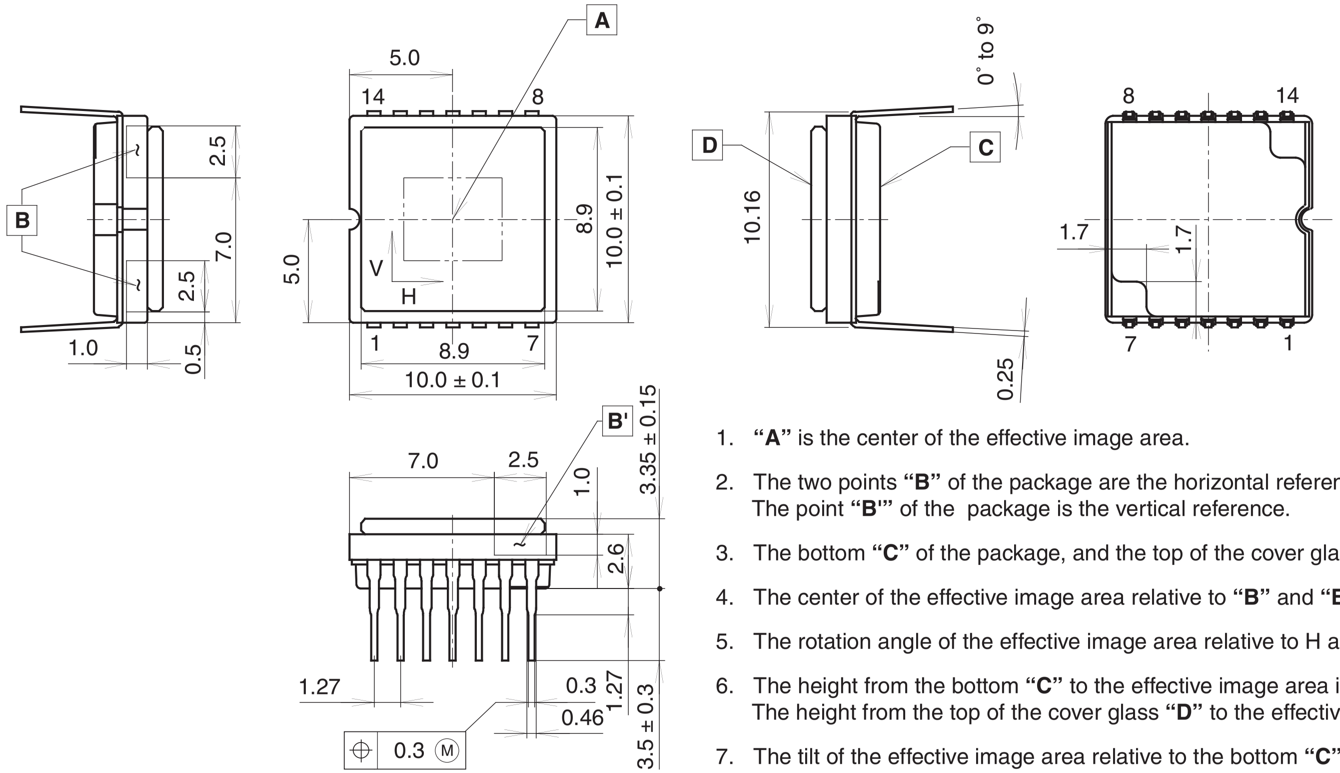




The cross section of lead frame can be seen on the side of the package for structure A.

## Package Outline

(Unit: mm)

14 pin DIP (400mil)




1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (5.0, 5.0) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 25μm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 25μm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.
10. Cover glass defect
    Edge part
    Length : no matter, Width : less than 0.5mm, Depth : less than the thickness of the glass.
    Corner part
    Length : less than 1.5mm, Depth : less than the thickness of the glass.

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | Plastic |
| LEAD TREATMENT | GOLD PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE MASS | 0.60g |
| DRAWING NUMBER | AS-D3-02(E) |