ID2103

High Side & Low Side Gate Drive IC

General Description

The ID2103 is a high voltage, high speed power MOSFET and IGBT driver based on P_SUB P_EPI process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT in a half-bridge configuration which operates up to 600 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

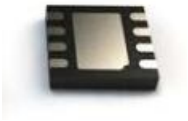
Features

- Fully operational to +600 V
- 3.3 V logic compatible
- dV/dt Immunity ±50 V/nsec
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for low side channel
- Output Source / Sink Current Capability 210 mA / 360mA
- -5V negative Vs ability
- Matched propagation delay for both channels

Applications

- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Half−Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Drive Converters

Package Options



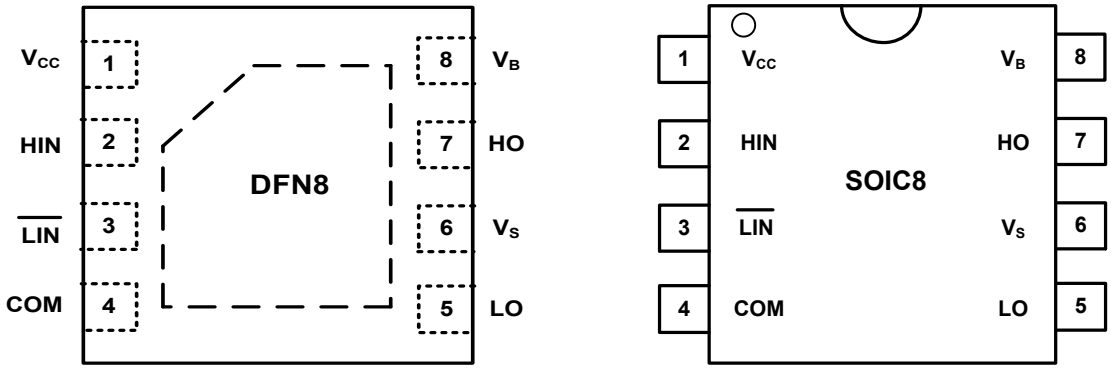
DFN 8

SOP8

Order Information

Part Number	Order Code	Package	Type
ID2103	ID2103SEC-R1	SOIC8	Reel
ID2103	ID2103DEC-R1	DFN8	Reel

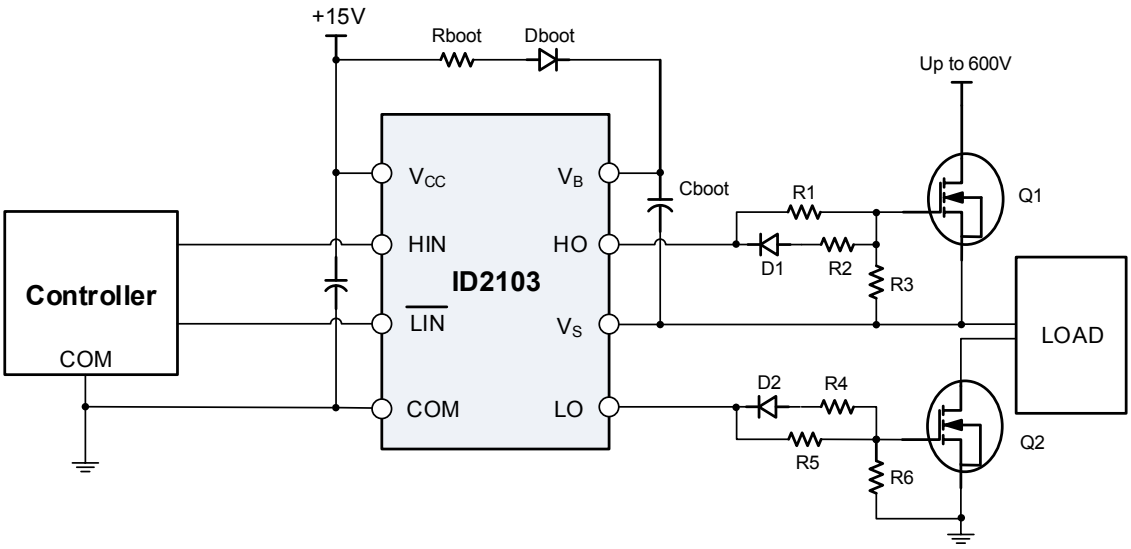
Pin Configuration



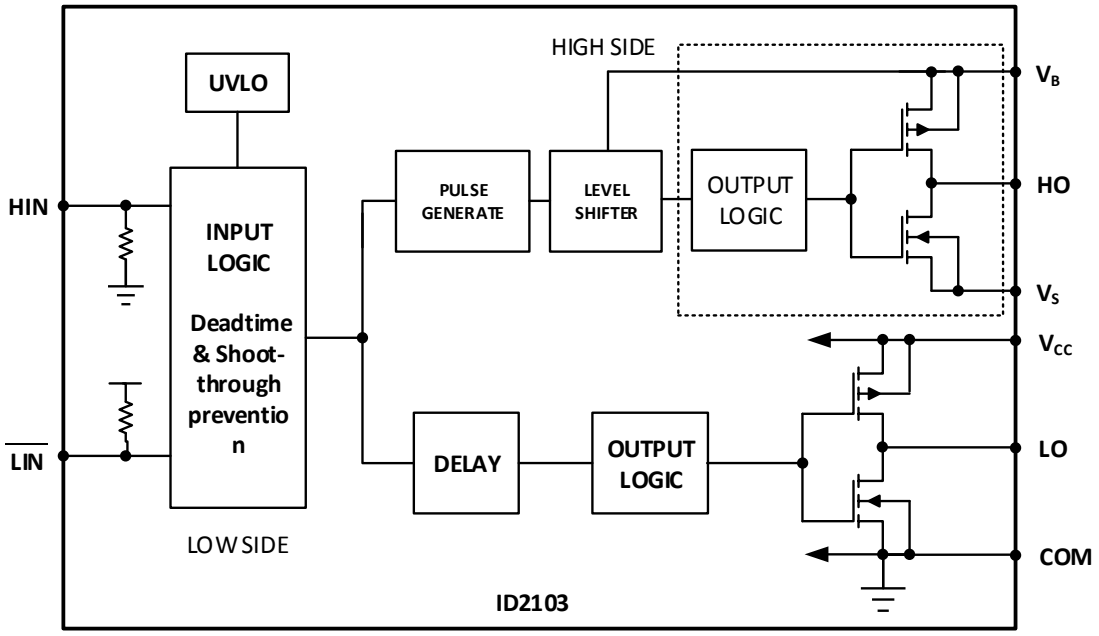
Pin Definitions

PIN NO.	PIN NAME	PIN FUNCTION
1	V_{CC}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	$\overline{LIN}$	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output, out of phase with LIN
6	V_S	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V_B	High side floating supply

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.

The absolute maximum ratings are stress ratings only at T_A=25°C, unless otherwise specified.

Symbol	Definition		MIN.	MAX.	Units
V_B	High side floating supply		-0.3	622[Note1]	V
V_S	High side floating supply return		V_B – 20	V_B + 0.3	
V_{HO}	High side gate drive output		V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply		-0.3	22	
V_{LO}	Low side gate drive output		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & $\overline{LIN}$		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		--	50	V/ns
ESD	HBM Model		2.5		kV
	CDM Model		200		V
P_D	Package Power Dissipation @ TA ≤25°C	8 Lead SOIC	--	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	8 Lead SOIC	--	200	°C /W
T_J	Junction Temperature		--	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		--	300	

Note 1: Max VB 622V is only for SOIC8.

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	--	600[Note2]	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & $\overline{LIN}$)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 2: Max VS of DFN package is 120V.

Dynamic Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	TYP.	MAX.	Units
t_{ONH}	High side turn on propagation delay	630	820	ns
t_{OFFH}	High side turn off propagation delay	140	220	
t_{ONL}	Low side turn on propagation delay	630	820	
t_{OFFL}	Low side turn off propagation delay	140	220	
MT	Delay matching time (t_{ON}, t_{OFF})	-	50	
DT	Dead time	500	650	
t_R	Turn on rising time	85	120	
t_F	Turn off falling time	35	90	

Static Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{UVCC+}	V_{CC} supply under-voltage positive going threshold	--	8.7	--	V
V_{UVCC-}	V_{CC} supply under-voltage negative going threshold	--	8	--	
I_{LK}	High-side floating supply leakage current	--	--	10	μA
I_{QBS}	Quiescent V_{BS} supply current	--	30	55	
I_{QCC}	Quiescent V_{CC} supply current	--	150	270	
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	--	--	0.1	V
V_{OL}	Low level output voltage drop, V_O	--	--	0.1	
I_{O+}	Output high short circuit pulsed current	130	210	--	mA
I_{O-}	Output low short circuit pulsed current	270	360	--	
V_{IH}	High level input threshold voltage	2.5	--	--	V
V_{IL}	Low level input threshold voltage	--	--	0.8	
I_{IN+}	Logic “1” input bias current (HIN “1” & LIN “0”)	--	6	20	μA
I_{IN-}	Logic “0” input bias current (HIN “0” & LIN “1”)	--	--	15	

Function Timing Diagram

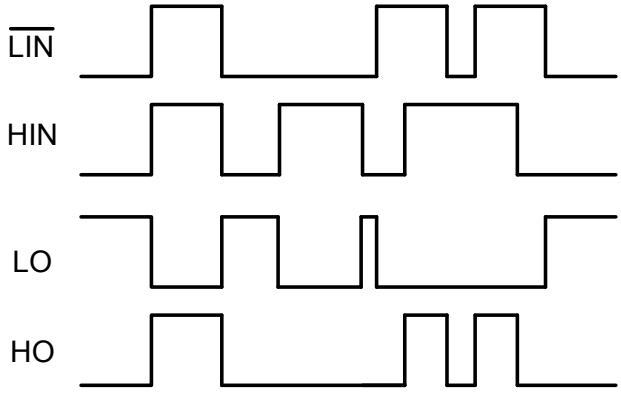


Fig.1 Input and output timing waveform

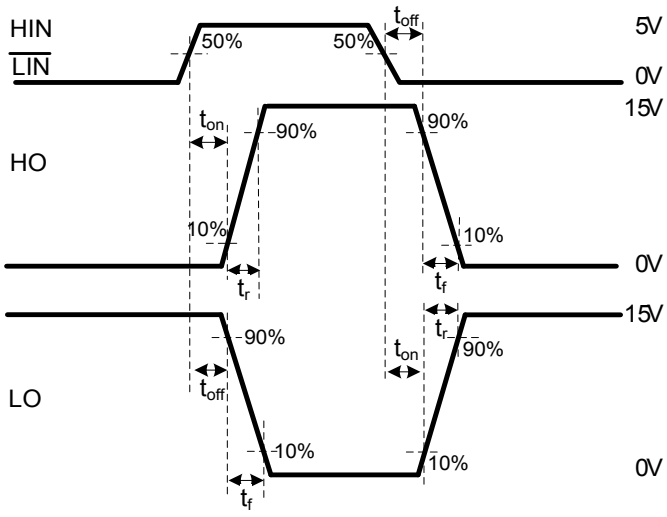


Fig.2 Propagation and Rise/Fall time definition

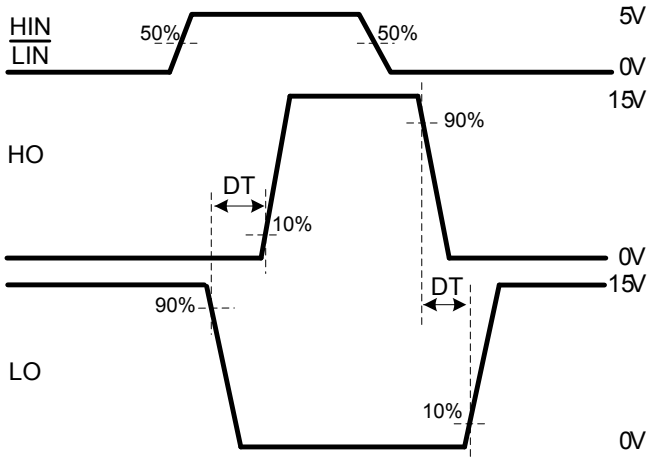


Fig.3 Dead time definition

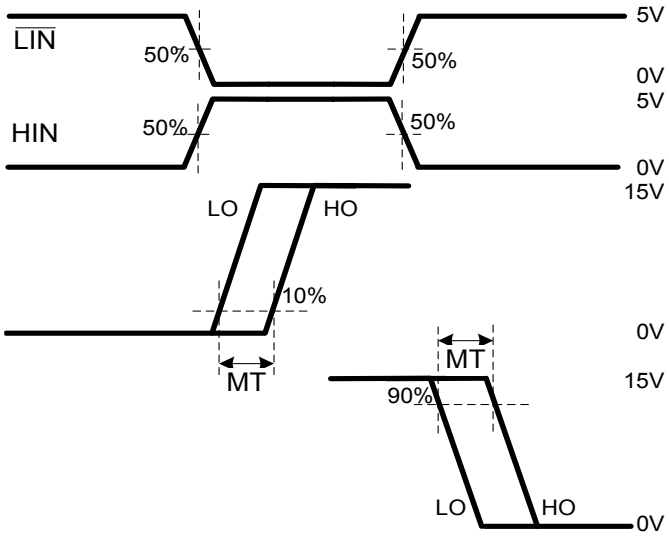


Fig.4 Delay matching definition

Characterization Curves

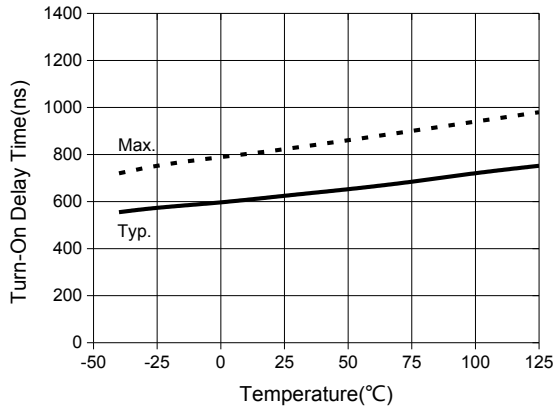


Fig.5 Turn-On Delay vs. Temperature

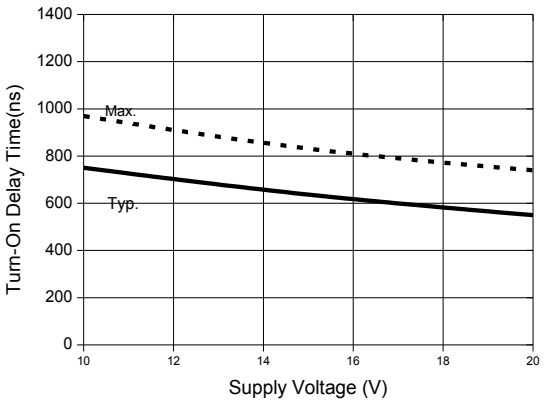


Fig.6 Turn-On Delay vs. Voltage

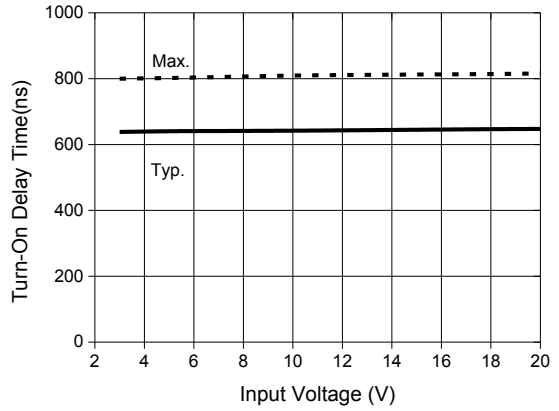


Fig.7 Turn-On Delay Time vs. Input Voltage

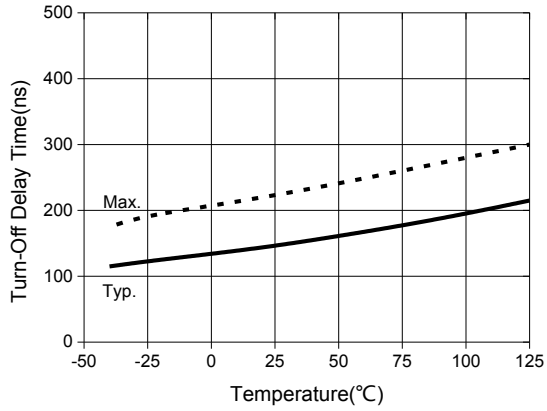


Fig.8 Turn-Off Delay Time vs. Temperature

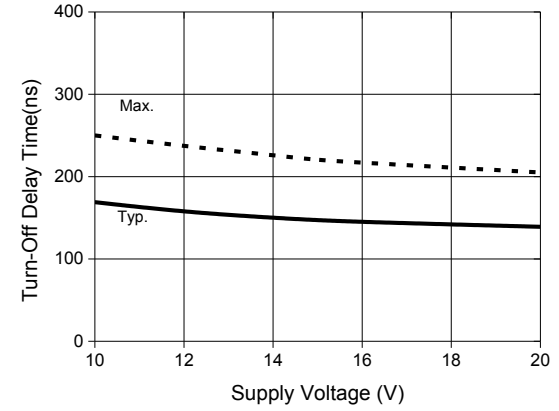


Fig.9 Turn-Off Delay Time vs. Supply Voltage

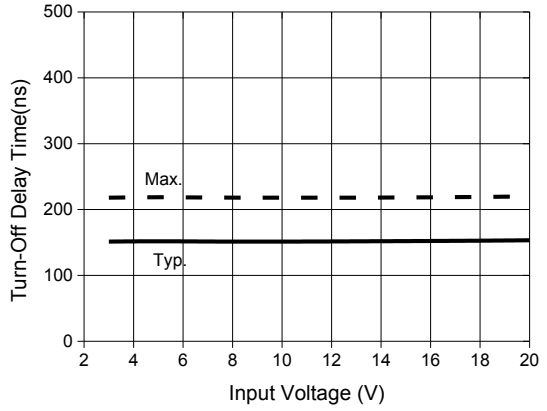


Fig.10 Turn-Off Delay Time vs. Input Voltage

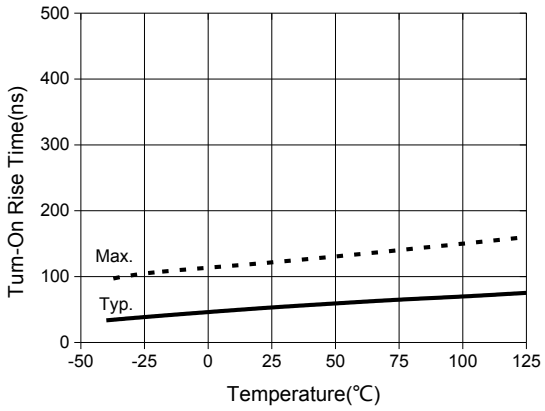


Fig.11 Turn-On Rise Time vs. Temperature

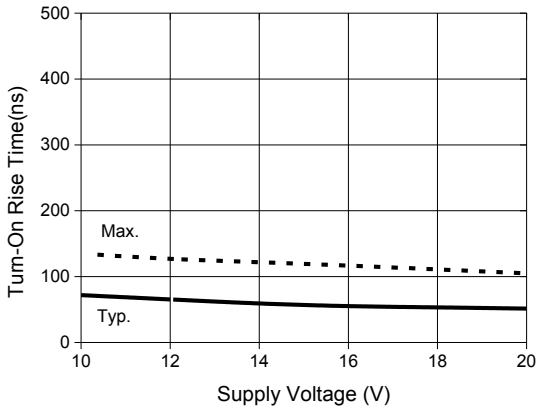


Fig.12 Turn-On Rise Time vs. Supply Voltage

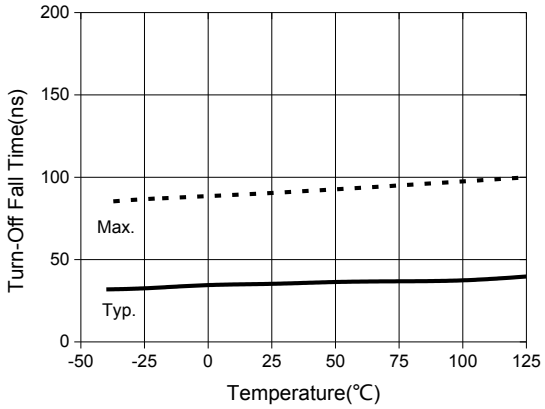


Fig.13 Turn-Off Fall Time vs. Temperature

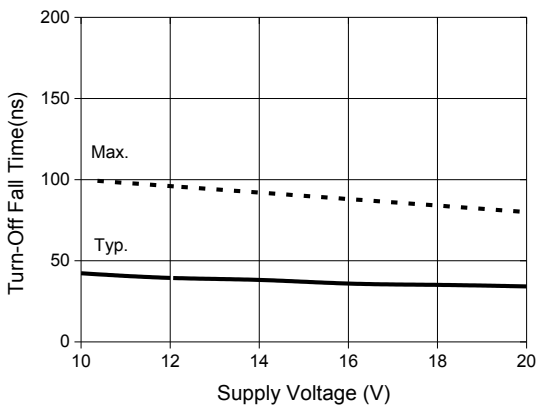


Fig.14 Turn-Off Fall Time vs. Supply Voltage

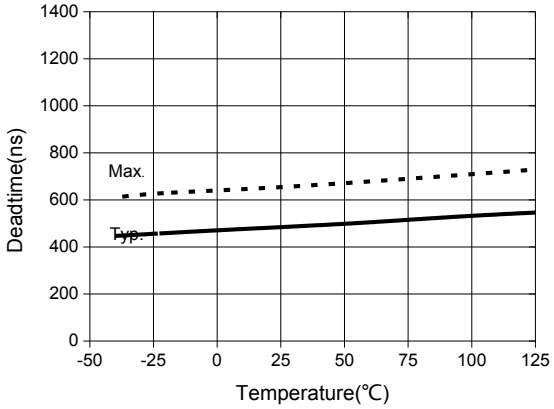


Fig.15 Dead time vs. Temperature

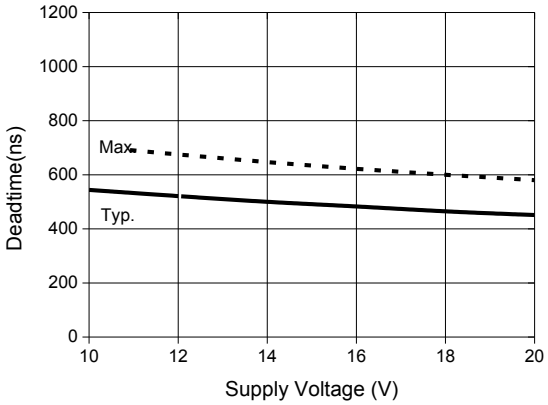


Fig.16 Dead time vs. Supply Voltage

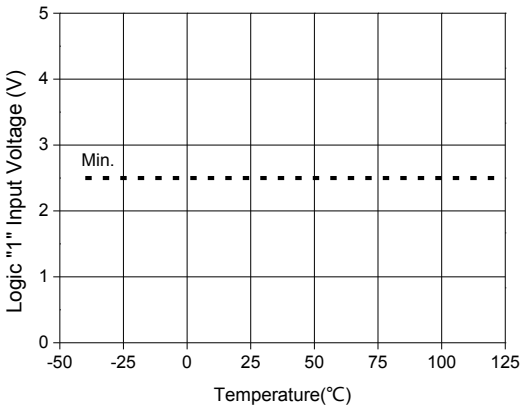


Fig.17 Logic "1" Input Voltage vs. Temperature

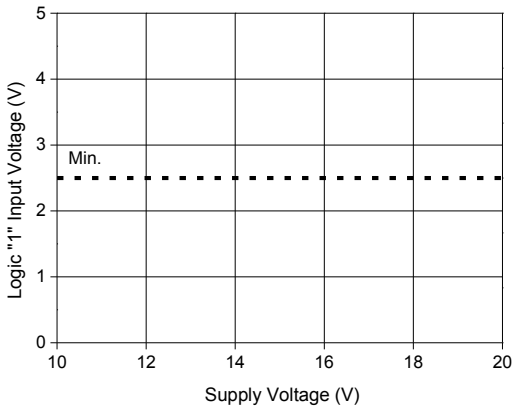


Fig.18 Logic "1" Input Voltage vs. Supply Voltage

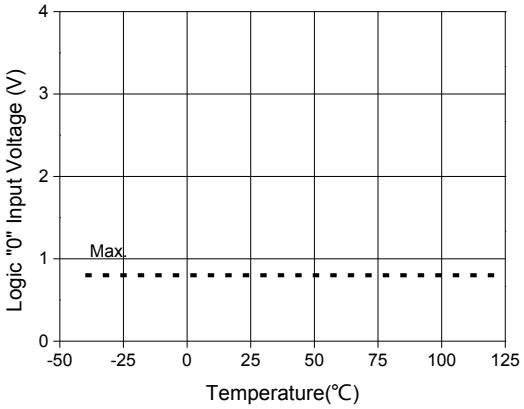


Fig.19 Logic "0" Input Voltage vs. Temperature

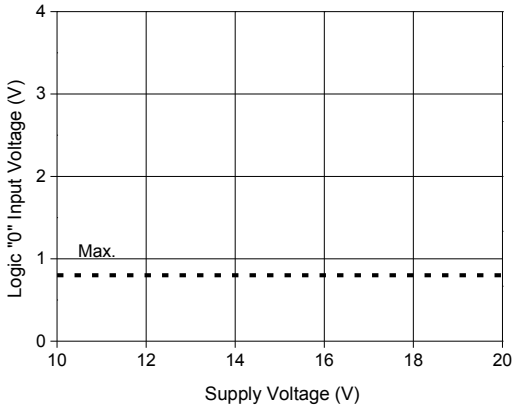


Fig.20 Logic "0" Input Voltage vs. Supply Voltage

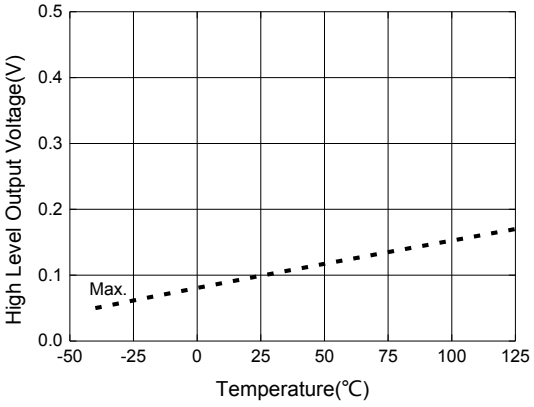


Fig.21 High Level Output vs. Temperature

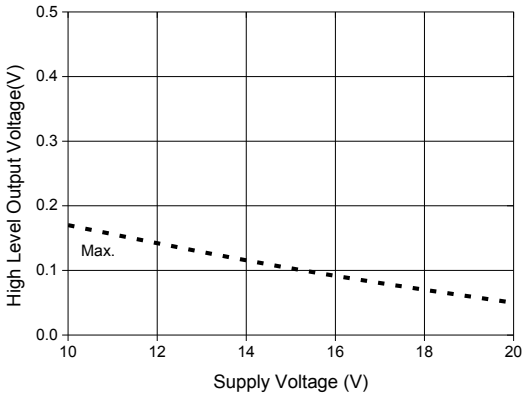


Fig.22 High Level Output vs. Supply Voltage

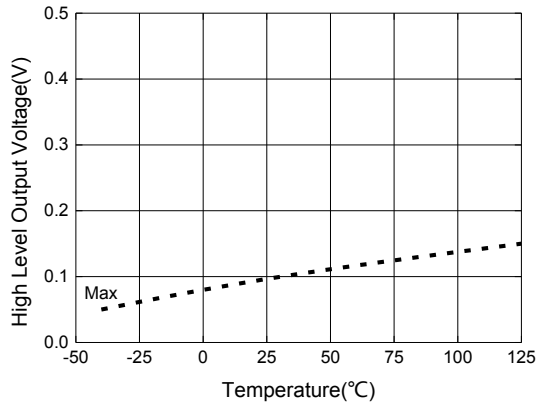


Fig.23 Low Level Output vs. Temperature

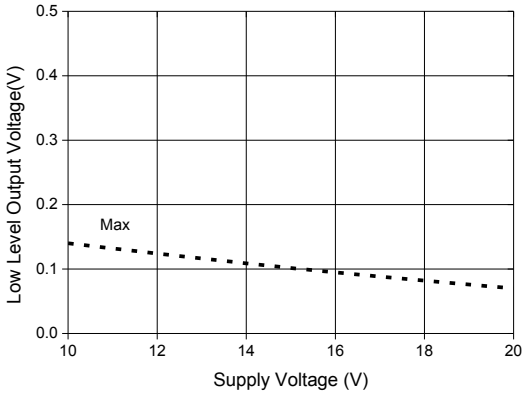


Fig.24 Low Level Output vs. Supply Voltage

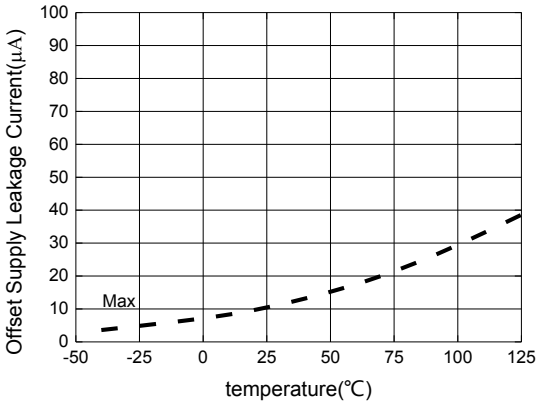


Fig.25 Offset Supply Current vs. Temperature

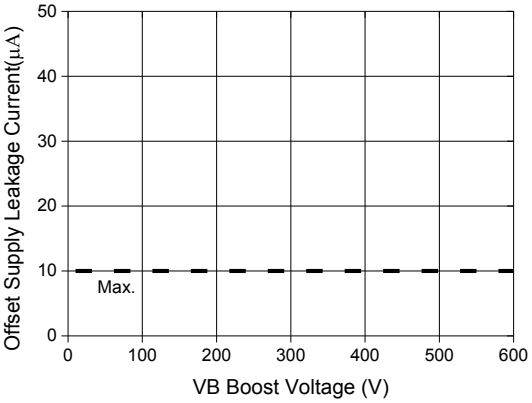


Fig.26 Offset Supply Current vs. Boost Voltage

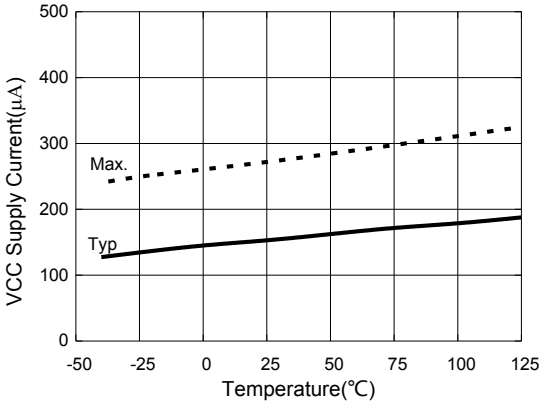


Fig.27 VCC Supply Current vs. Temperature

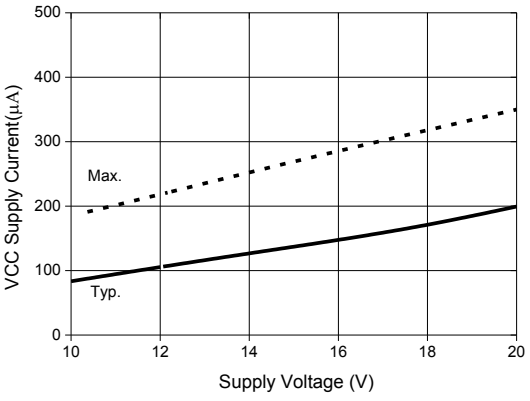


Fig.28 VCC Supply Current vs. Supply Voltage

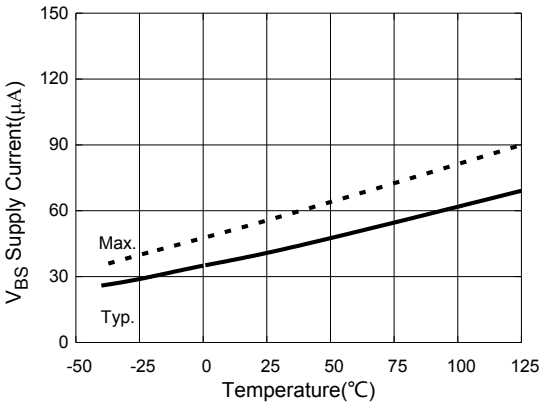


Fig.29 VBS Supply Current vs. Temperature

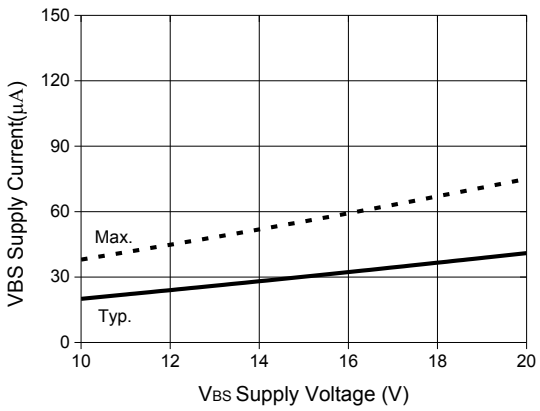


Fig.30 VBS Supply Current vs. Supply Voltage

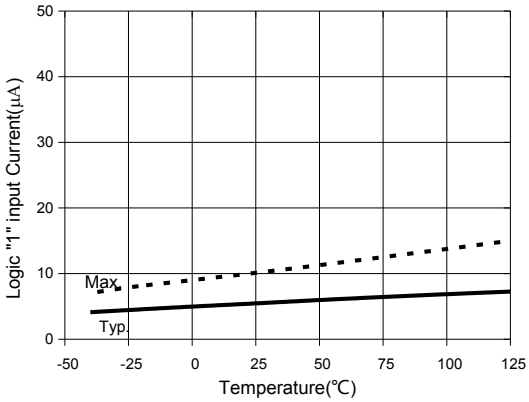


Fig.31 Logic "1" Input Current vs. Temperature

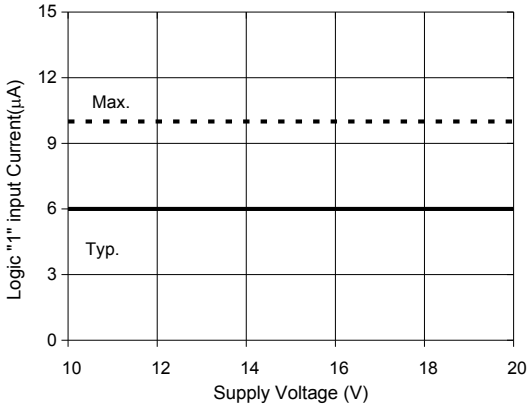


Fig.32 Logic "1" Input Current vs. Supply Voltage

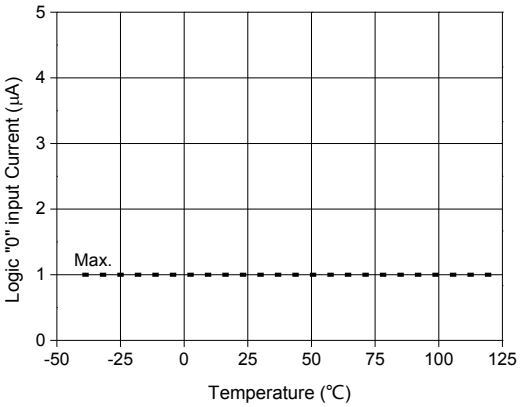


Fig.33 Logic "0" Input Current vs. Temperature

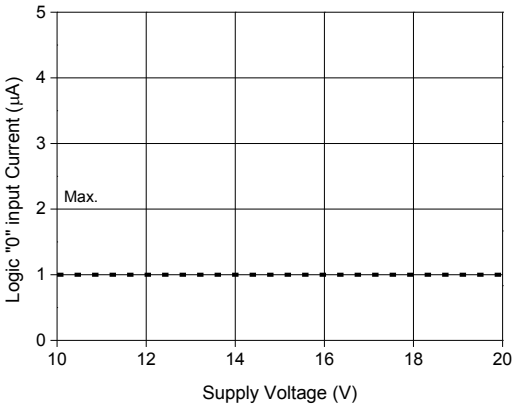


Fig.34 Logic "0" Input Current vs. Supply Voltage

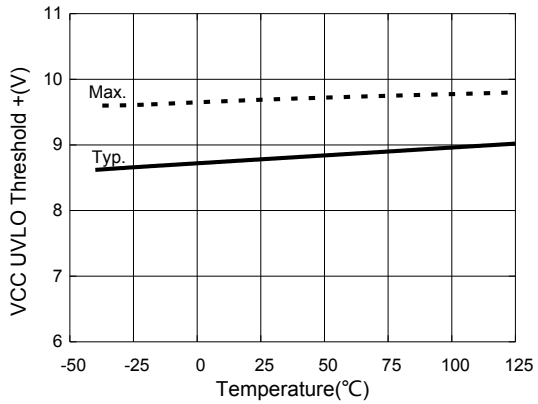


Fig.35 VCC Under voltage Threshold(+) vs. Temperature

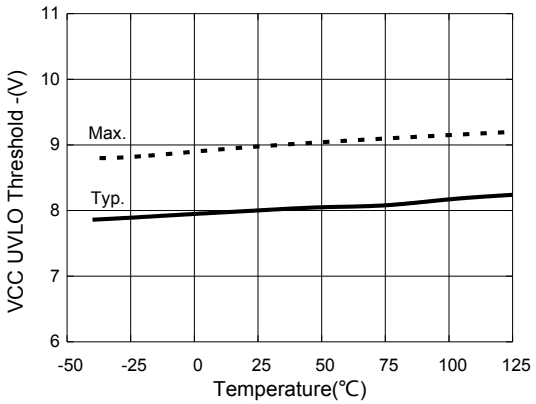


Fig.36 VCC Under voltage Threshold(-) vs. Temperature

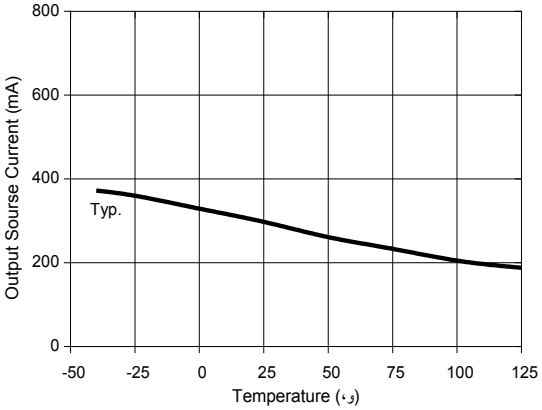


Fig.37 Output Source Current vs. Temperature

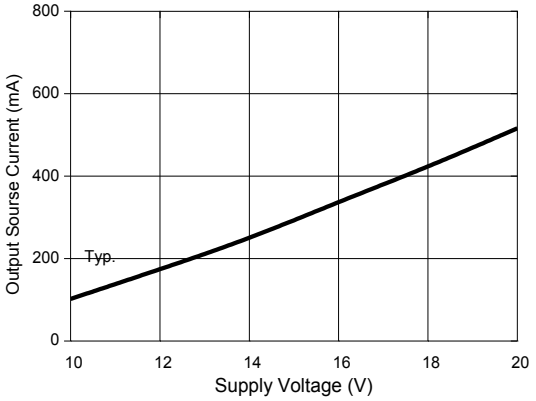


Fig.38 Output Source Current vs. Supply Voltage

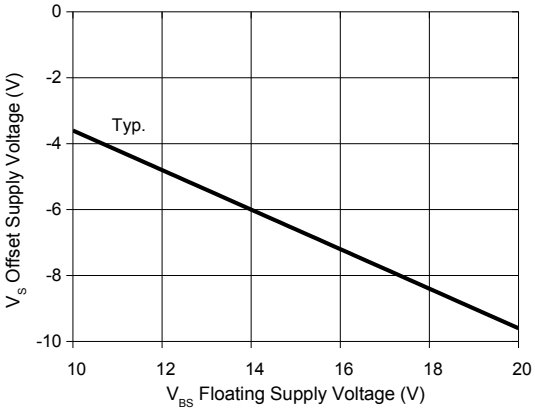


Fig.39 Maximum VS Negative Offset vs. Supply Voltage

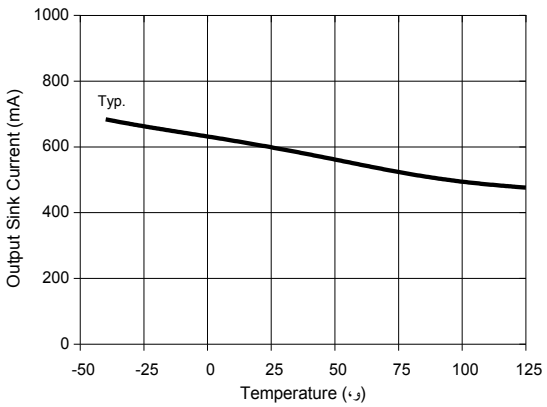


Fig.40 Output Sink Current vs. Temperature

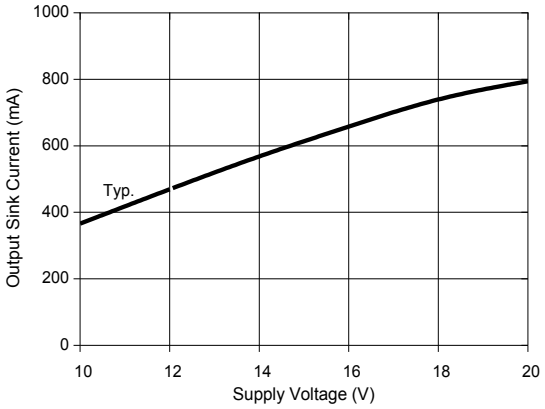


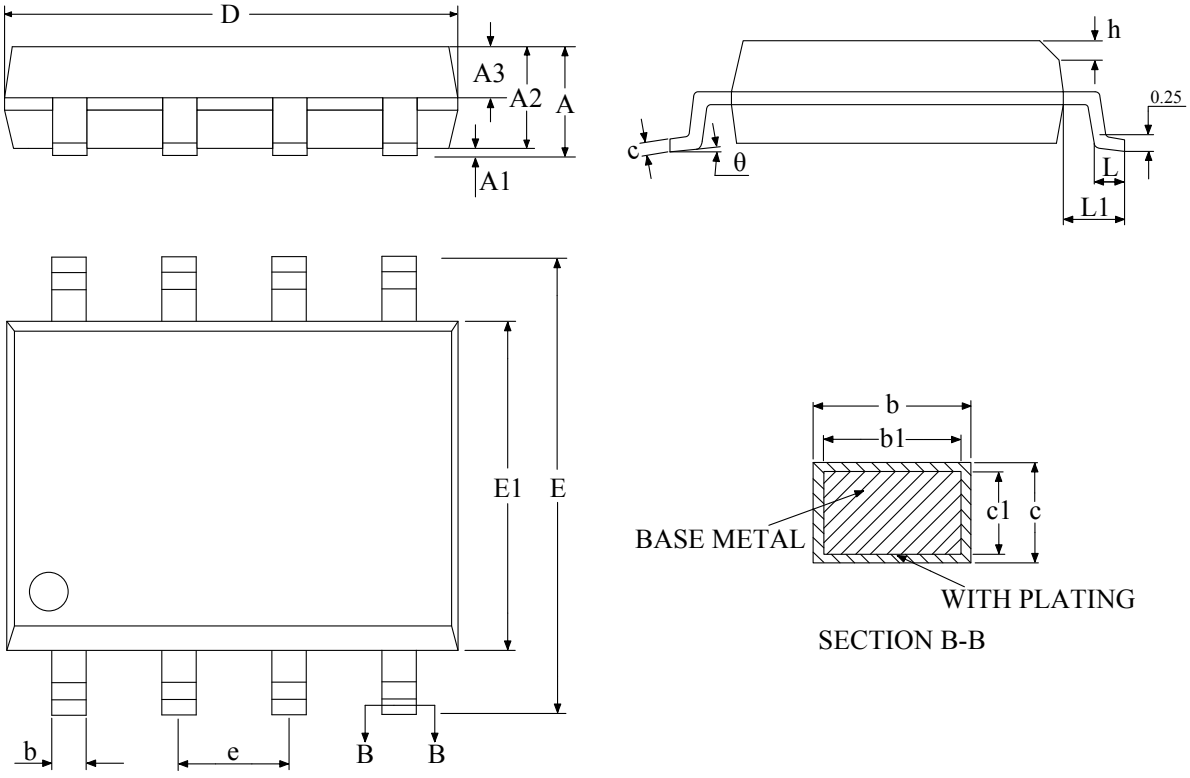
Fig.41 Output Sink Current vs. Supply Voltage

Package Information

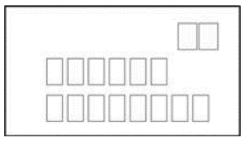
SOIC8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Package Outlines



SOIC8 Package Mark Information



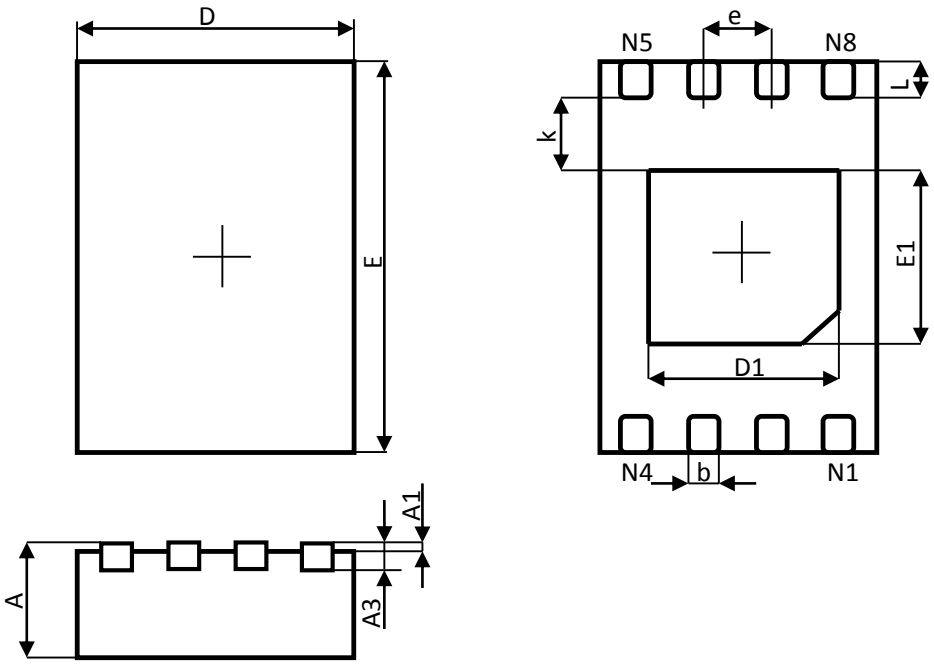
TOP Mark
Logo
ID2103
YWWXXXXX[Note3]

Note3：Y：Year code，WW：Week codes，XXXXX：Package codes

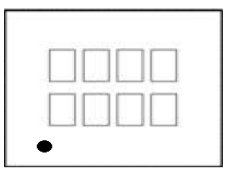
DFN8 Package Dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min. (mm)	Max. (mm)	Min.(inch)	Max.(inch)
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

Package Outlines



DFN8 Package Mark Information



TOP Mark
ID2103
AYWX[Note4]
Pin 1 indicator point

Note4：A：Internal code，Y：Year code，W：Week codes， X：Package codes