ID2206D

High Side & Low Side Gate Drive IC

General Description

The ID2206D is a high voltage, high speed power MOSFET driver with independent high and low side referenced output channels based on P_SUB P_EPI process. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 600 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. ID2206D is the version with LO in phase with LIN.

Features

- Fully operational to +600 V
- 3.3 V input logic compatible
- dV/dt Immunity ±50 V/nsec
- Gate drive supply range from 10 V to 18 V
- Typically output Source/Sink current capability 200mA/350mA
- Typically -7V negative Vs bias capability
- Matched propagation delay for both channels
- ID2206D (LO is in phase with LIN)
- Built-in bootstrap diode

Applications

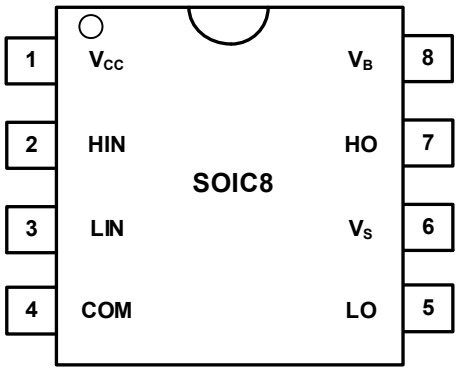
- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Half−Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Drive Converters

Package Options

Order Information

Part Number	Order Code	Package	Type
ID2206D	ID2206DSEC-R1	SOIC8	Reel

Pin Configuration



ID2206D

Pin Definitions

PIN NO.	PIN NAME	PIN FUNCTION
1	V_{CC}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	LIN	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output
6	V_S	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V_B	High side floating supply

Typical Application Circuit

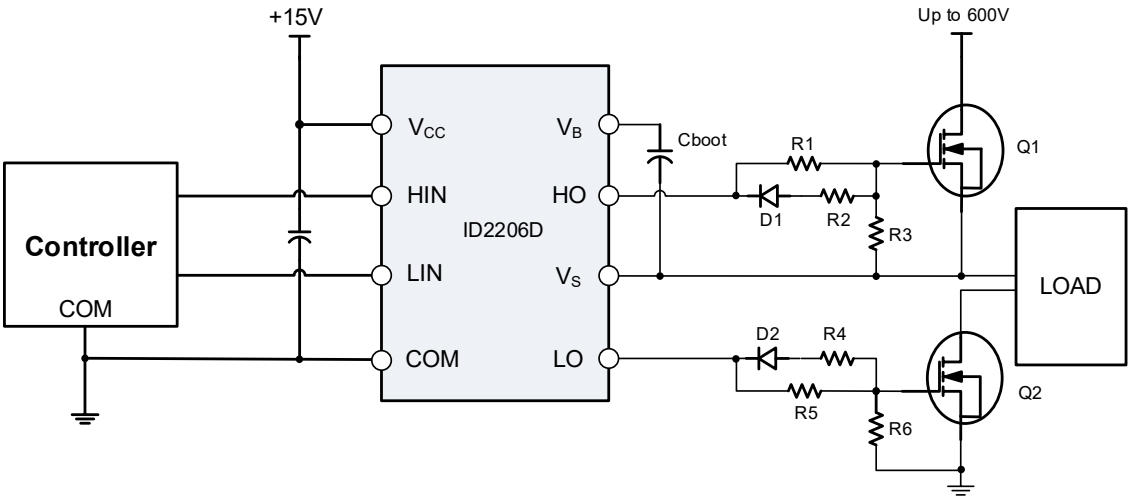


Fig.1 Typical application of ID2206D

Functional Block Diagram

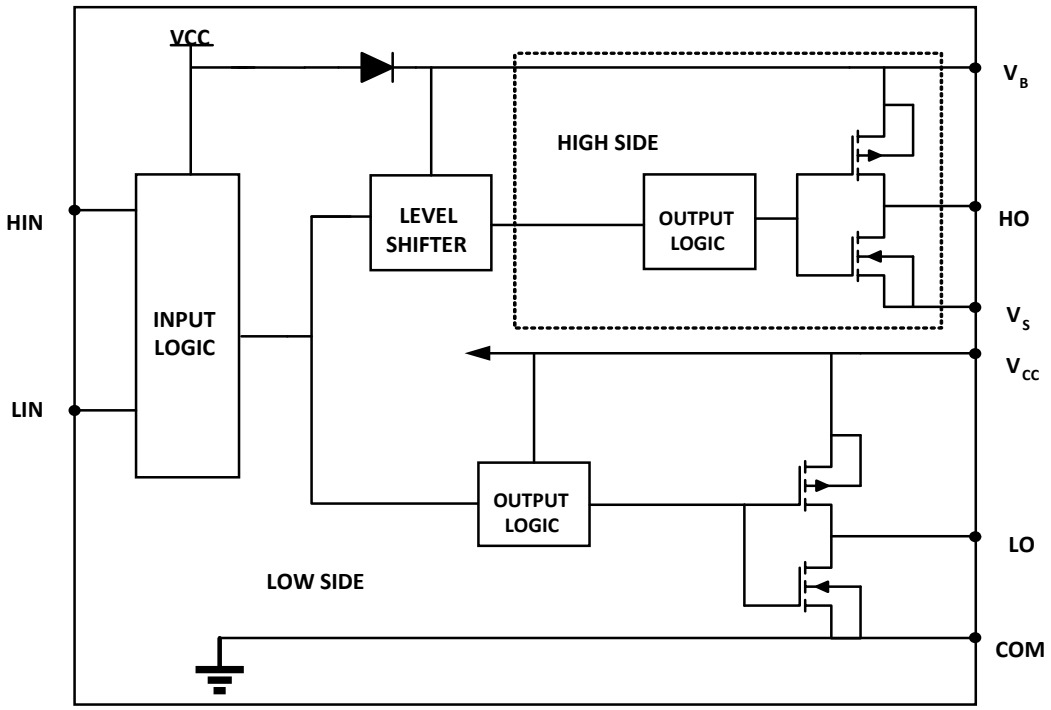


Fig.2 Function block diagram of ID2206D

Absolute Maximum Ratings

Exceeding these ratings may damage the device.

The absolute maximum ratings are stress ratings only at T_A=25°C, unless otherwise specified.

Symbol	Definition		MIN.	MAX.	Units
V_B	High side floating supply		-0.3	620	V
V_S	High side floating supply return		V_B – 20	V_B + 0.3	
V_{HO}	High side gate drive output		V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply		-0.3	20	
V_{LO}	Low side gate drive output		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & LIN		-0.3	V_{CC} + 0.3	
ESD	HBM Model		1.5		kV
	CDM Model		500		V
P_D	Package Power Dissipation @ TA ≤25°C	--	--	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	--	--	200	°C /W
T_J	Junction Temperature		--	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		--	300	

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S + 10	V_S + 18	V
V_S	High side floating supply return	-7	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	18	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Dynamic Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	TYP.	MAX.	Units
t_{ONH}	High side turn on propagation delay	130	230	ns
t_{OFFH}	High side turn off propagation delay	130	230	
t_{ONL}	Low side turn on propagation delay	130	230	
t_{OFFL}	Low side turn off propagation delay	130	230	
MT	Delay matching time (t_{ON}, t_{OFF})	--	60	
DT	Dead time	150	220	
MDT	Dead time matching	10	--	
t_R	Turn on rising time	90	170	
t_F	Turn off falling time	50	90	

Static Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
I_{LK}	High-side floating supply leakage current	--	--	50	µA
I_{QBS}	Quiescent V_{BS} supply current	--	80	160	
I_{QCC}	Quiescent V_{CC} supply current	--	170	270	
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	--	--	0.1	V
V_{OL}	Low level output voltage drop, V_O	--	--	0.1	
I_{O+}	Output high short circuit pulsed current	--	200	--	mA
I_{O-}	Output low short circuit pulsed current	--	360	--	
V_{CCU+}	VCC under voltage threshold voltage	8	8.9	9.8	
V_{CCU-}		7.4	8.2	9	
V_{BSU+}	VBS under voltage threshold voltage	8	8.9	9.8	
V_{BSU-}		7.4	8.2	9	
V_{IH}	High level input threshold voltage	2.5	--	--	V
V_{IL}	Low level input threshold voltage	--	--	0.8	
I_{IN+}	Logic “1” input bias current (HIN “1” & LIN “1”)	--	6	10	µA
I_{IN-}	Logic “0” input bias current (HIN “0” & LIN “0”)	--	--	1	
R_{BSD}	Bootstrap driver on-resistance	--	200	--	Ω

Note 2: The current ability is test under the condition that VCC=15V;

Function Timing Diagram

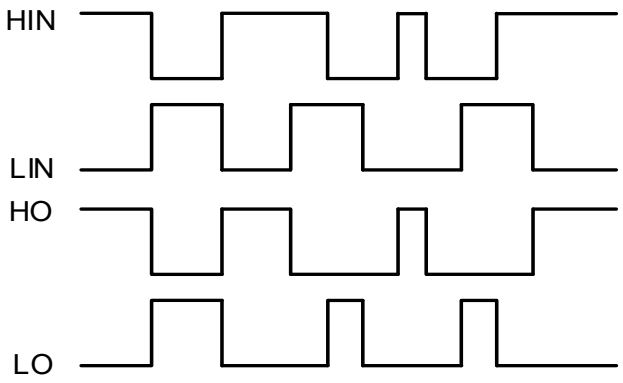


Fig.1 Input and output timing waveform

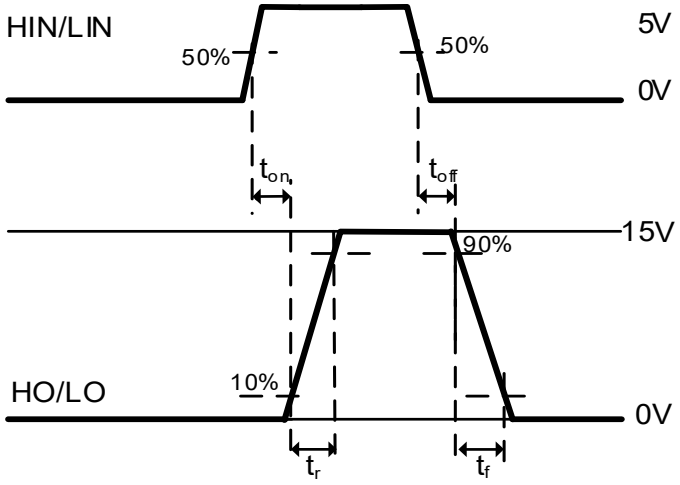


Fig.2 Propagation and Rise/Fall time definition

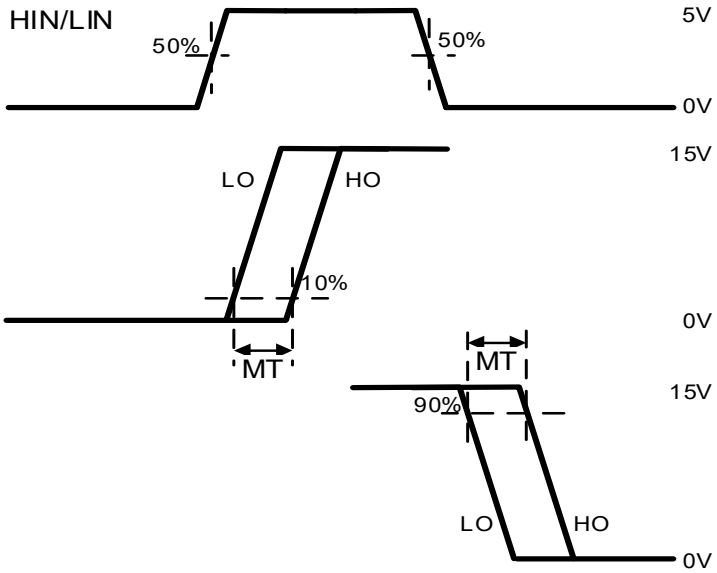


Fig.3 Delay matching definition

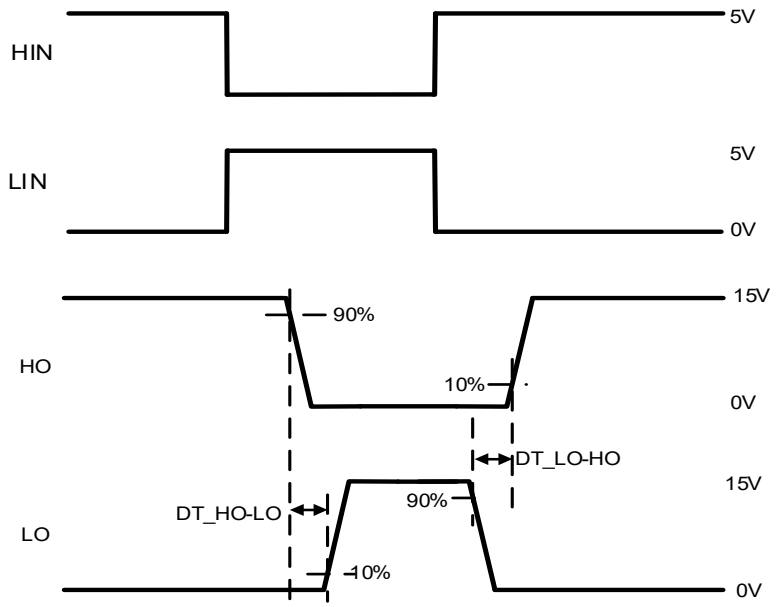


Fig.4 DT definition

Package Information

SOIC8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Package Outlines