High Side & Low Side Gate Drive IC

General description

The ID2304D is a high voltage, high speed power MOSFET and IGBT driver based on P_SUB P_EPI process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT in a half-bridge configuration which operates up to 600 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

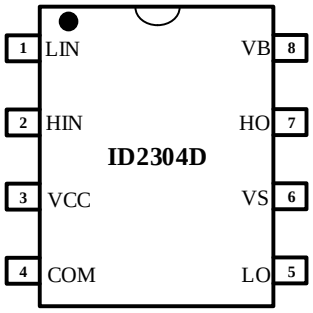
Application

- Small and medium-power motor driver
- Power MOSFET or IGBT driver
- Half-Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Driver Converters

Features

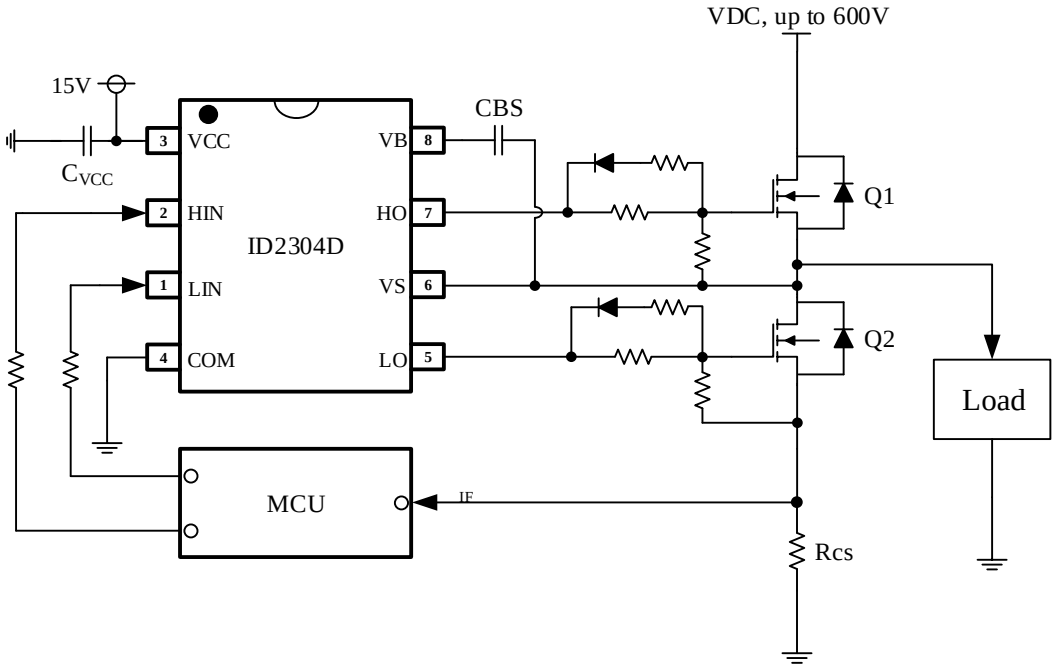
- Fully operational to +600 V
- 3.3 V and 5 V logic compatible
- dV/dt Immunity ±50 V/nsec
- Negative VS Swing to -7 V
- Gate drive supply range from 10 V to 18 V
- UVLO for high side & low side channels
- Output Source/Sink Current Capability 300 mA / 500 mA
- Matched propagation delay for both channels
- Internal dead time 120 ns typical
- Build-in bootstrap diode

Package/Order Information



Order code	Package
ID2304DSEC-R1	SOP8

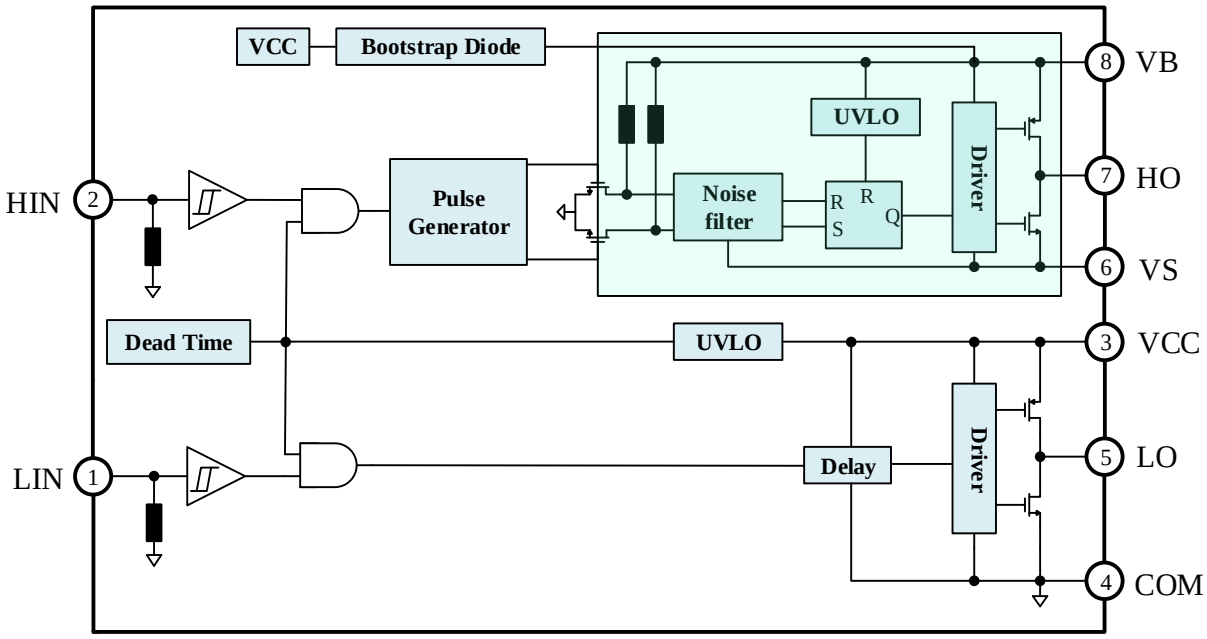
Typical Application Circuit



Pin Definitions

Pin Name	Pin Number	Pin Function Description
LIN	1	Logic input for low side gate driver output (LO)
HIN	2	Logic input for high side gate driver output (HO)
V_{CC}	3	Low side and main power supply
COM	4	Ground
LO	5	Low side gate drive output, out of phase with LIN
V_S	6	High side floating supply return or bootstrap return
HO	7	High side gate drive output, in phase with HIN
V_B	8	High side floating supply

Functional Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at T_A=25℃, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	620	V
V_S	High side floating supply return	V_B – 20	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	20	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & LIN	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	--	50	V/ns
ESD	HBM Model	2.5	--	kV
	CDM Model	200	--	V
P_D	Package Power Dissipation @ T_A ≤25°C (8 Lead SOP)	--	0.625	W
R_{thJA}	Thermal Resistance Junction to Ambient (8 Lead SOP)	--	200	℃ /W
T_J	Junction Temperature	--	150	℃
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	--	300	

Recommended Operating Conditions

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply	V_S +10	V_S +18	V
V_S	High side floating supply return	-	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	18	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	℃

Dynamic Electrical Characteristics

(V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.)

Symbol	Definition	TYP.	MAX.	Units
t_{ONH}	High side turn on propagation delay	300	450	ns
t_{OFFH}	High side turn off propagation delay	300	450	
t_{ONL}	Low side turn on propagation delay	300	450	
t_{OFFL}	Low side turn off propagation delay	300	450	
DT	Dead time	120	150	
MT	Delay matching time (t_{ON}, t_{OFF})	10	60	
t_R	Turn on rising time	50	95	
t_F	Turn off falling time	35	60	

Static Electrical Characteristics

(V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.)

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{UVCCR}	V_{CC} supply under-voltage reset threshold	8.3	8.9	9.5	V
V_{UVCCT}	V_{CC} supply under-voltage trigger threshold	7.6	8.2	8.8	
V_{UVBSR}	V_{BS} supply under-voltage reset threshold	8.3	8.9	9.5	
V_{UVBST}	V_{BS} supply under-voltage trigger threshold	7.6	8.2	8.8	
I_{LK}	High-side floating supply leakage current	--	--	50	μA
I_{QBS}	Quiescent V_{BS} supply current	--	80	160	
I_{QCC}	Quiescent V_{CC} supply current	--	170	270	
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	--	--	0.3	V
V_{OL}	Low level output voltage drop, V_O	--	--	0.3	
I_{O+}	Output high short circuit pulsed current	--	300	--	mA
I_{O-}	Output low short circuit pulsed current	--	500	--	
V_{IH}	Logic “1”(HIN& LIN) input voltage	2.5	--	--	V
V_{IL}	Logic “0” (HIN & LIN) input voltage	--	--	0.8	
I_{IN+}	Logic “1” input bias current	--	6	10	μA
I_{IN-}	Logic “0” input bias current	--	--	1	
R_{BSD}	Internal bootstrap equivalent resistor value	--	200	--	Ω

Function Timing Diagram

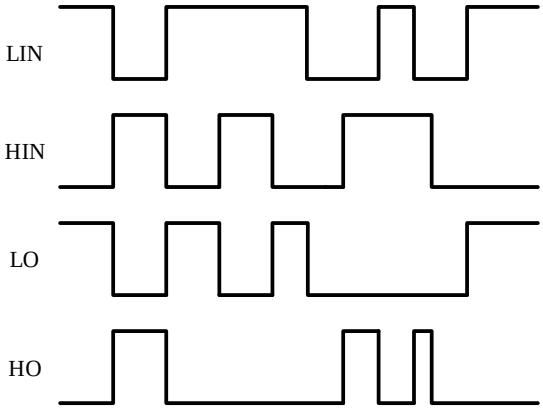


Fig.1 Input and output timing waveform

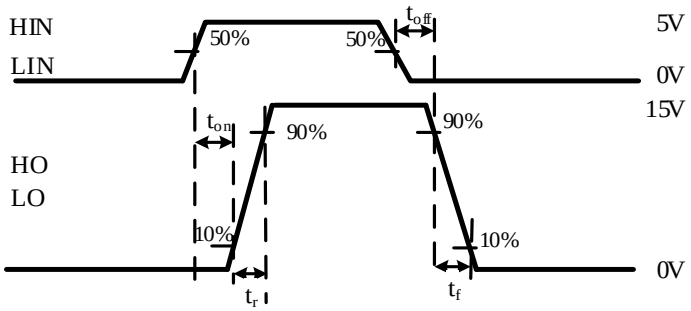


Fig.2 Propagation and Rise/Fall time definition

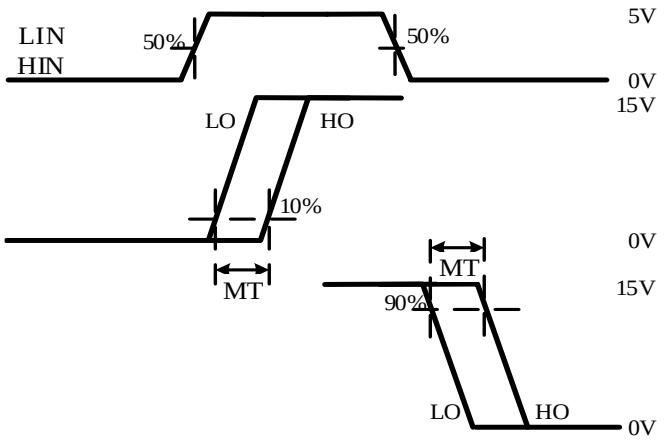


Fig.3 Delay matching definition

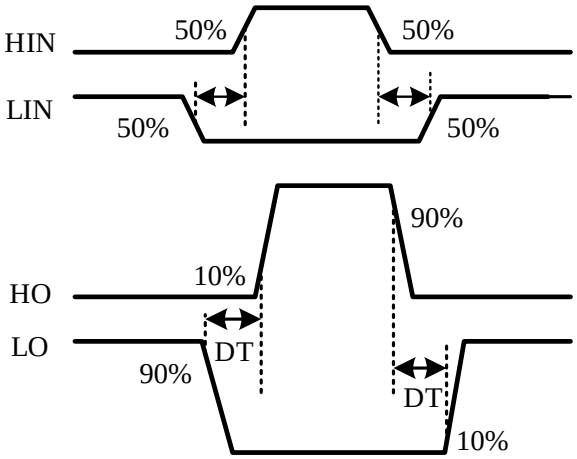
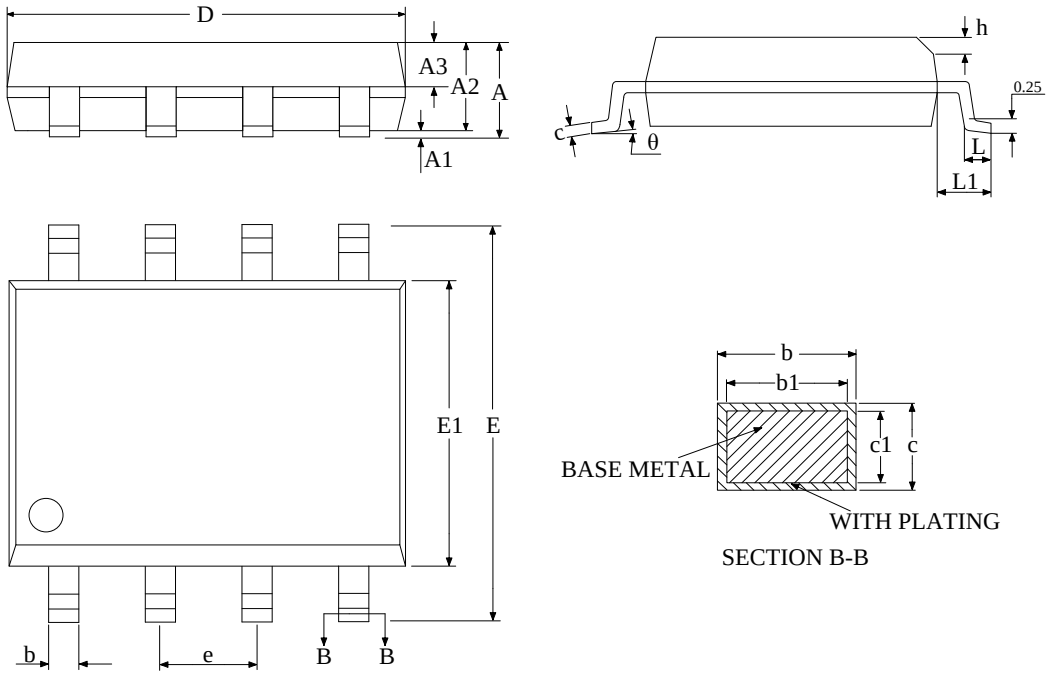


Fig.4 Dead-time definition

Package Information

Package Information SOP8



Symbol \ Size	Min. (mm)	Typ. (mm)	Max. (mm)	Symbol \ Size	Min. (mm)	Typ. (mm)	Max. (mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Top mark	Package
iDR. ID2304D YWWXXXXX	SOP8

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

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