ID5S609/ID5S609F1

High Side & Low Side Gate Drive IC

General Description

The ID5S609/ID5S609F1 is a high voltage, high speed power MOSFET and IGBT driver based on P_sub P_epi process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT in a half-bridge configuration which operates up to 600V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

Features

- Operation to +600 V
- Typically 400mA/800mA Source/Sink current
- 3.3 V input logic compatible
- dV/dt Immunity ±50 V/nsec
- Gate drive supply range from 10 V to 20 V
- UVLO for both channels
- Cross-conduction prevention logic with 100ns internal fixed Dead time
- Matched propagation delay for all channels

Applications

- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Lighting ballast
- Half−Bridge Power Converters
- Full-Bridge Power Converters

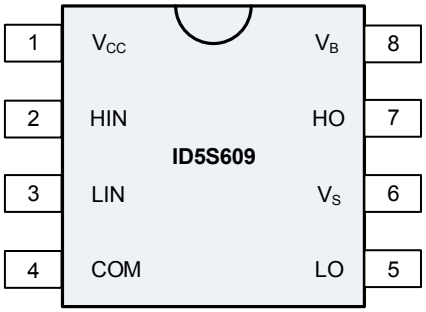
Package Options

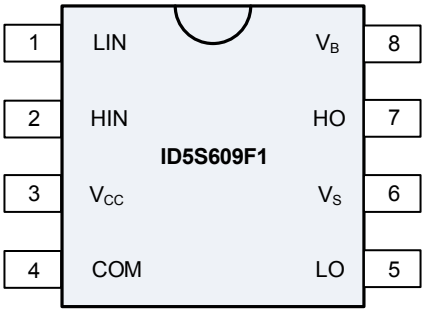
SOIC-8

Order Information

Part Number	Order Code	Package	Type
ID5S609	ID5S609SEC-R1	8-lead, SOIC	Reel
ID5S609F1	ID5S609F1SEC-R1	8-lead, SOIC	Reel

Pin Configuration

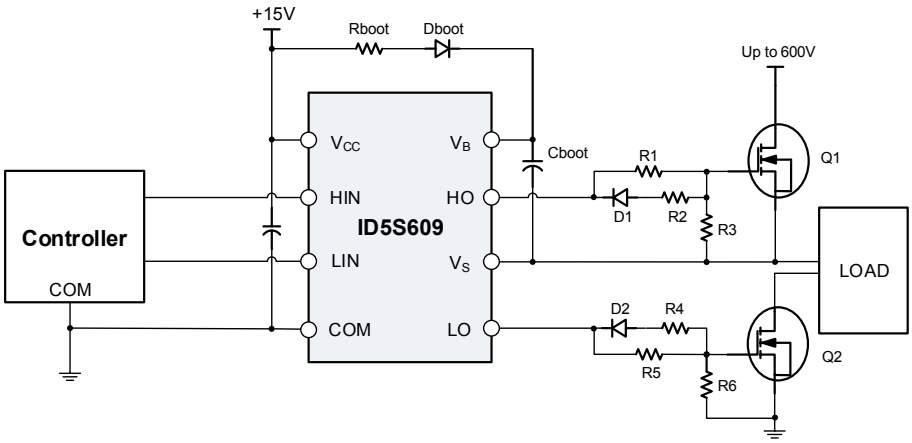


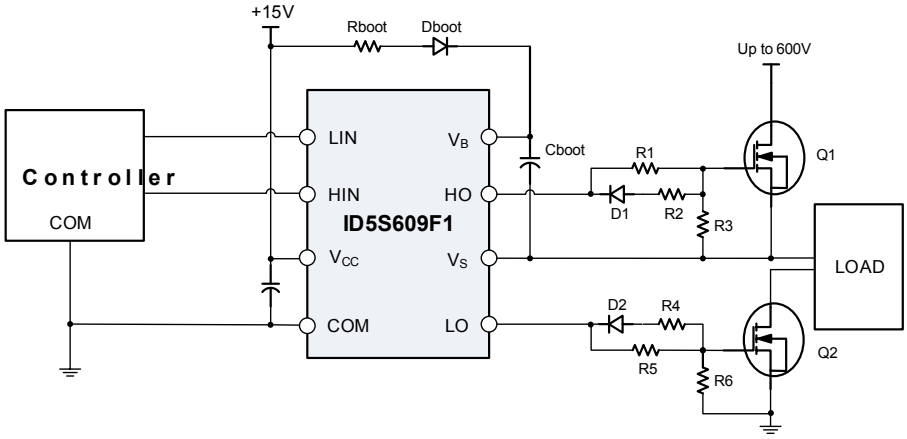


Pin Definitions

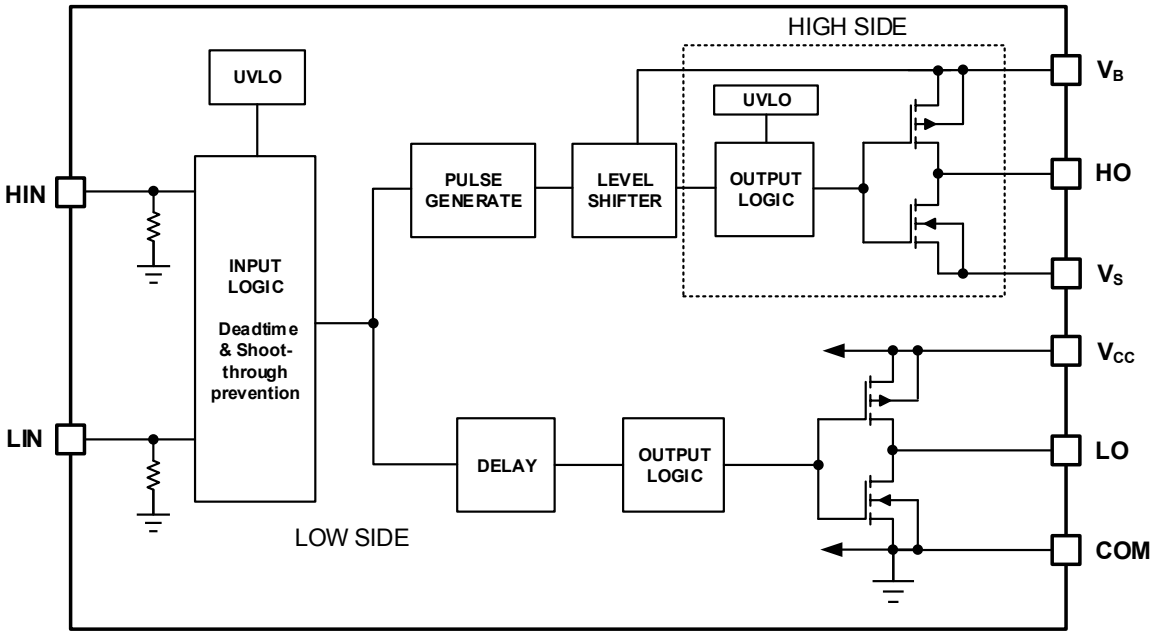
PIN NO.		PIN NAME	PIN FUNCTION
ID5S609	ID5S609F1		
1	3	VCC	Low side and main power supply
2	2	HIN	Logic input for high side gate driver output (HO)
3	1	LIN	Logic input for low side gate driver output (LO)
4	4	COM	Ground
5	5	LO	Low side gate drive output, in phase with LIN
6	6	VS	High side floating supply return or bootstrap return
7	7	HO	High side gate drive output, in phase with HIN
8	8	VB	High side floating supply

Typical Application Circuit





Functional Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.

The absolute maximum ratings are stress ratings only at T_A=25°C, unless otherwise specified.

Symbol	Definition		MIN.	MAX.	Units
V_B	High side floating supply		-0.3	620	V
V_S	High side floating supply return		V_B - 20	V_B + 0.3	
V_{HO}	High side gate drive output		V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply		-0.3	20	
V_{LO}	Low side gate drive output		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN and LIN		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		—	50	V/ns
ESD	HBM Model		2.5	—	kV
	Machine Model		200	—	V
P_D	Package Power Dissipation @ TA ≤25°C	8 Lead SOIC	—	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	8 Lead SOIC	—	200	°C /W
T_J	Junction Temperature		—	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	-	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Dynamic Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
t_{onH}	High side turn-on propagation delay	160	220	t_{onH}	ns
t_{offH}	High side turn-off propagation delay	150	220	t_{offH}	
t_{onL}	Low side turn-on propagation delay	160	220	t_{onL}	
t_{offL}	Low side turn-off propagation delay	150	220	t_{offL}	
MT	Delay matching	20	50	MT	
DT	Dead time	180	250	DT	
t_r	Turn-on rise time	60	120	t_r	
t_f	Turn-off fall time	50	100	t_f	

Static Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic “1”(HIN & LIN) input voltage	2.3	-	-	V
V_{IL}	Logic “0” (HIN & LIN) input voltage	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	-	-	0.3	
V_{OL}	Low level output voltage, V_O	-	-	0.3	
I_{QCC}	Quiescent V_{CC} supply current	-	150	300	uA
I_{QBS}	Quiescent V_B supply current	-	50	100	
I_{LK}	Leakage current from V_S(600V) to GND		-	10	
I_{IN+}	Logic “1” input bias current	-	6	10	
I_{IN-}	Logic “0” input bias current	-	-	1	
V_{BSU+}	V_{BS} supply UVLO threshold	-	8.7	-	V
V_{BSU-}		-	8	-	
V_{CCU+}	V_{CC} supply UVLO threshold	-	8.7	-	
V_{CCU-}		-	8	-	
I_{O+}	Output high short circuit pulsed current		400		mA
I_{O-}	Output low short circuit pulsed current		800		

Function Timing Diagram

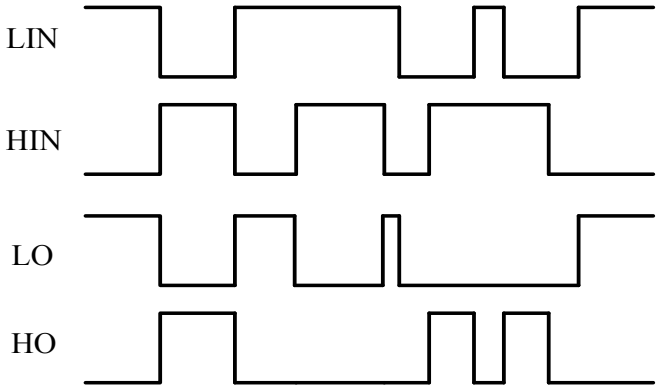


Fig.1 Input/Output timing waveform

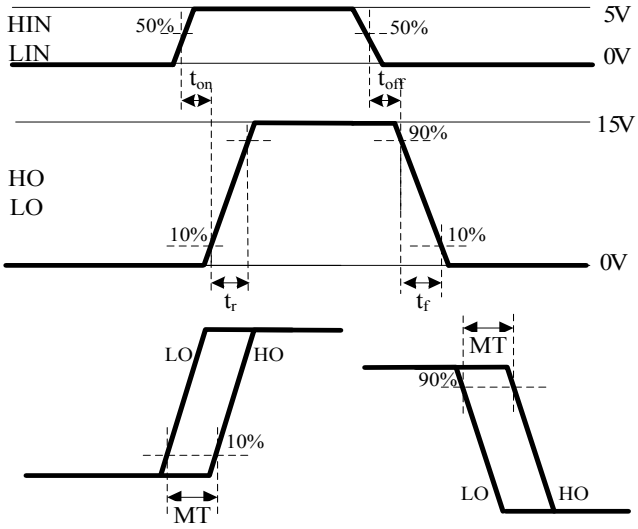


Fig.2 (a) Switching time waveform definitions

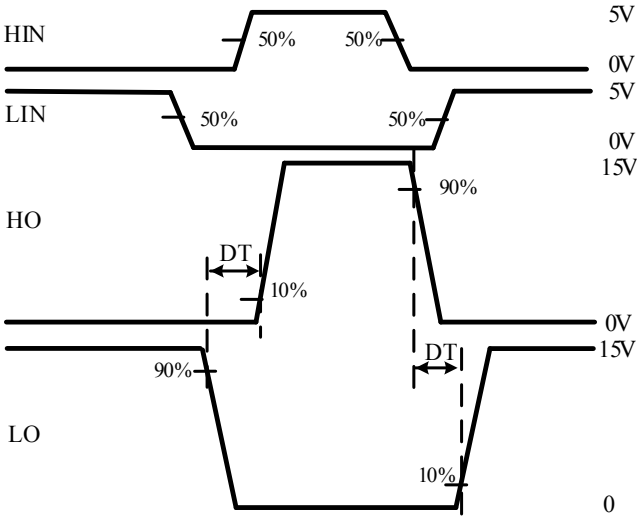


Fig.2 (b) Dead-time waveform definitions

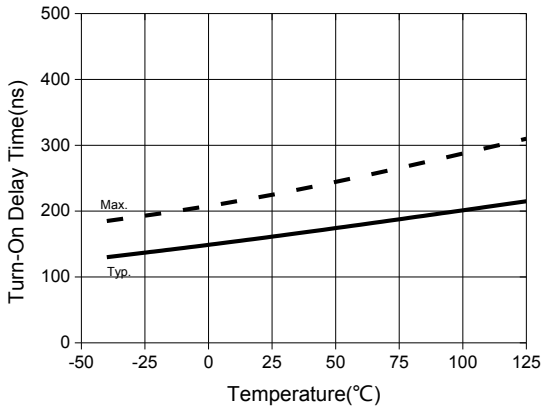


Fig.3 Turn-On Delay vs. Temperature

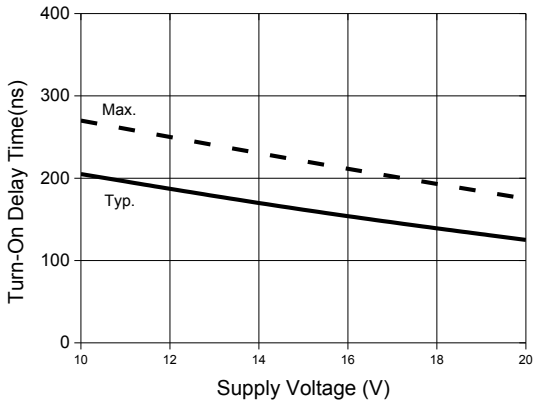


Fig.4 Turn-On Delay vs. Voltage

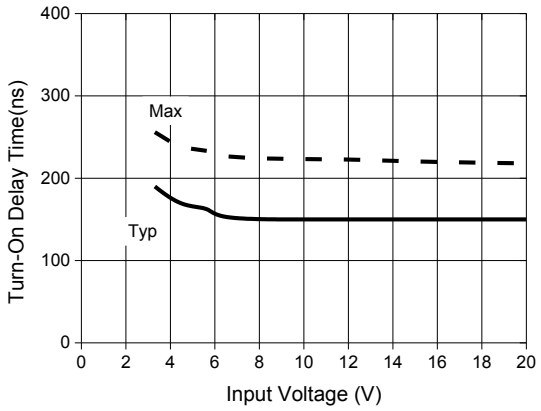


Fig.5 Turn-On Delay Time vs. Input Voltage

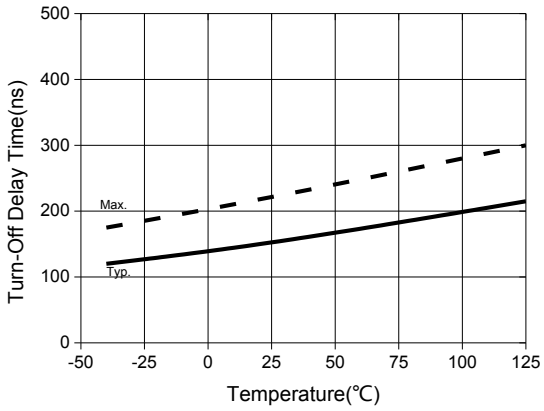


Fig.6 Turn-Off Delay Time vs. Temperature

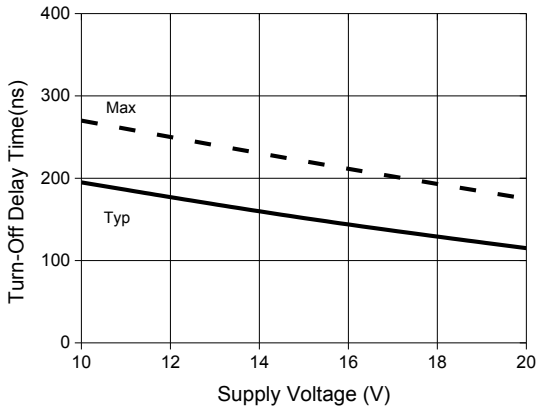


Fig.7 Turn-Off Delay Time vs. Supply Voltage

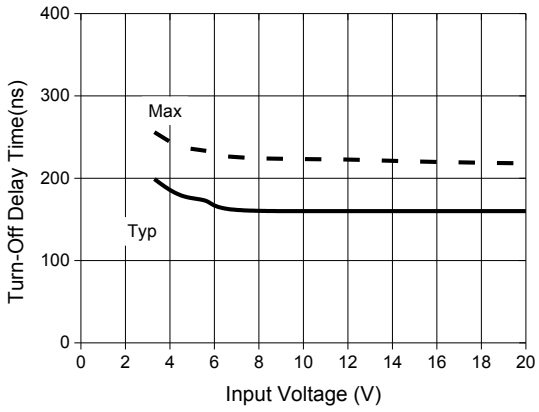


Fig.8 Turn-Off Delay Time vs. Input Voltage

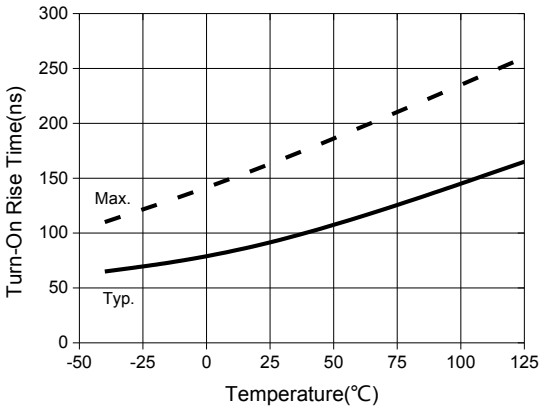


Fig.9 Turn-On Rise Time vs. Temperature

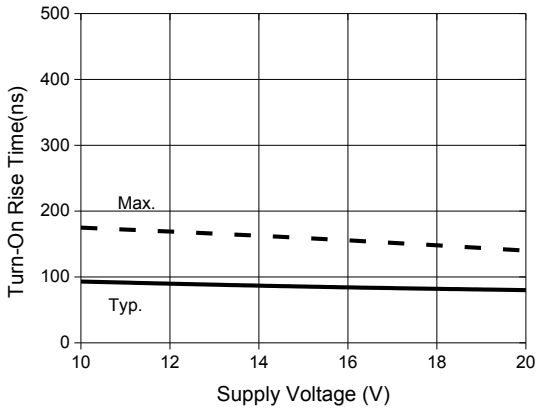


Fig.10 Turn-On Rise Time vs. Voltage

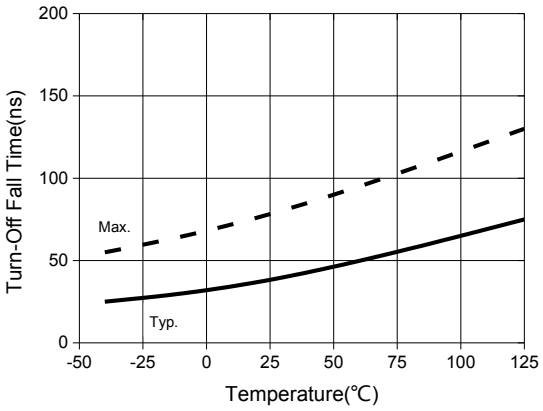


Fig.11 Turn-Off Fall Time vs. Temperature

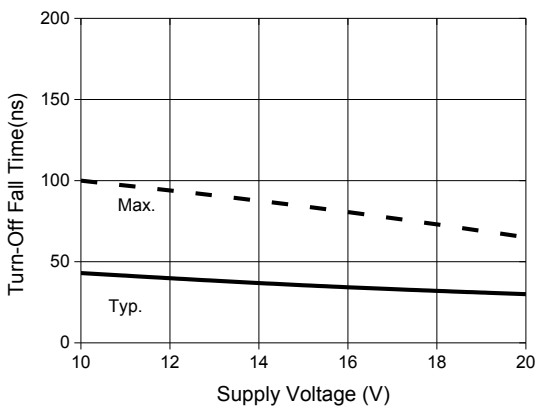


Fig.12 Turn-Off Fall Time vs. Voltage

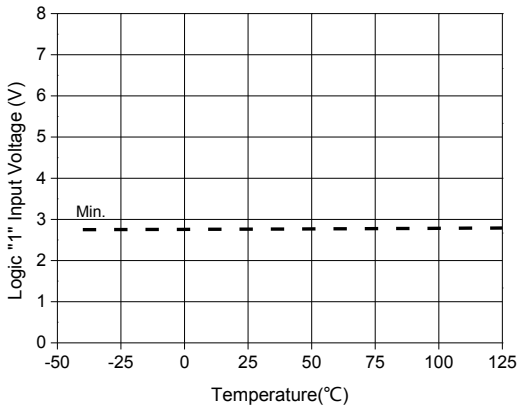


Fig.13 Logic "1" Input Voltage vs. Temperature

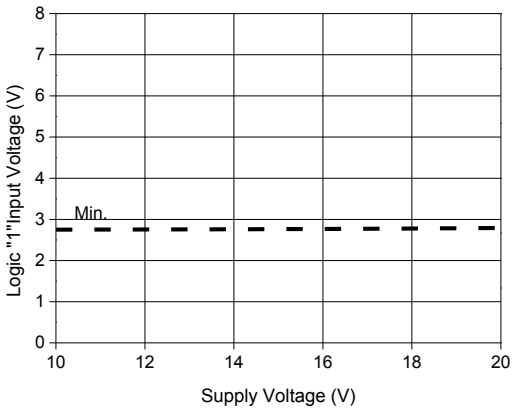


Fig.14 Logic "1" Input Voltage vs. Voltage

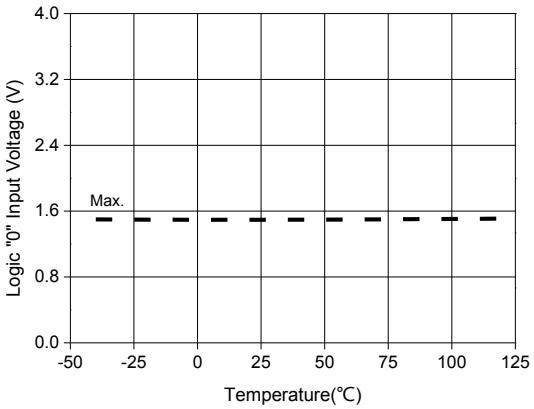


Fig.15 Logic "0" Input Voltage vs. Temperature

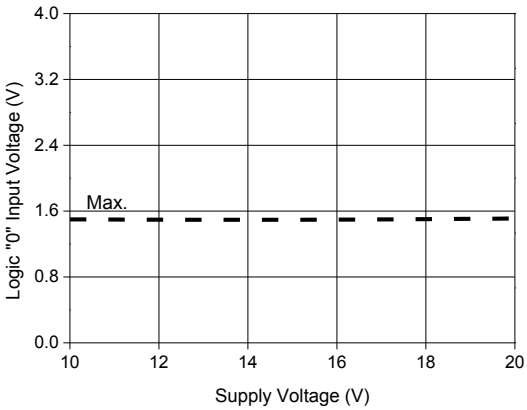


Fig.16 Logic "0" Input Voltage vs. Voltage

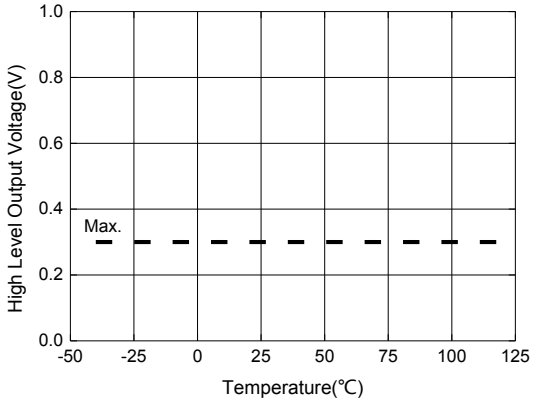


Fig.17 High Level Output vs. Temperature

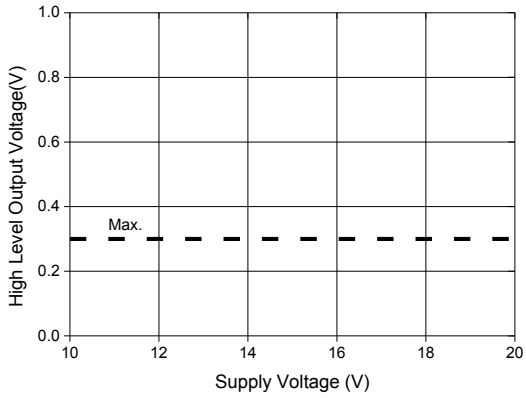


Fig.18 High Level Output vs. Voltage

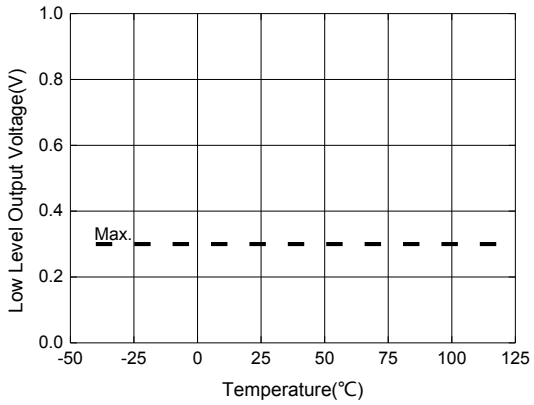


Fig.19 Low Level Output vs. Temperature

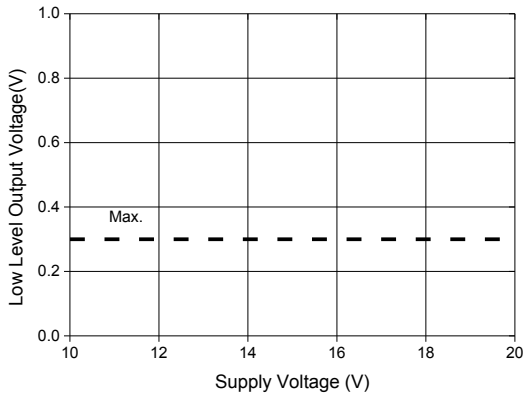


Fig.20 Low Level Output vs. Voltage

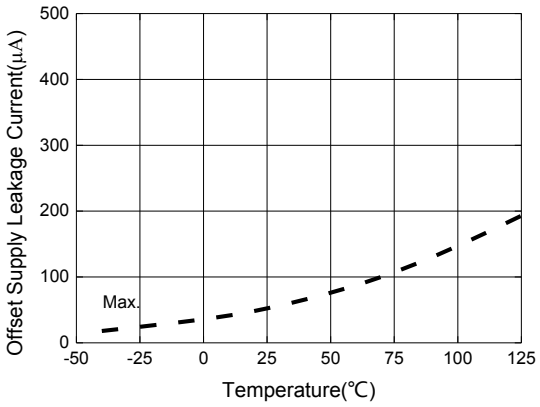


Fig.21 Offset Supply Current vs. Temperature

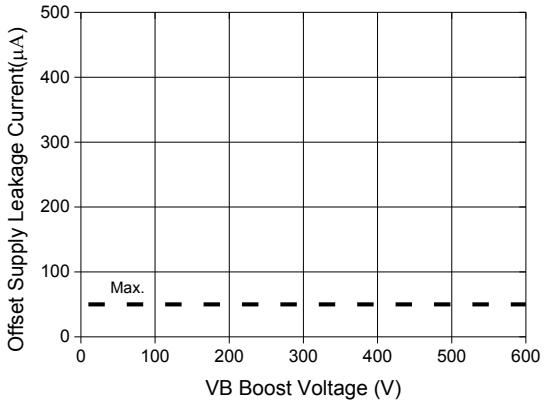


Fig.22 Offset Supply Current vs. Voltage

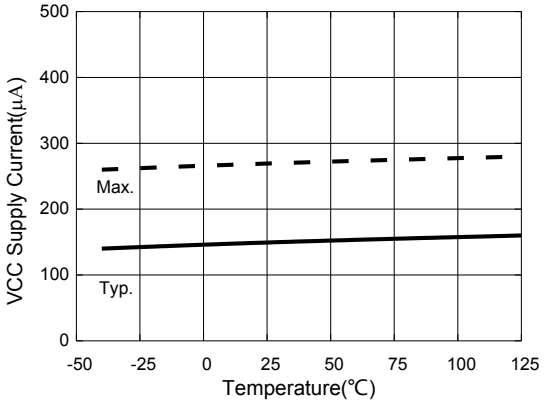


Fig.23 VCC Supply Current vs. Temperature

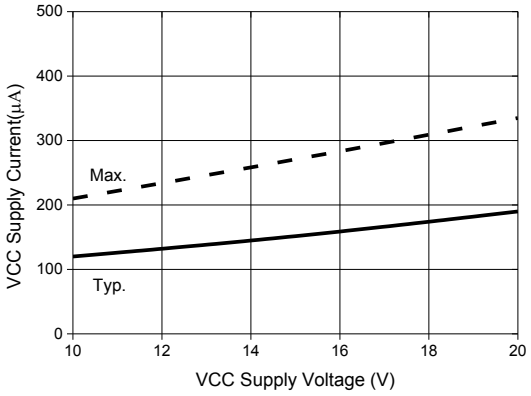


Fig.24 VCC Supply Current vs. Voltage

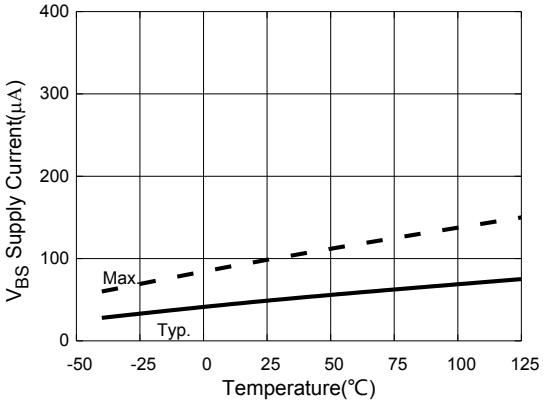


Fig.25 VBS Supply Current vs. Temperature

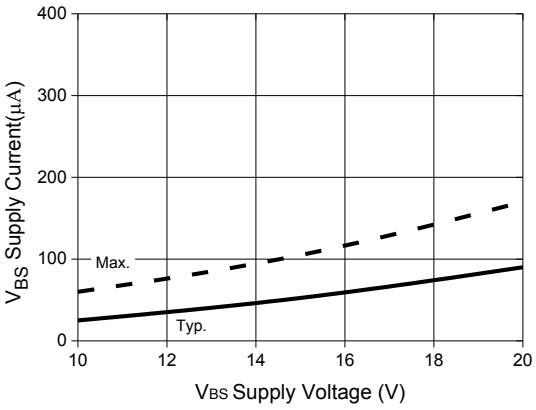


Fig.26 VBS Supply Current vs. Voltage

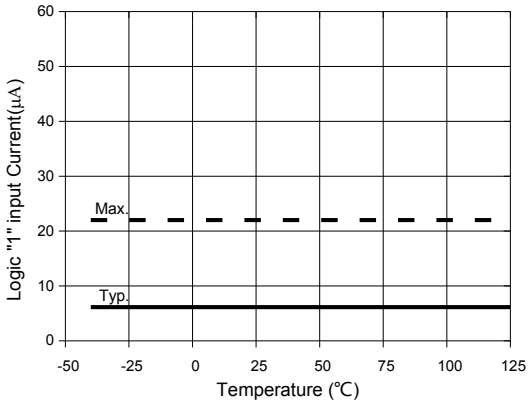


Fig.27 Logic "1" Input Current vs. Temperature

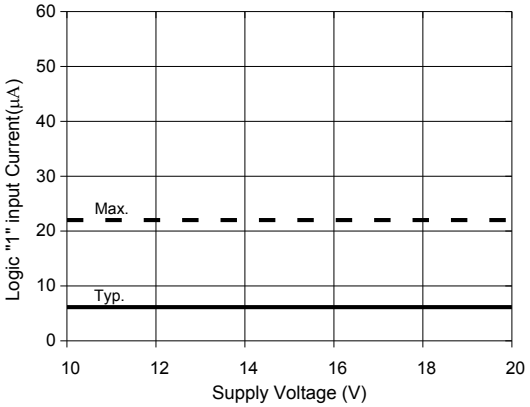


Fig.28 Logic "1" Input Current vs. Voltage

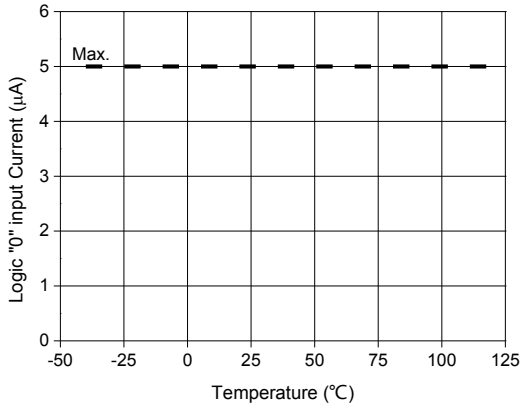


Fig.29 Logic "0" Input Current vs. Temperature

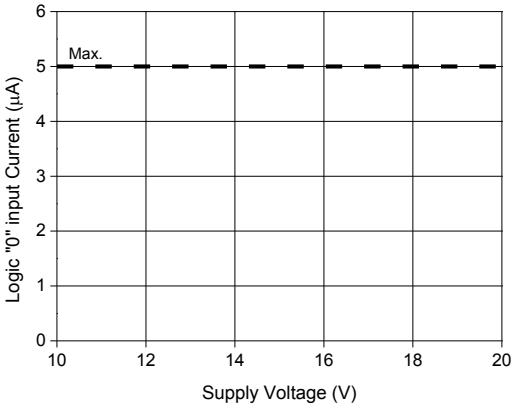


Fig.30 Logic "0" Input Current vs. Voltage

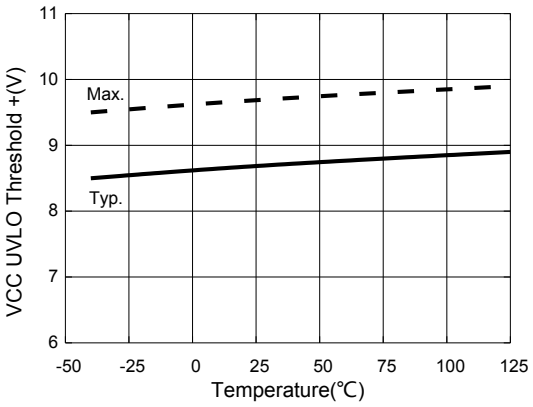


Fig.31 VCC Undervoltage Threshold (+)
Vs. Temperature

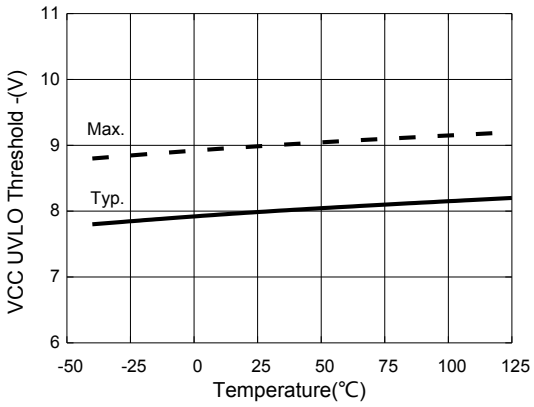


Fig.32 VCC Undervoltage Threshold (-)
vs. Temperature

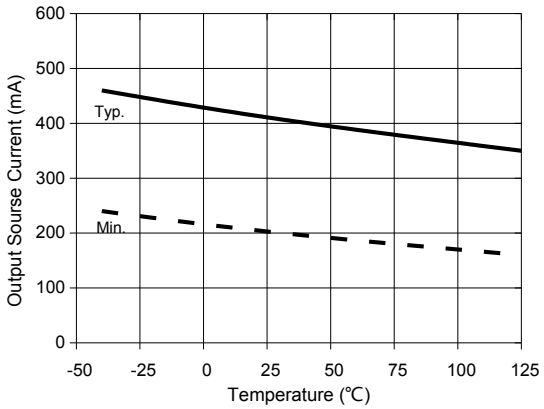


Fig.33 Output Source Current vs. Temperature

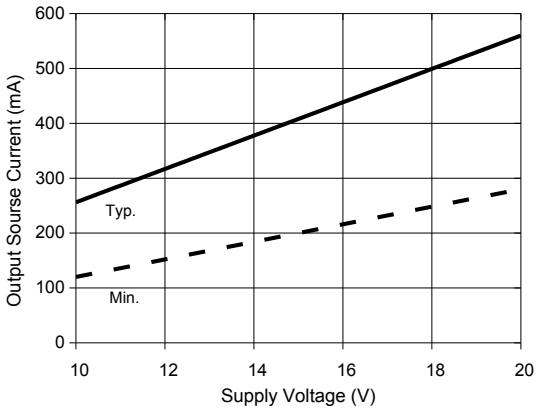


Fig.34 Output Source Current vs. Voltage

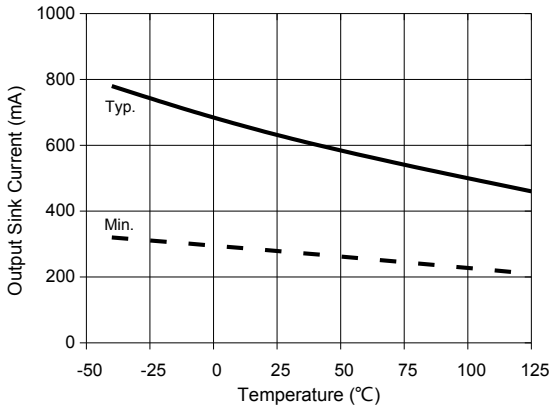


Fig.35 Output Sink Current vs. Temperature

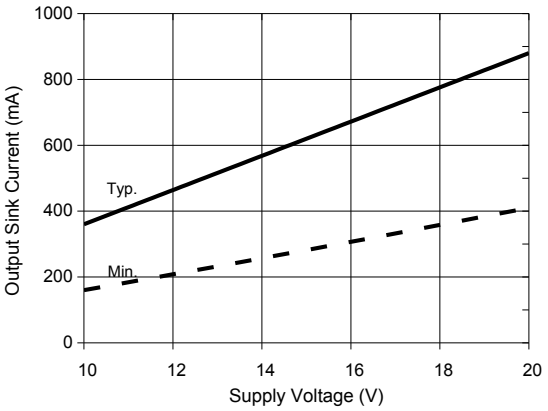


Fig.36 Output Sink Current vs. Voltage

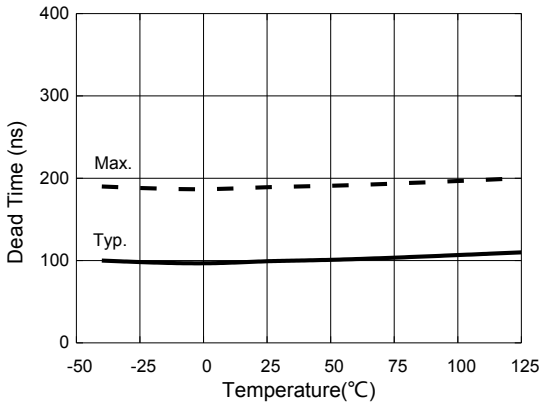


Fig.37 Dead Time vs. Temperature

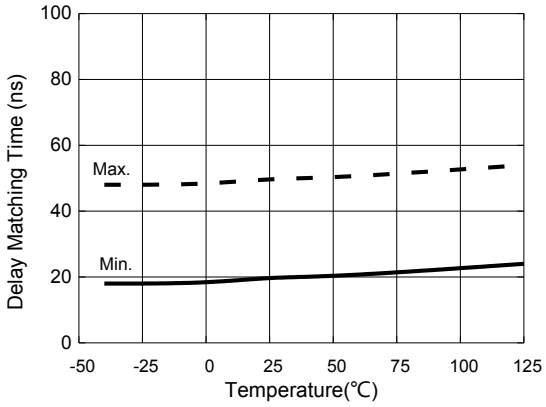


Fig.38 High Side & Low Side Delay Matching Time vs. Temperature

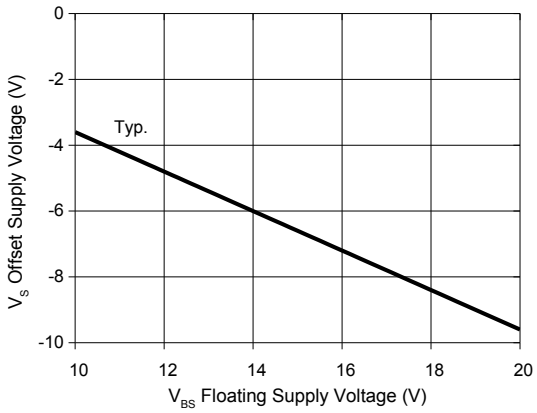


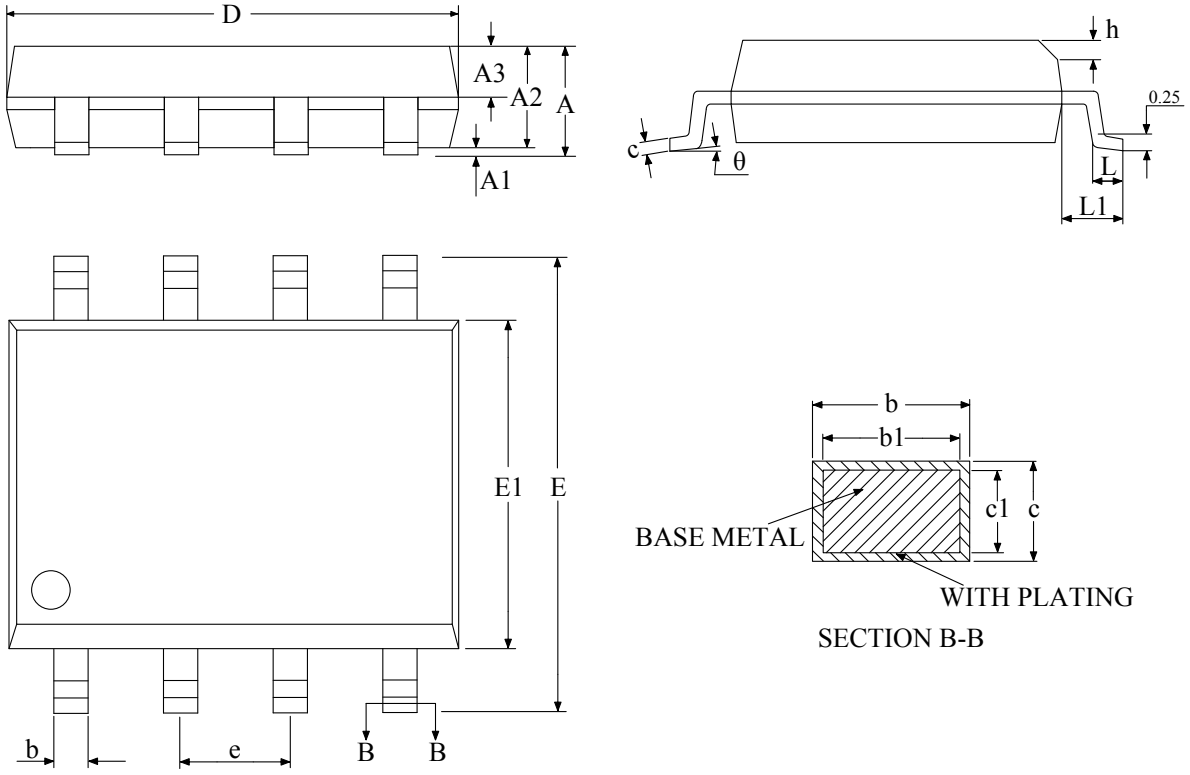
Fig.39 Maximum VS Negative Offset vs. Supply Voltage

Package Information

SOIC8 Package Dimensions

Size / Symbol	MIN(mm)	MAX(mm)	Size / Symbol	MIN(mm)	MAX(mm)
A	1.499	1.750	e	1.27TYP	
A1	0.102	0.249	h	-	-
A2	1.397	-	h1	0.254	0.457
b	0.406TYP		L	0.406	0.889
c	0.2TYP		Θ1	12°TYP	
D	4.852	4.952	Θ2	12°TYP	
E	5.842	6.198	Θ3	0	8
E1	3.877	3.997	Θ4	45	

SOIC8 Package Outlines



Mark	Package
ID5S609/ID5S609F1 ABYWX	SOIC8

Note：AB：Product code，Y：Year code； W：Week code； X：Package code