ID7T6036

3-Phase High Voltage Gate Drive IC

General Description

The ID7T6036 is a three-phase gate drive IC which can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600V. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an over-current or under-voltage shutdown has occurred. Over-current fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

Features

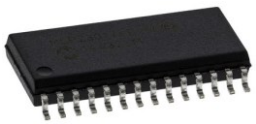
- ❑ Operation to +600 V
- ❑ Typically 200mA/350mA Source/Sink current
- ❑ 3.3 V/5V/15V input logic compatible
- ❑ dV/dt Immunity ±50 V/nsec
- ❑ Typically - 9V negative Vs bias capability
- ❑ Gate drive supply range from 10 V to 20 V
- ❑ UVLO for all channels
- ❑ Cross-conduction prevention logic
- ❑ Over-current shutdown turns off all six drivers
- ❑ Externally adjustable Fault-clear timing
- ❑ Built-in advanced input filter
- ❑ Matched propagation delay for all channels

Applications

- ❑ Sewing Machine/Power Toll
- ❑ Air Conditioners/ Washing Machines /Refrigerator
- ❑ General Purpose Inverters

Package Options

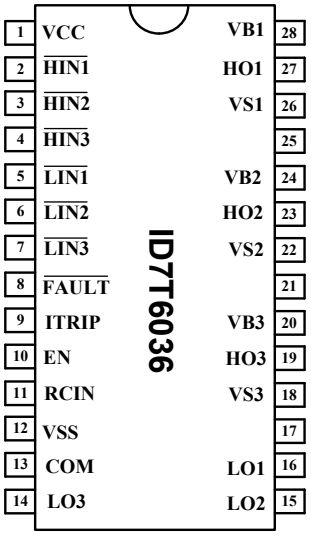
28-SOIC



Order Information

Part Number	Order Code	Package	Type
ID7T6036	ID7T6036SAC-R1	SOIC28	Reel

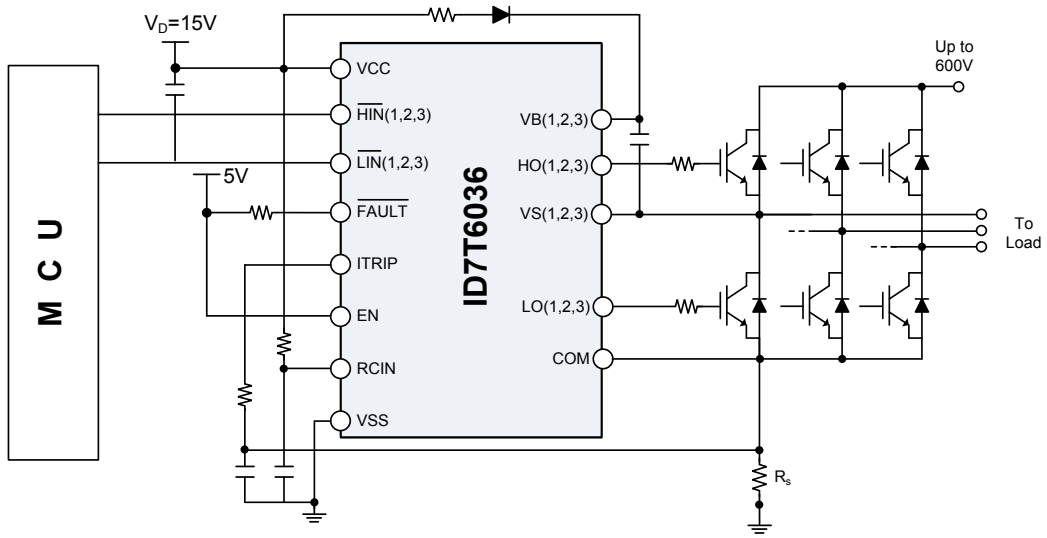
Pin Configuration



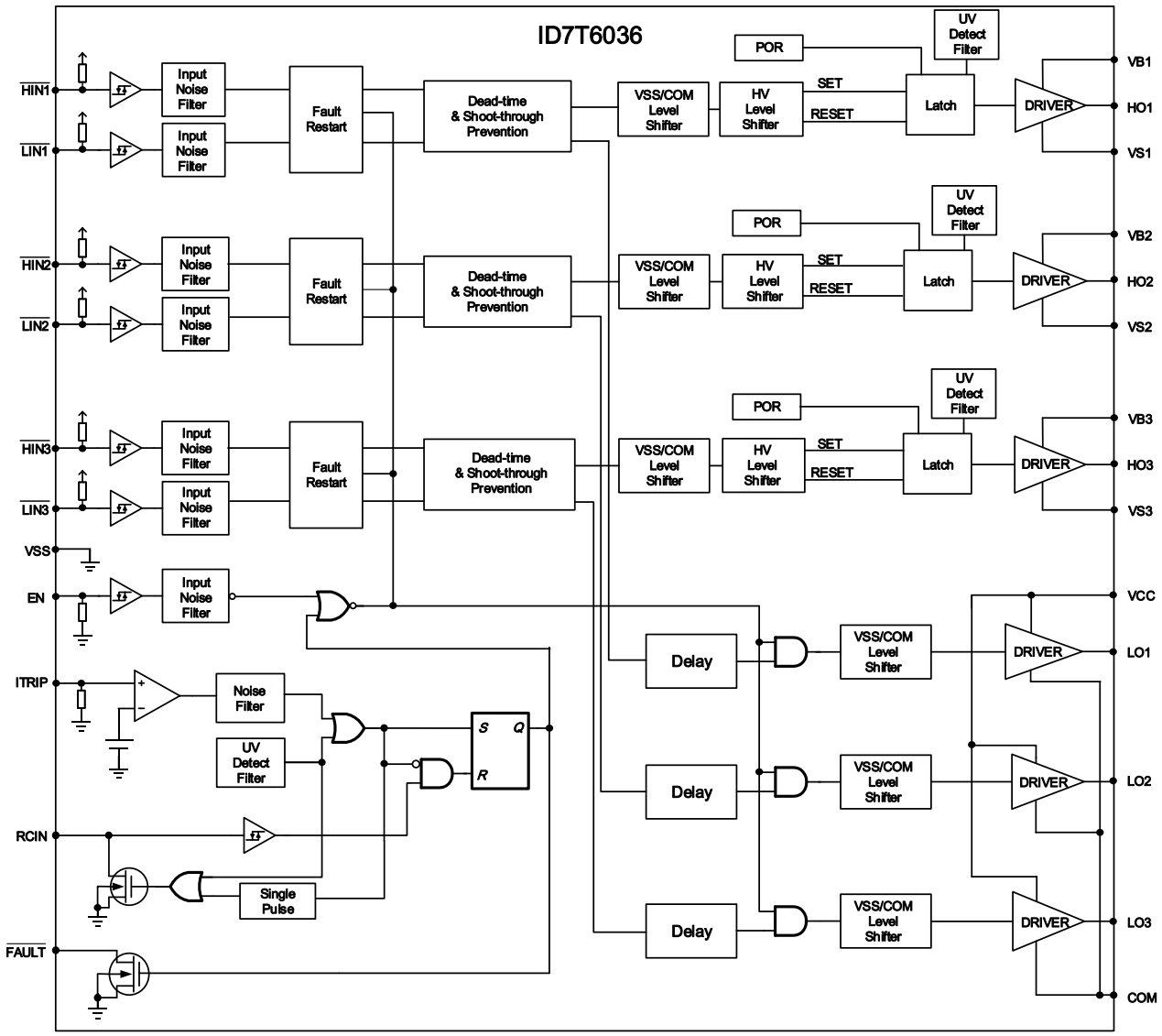
Pin Definitions

PIN NO.	PIN NAME	PIN FUNCTION
1	VCC	Low side and logic fixed supply voltage
2	$\overline{\text{HIN1}}$	Signal Input for 1 Phase High-side
3	$\overline{\text{HIN2}}$	Signal Input for 2 Phase High-side
4	$\overline{\text{HIN3}}$	Signal Input for 3 Phase High-side
5	$\overline{\text{LIN1}}$	Signal Input for 1 Phase Low-side
6	$\overline{\text{LIN2}}$	Signal Input for 2 Phase Low-side
7	$\overline{\text{LIN3}}$	Signal Input for 3 Phase Low-side
8	$\overline{\text{FAULT}}$	Indicates over-current (ITRIP)or low-side under-voltage lockout
9	ITRIP	Analog input for overcurrent shutdown.
10	EN	Logic input to enable I/O functionality
11	RCIN	External RC network input used to define FAULT CLEAR delay
12	VSS	Logic ground
13	COM	Low side gate drivers return
14	LO3	Low side gate driver outputs for 3 Phase
15	LO2	Low side gate driver outputs for 2 Phase
16	LO1	Low side gate driver outputs for 1 Phase
18	VS3	High voltage floating supply return for 3 Phase
19	HO3	High side gate driver outputs for 3 Phase
20	VB3	High side floating supply for 3 Phase
22	VS2	High voltage floating supply return for 2 Phase
23	HO2	High side gate driver outputs for 2 Phase
24	VB2	High side floating supply for 2 Phase
26	VS1	High voltage floating supply return for 1 Phase
27	HO1	High side gate driver outputs for 1 Phase
28	VB1	High side floating supply for 1 Phase

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at T_A=25°C, unless otherwise specified.

Symbol	Definition		MIN.	MAX.	Units
VB(1,2,3)	High side floating supply		-0.3	620	V
VS(1,2,3)	High side floating supply return		V_B - 20	V_B + 0.3	
VHO(1,2,3)	High side gate drive output		V_S -0.3	V_B + 0.3	
VCC	Low side and main power supply		-0.3	20	
VLO(1,2,3)	Low side gate drive output		COM -0.3	V_{CC} + 0.3	
VIN	Logic input of $\overline{HIN}$ & $\overline{LIN}$		V_{SS} -0.3	V_{CC} + 0.3	
VSS	Logic ground		V_{CC}-20	V_{CC}+0.3	
VRCIN	RCIN input voltage		V_{SS}	V_{CC}	
VFLT	$\overline{FAULT}$ output voltage		V_{SS}-0.3	V_{CC}+0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		—	50	V/ns
ESD	HBM Model		2.5	—	kV
	Machine Model		200	—	V
P_D	Package Power Dissipation @ TA ≤25°C	28 Lead SOIC	—	1.6	W
Rth_{JA}	Thermal Resistance Junction to Ambient	28 Lead SOIC	—	78	°C /W
T_J	Junction Temperature		—	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
VB(1,2,3)	High side floating supply	VS +10	VS +20	V
VS(1,2,3)	High side floating supply return	COM -9	600	
VHO(1,2,3)	High side gate drive output voltage	VS1,2,3	VB,1,2,3	
VCC	Low side supply	10	20	
VLO(1,2,3)	Low side gate drive output voltage	0	VCC	
VIN	Logic input voltage($\overline{HIN}$ & $\overline{LIN}$)	0	VCC	
VSS	Logic ground	-5	5	
VRCIN	RCIN input voltage	VSS	VCC	
VFLT	$\overline{FAULT}$ output voltage	VSS	VCC	
T_A	Ambient temperature	-40	125	°C

Dynamic Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
t_{ON}	Turn on propagation delay	400	530	750	ns
t_{OFF}	Turn off propagation delay	400	530	750	
t_R	Turn on rising time	-	125	190	
t_F	Turn off falling time	-	50	75	
$t_{IN,FLT}$	Input filter time ($\overline{HIN}$,$\overline{LIN}$)	200	350	510	
t_{EN}	Enable low to output shutdown propagation delay	350	460	650	
$t_{EN,FLT}$	Enable input filter time	100	200	-	
t_{UVCC}	UVCC filter time	-	7	-	µs
t_{UVBS}	UVBS filter time	-	7	-	
$t_{UVCC,FO}$	UVCC to FAULT shutdown propagation delay	-	7	-	
$t_{UVCC,LO}$	UVCC to LO shutdown propagation delay	-	7	-	
$t_{UVBS,HO}$	UVBS to HO shutdown propagation delay	-	7	-	
t_{FOd}	$\overline{FAULT}$ output duration time (RCIN: C = 1nF, R = 2 MΩ)	1.3	1.65	2	ms
t_{ITRIP}	ITRIP to output shutdown propagation delay	420	620	970	ns
$t_{IT,FLT}$	ITRIP filter time	-	400	-	
t_{FO}	ITRIP to $\overline{FAULT}$ propagation delay	400	600	950	
DT	Deadtime	190	275	420	
MDT	DT Matching	-	-	60	
MT	Delay matching time (t_{ON}, t_{OFF})	-	-	50	
PM	Pulse width distortion[1]	-	-	75	

Notes:

1. PM is defined as PW_{IN}-PW_{OUT}

Static Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{UVCC+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V
V_{UVCC-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9.0	
V_{UVCCHY}	V_{CC} supply undervoltage hysteresis	0.3	0.7	-	
I_{LK}	High-side floating supply leakage current	-	-	50	μA
I_{QBS}	Quiescent V_{BS} supply current	-	70	120	
I_{QCC}	Quiescent V_{CC} supply current	-	1	2	mA
I_{PBS}	Operating V_{BS} supply current	-	400	600	μA
I_{PCC}	Operating V_{CC} supply current (per 1phase)	-	1.3	1.8	mA
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	-	0.9	1.4	V
V_{OL}	Low level output voltage drop, V_O	-	0.4	0.6	
I_{O+}	Output high short circuit pulsed current	120	200	-	mA
I_{O-}	Output low short circuit pulsed current	250	350	-	
V_{IH}	High level input threshold voltage	2.5	-	-	V
V_{IL}	Low level input threshold voltage	-	-	0.8	
V_{CLAMP}	Input clamp voltage ($\overline{HIN}$,$\overline{LIN}$, ITRIP, EN)	5.2	5.6	5.9	
I_{HIN+}	Input bias current (HO = High)	-	150	200	μA
I_{HIN-}	Input bias current (HO = Low)	-	110	150	
I_{LIN+}	Input bias current (LO = High)	-	150	200	
I_{LIN-}	Input bias current (LO = Low)	-	110	150	
$V_{RCIN,TH}$	RCIN positive going threshold	-	8	-	V
$V_{RCIN,HY}$	RCIN hysteresis	-	3	-	
I_{RCIN}	RCIN input bias current	-	-	1	μA
$R_{RCIN,ON}$	RCIN low on resistance	-	50	100	Ω
$V_{IT,TH+}$	ITRIP positive going threshold	0.42	0.46	0.5	V
$V_{IT,TH-}$	ITRIP negative going threshold	-	0.4	0.49	
$V_{IT,HY}$	ITRIP hysteresis	-	0.06	-	
I_{ITRIP+}	“High” ITRIP input bias current	-	5	40	μA
I_{ITRIP-}	“Low” ITRIP input bias current	-	-	1	
$V_{EN,TH+}$	Enable positive going threshold	-	-	2.5	V
$V_{EN,TH-}$	Enable negative going threshold	0.8	-	-	
I_{EN+}	“High” Enable input bias current	-	5	40	μA
I_{EN-}	“Low” Enable input bias current	-	-	1	
$R_{FO,ON}$	$\overline{FAULT}$ low on resistance	-	50	100	Ω

Function Timing Diagram

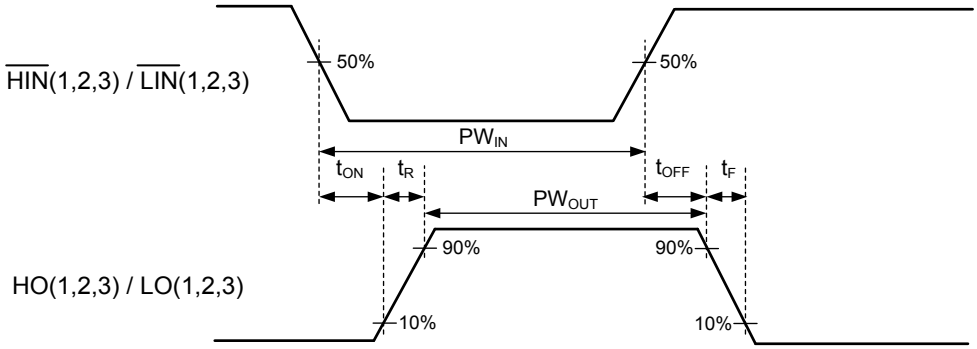


Fig.1 Switching timing waveform

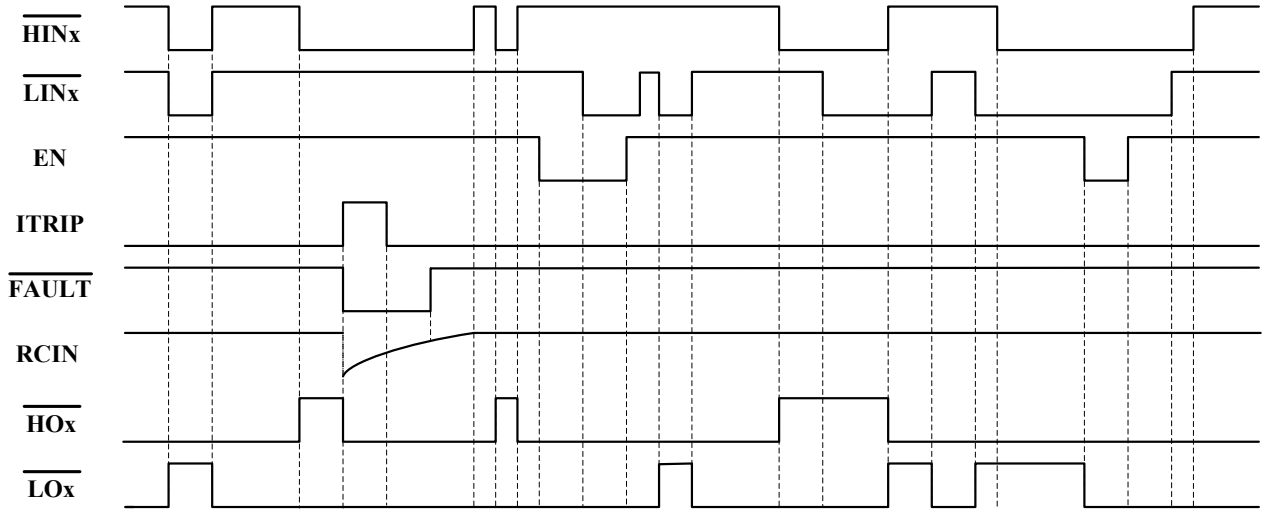


Fig.2 Input/Output timing waveform

Characterization Curves

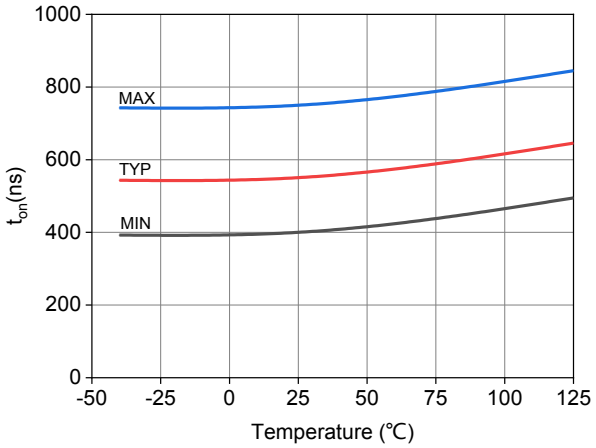


Figure 3: t_{ON} vs. temperature

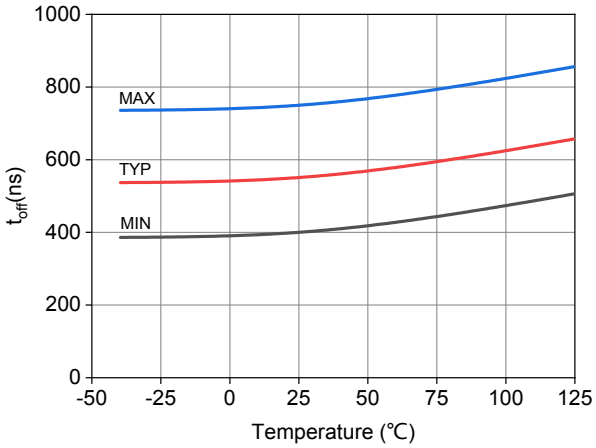


Figure 4: t_{OFF} vs. temperature

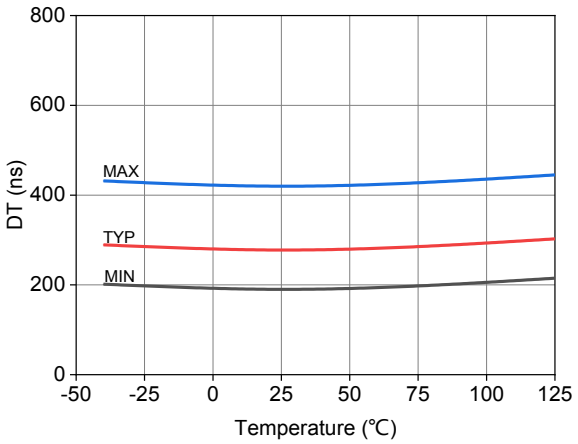


Figure 5: DT vs. temperature

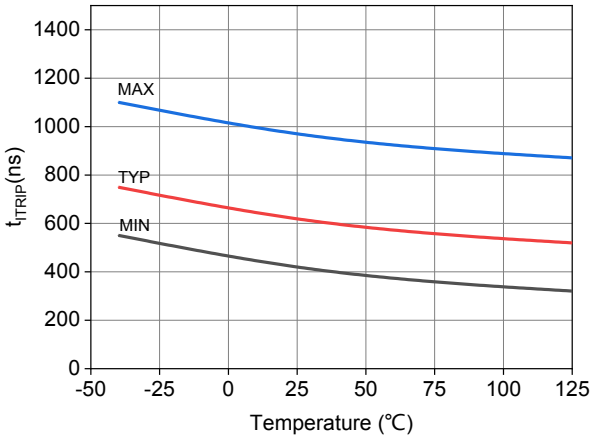


Figure 6: t_{ITRIP} vs. temperature

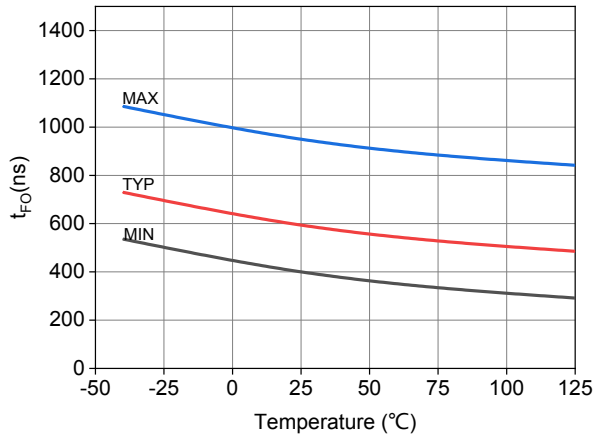


Figure 7: t_{FO} vs. temperature

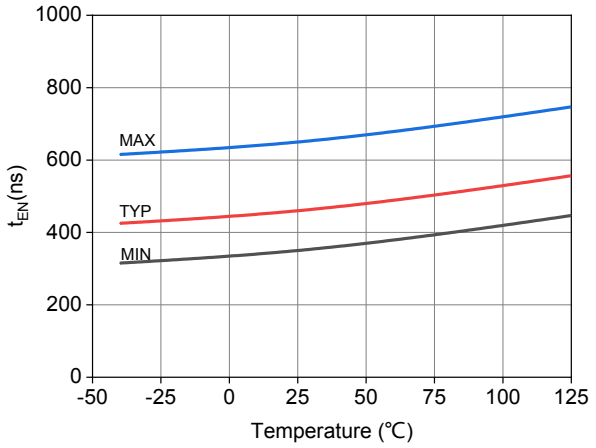


Figure 8: t_{EN} vs. temperature

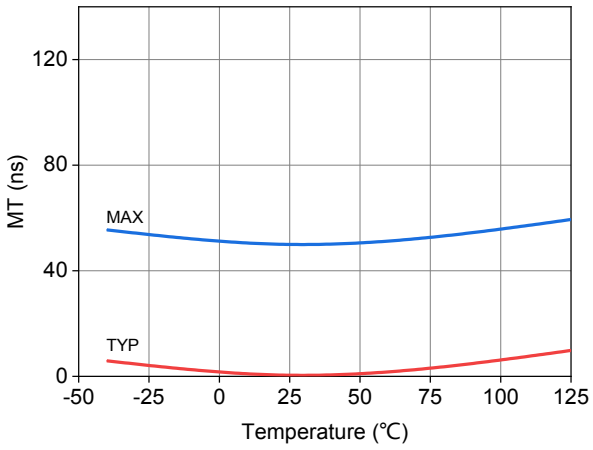


Figure 9: MT vs. temperature Figure

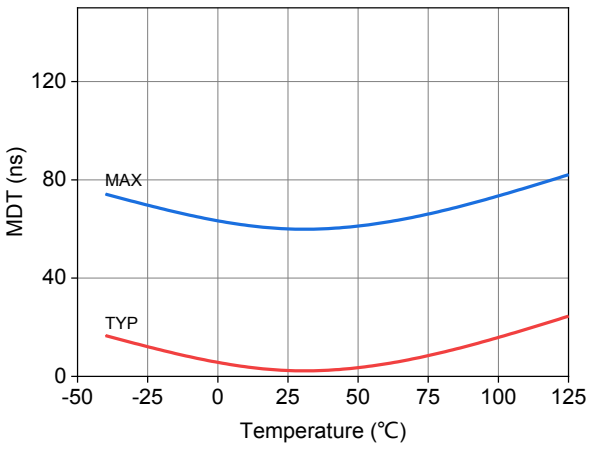


Figure 10: MDT vs. temperature

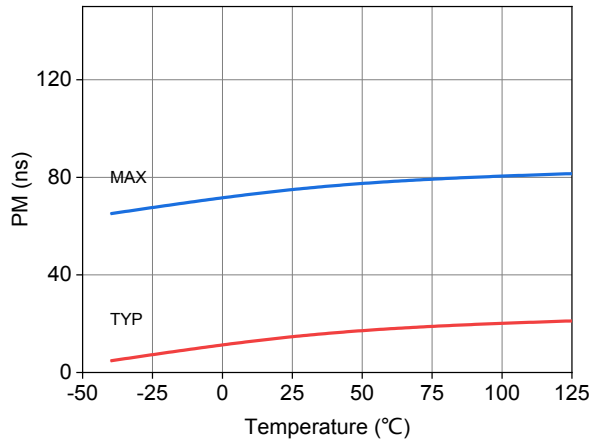


Figure 11: PM vs. temperature Figure

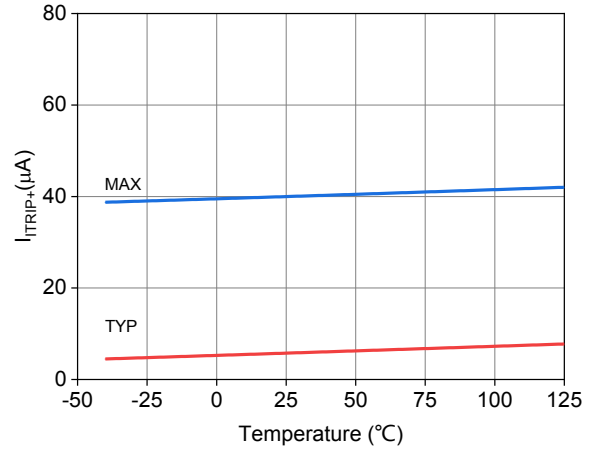


Figure 12: I_{ITRIP+} vs. temperature

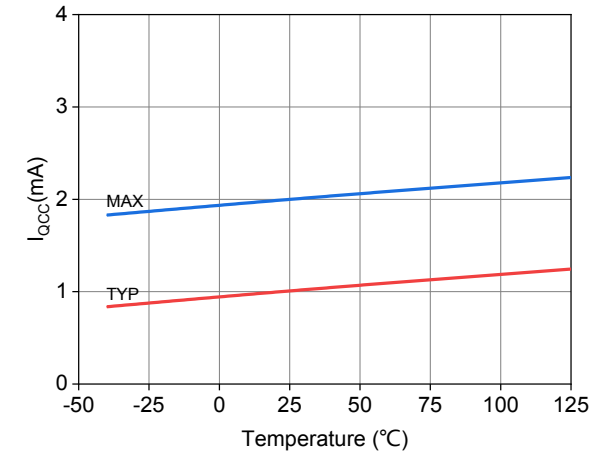


Figure 13: I_{QCC} vs. temperature Figure

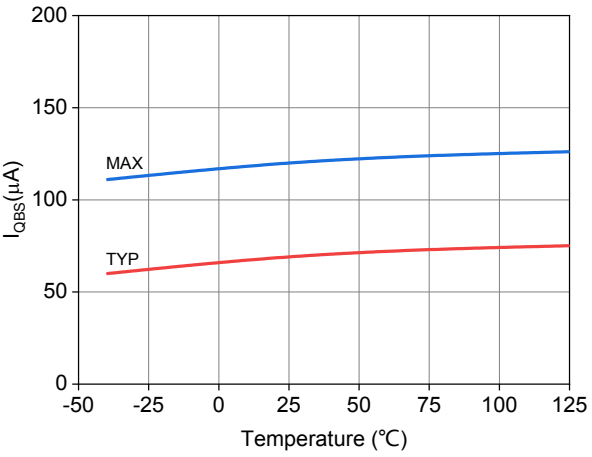


Figure 14: I_{QBS} vs. temperature

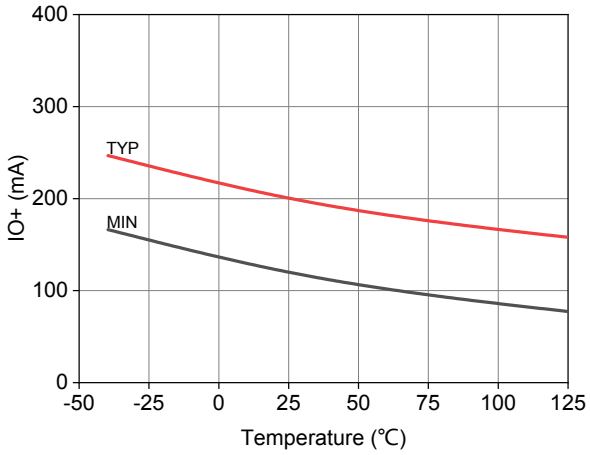


Figure 15: IO+ vs. temperature Figure

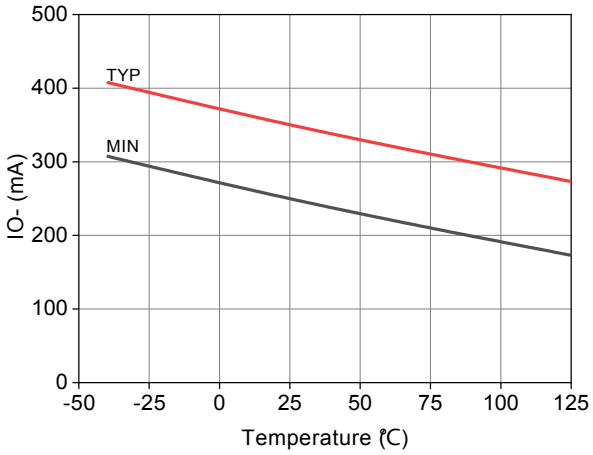


Figure 16: IO- vs. temperature

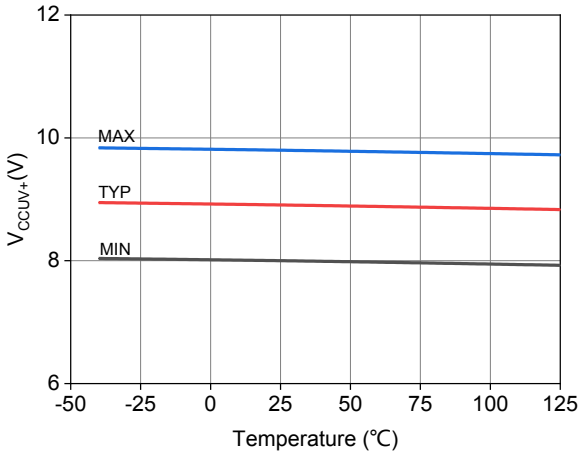


Figure 17: V_{CCUV+} vs. temperature Figure

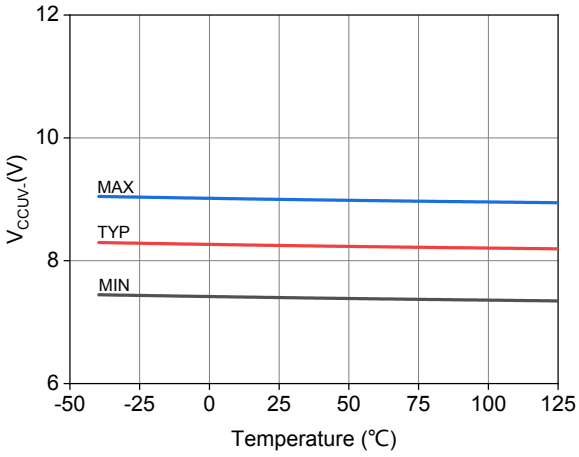


Figure 18: V_{CCUV-} vs. temperature

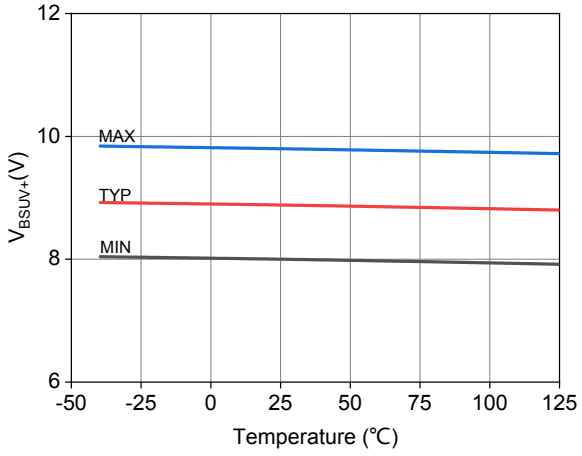


Figure 19: VBSUV+ vs. temperature Figure

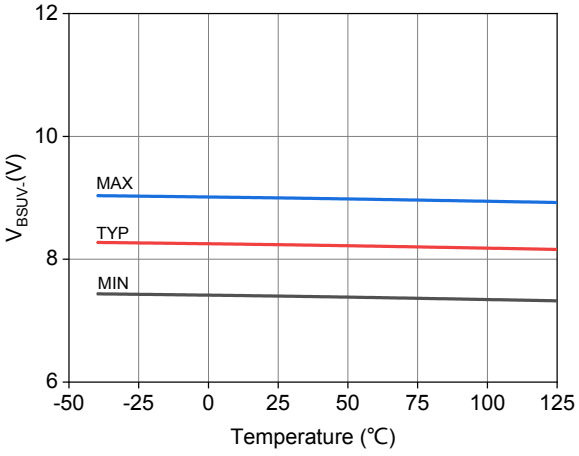


Figure 20: VBSUV- vs. temperature

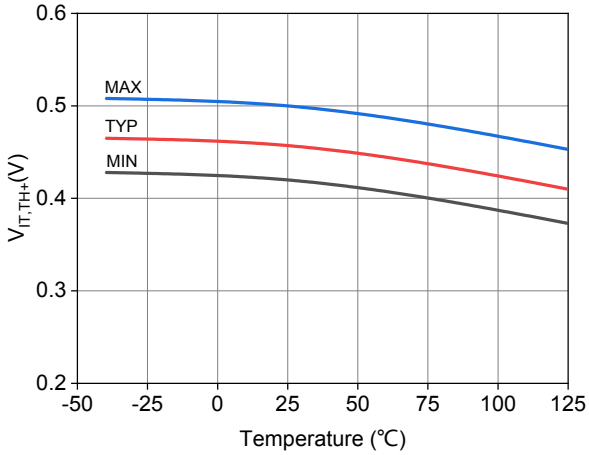


Figure 21: $V_{IT,TH+}$ vs. temperature

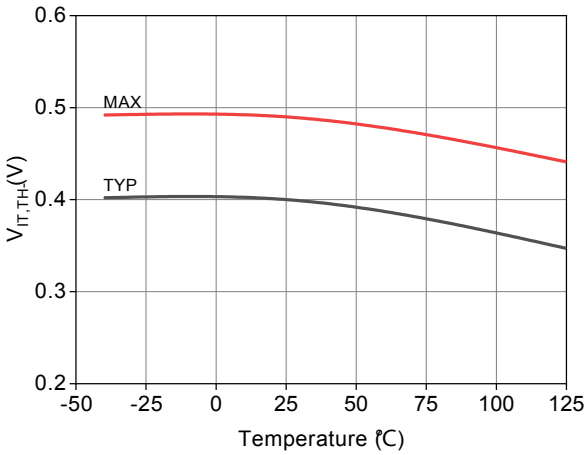


Figure 22: $V_{IT,TH-}$ vs. temperature

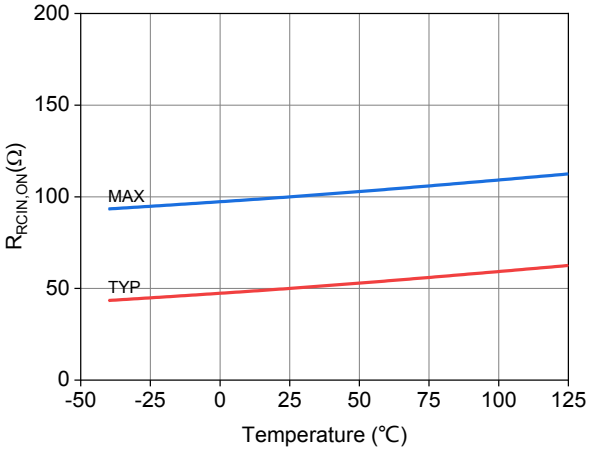


Figure 23: $R_{RCIN,ON}$ vs. temperature

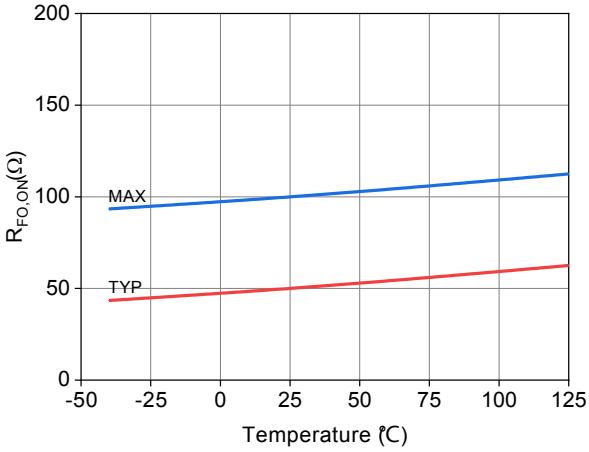


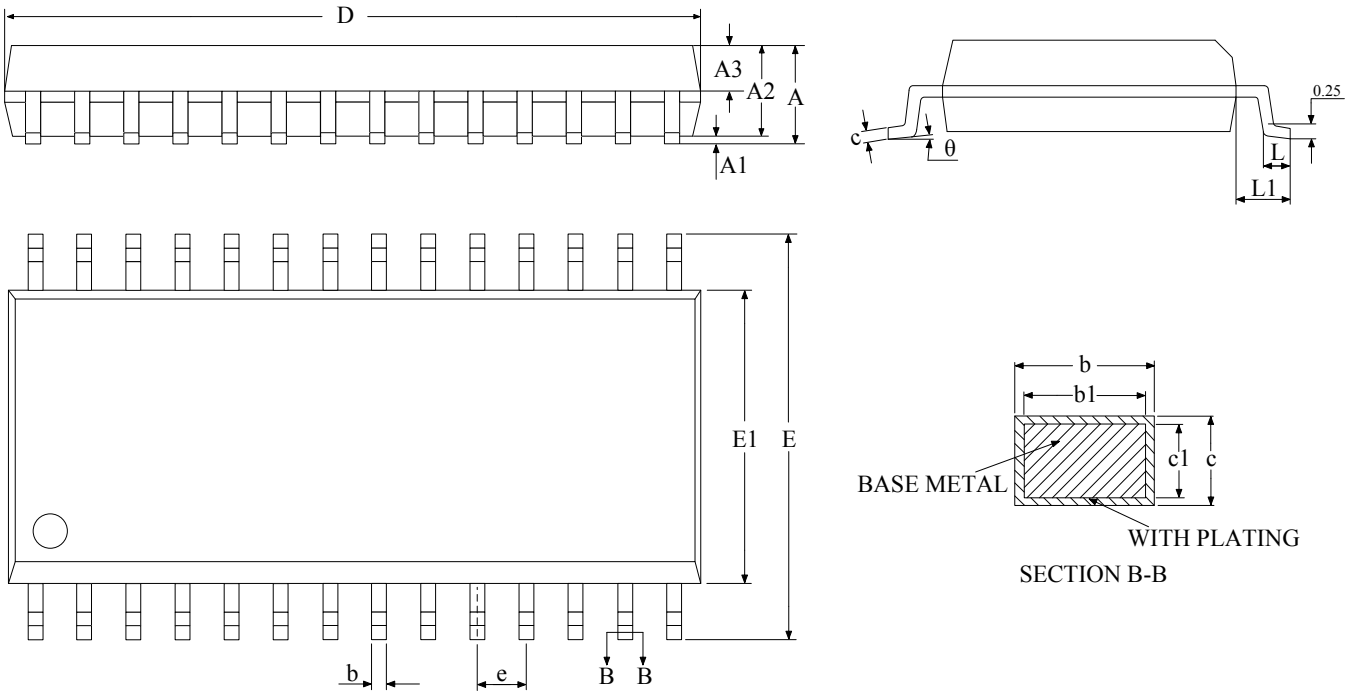
Figure 24: $R_{FO,ON}$ vs. temperature

Package Information

SOIC28 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	2.65	D	17.89	18.09	18.29
A1	0.10	-	0.30	E	10.10	10.30	10.50
A2	2.25	2.30	2.35	E1	7.30	7.50	7.70
A3	0.97	1.02	1.07	e	1.27BSC		
b	0.39	-	0.48	L	0.70	-	1.00
b1	0.38	0.41	0.43	L1	1.40BSC		
c	0.25	-	0.31	θ	0	-	8°
c1	0.24	0.25	0.26				

SOIC28 Package Outlines



Mark	Package
ID7T6036 ABYWX	SOIC28

Note：AB：Product code，Y：Year code； W：Week code； X：Package code