ID9S6015D

600V Half Bridge Gate Drive IC

General Description

The ID9S6015D is a wafer level production, which is a single phase high voltage power MOSFET and IGBT gate driver optimized to drive the gates of both high-side and low-side power transistors. The floating channel driver design can accommodate BUS voltages as high as 600 V. With a wide operation voltage range, high or low side gate drive voltage can be optimized for the best efficiency. Internal non-overlap circuitry further reduces switching losses by preventing simultaneous conduction of both transistors. The Under Voltage Lockout (UVLO) function ensures that both driver outputs are low when the supply voltage is low.

Features

- ❑ Fully operational to+600 V
- ❑ Matched propagation delay for both channels
- ❑ Floating channel designed for bootstrap operation
- ❑ Gate drive supply range from 10 V to 20 V
- ❑ UVLO for both channels
- ❑ Cross Conduction Protection with 540 ns Internal Fixed Dead Time
- ❑ Integrated bootstrap diode
- ❑ Integrated gate on/off resistor
- ❑ Built-in temperature-sensing

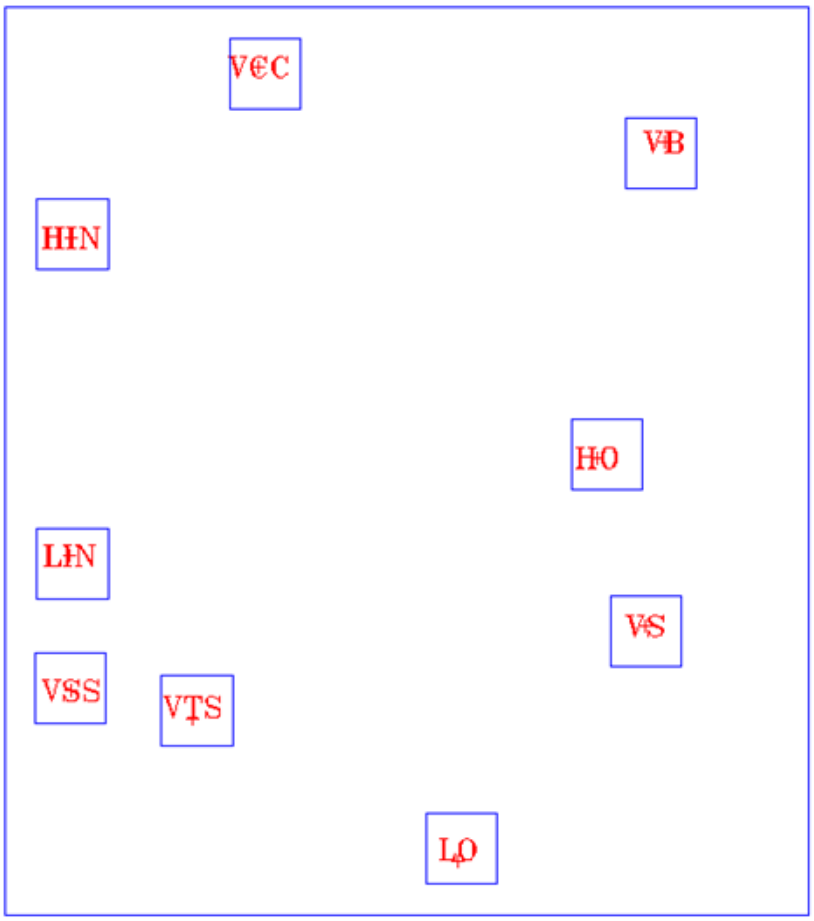
Applications

- ❑ 3A and 5A IPM

Order Information

Part Number	Order Code	Package	Type
ID9S6015D	ID9S6015D	Wafer-level	---

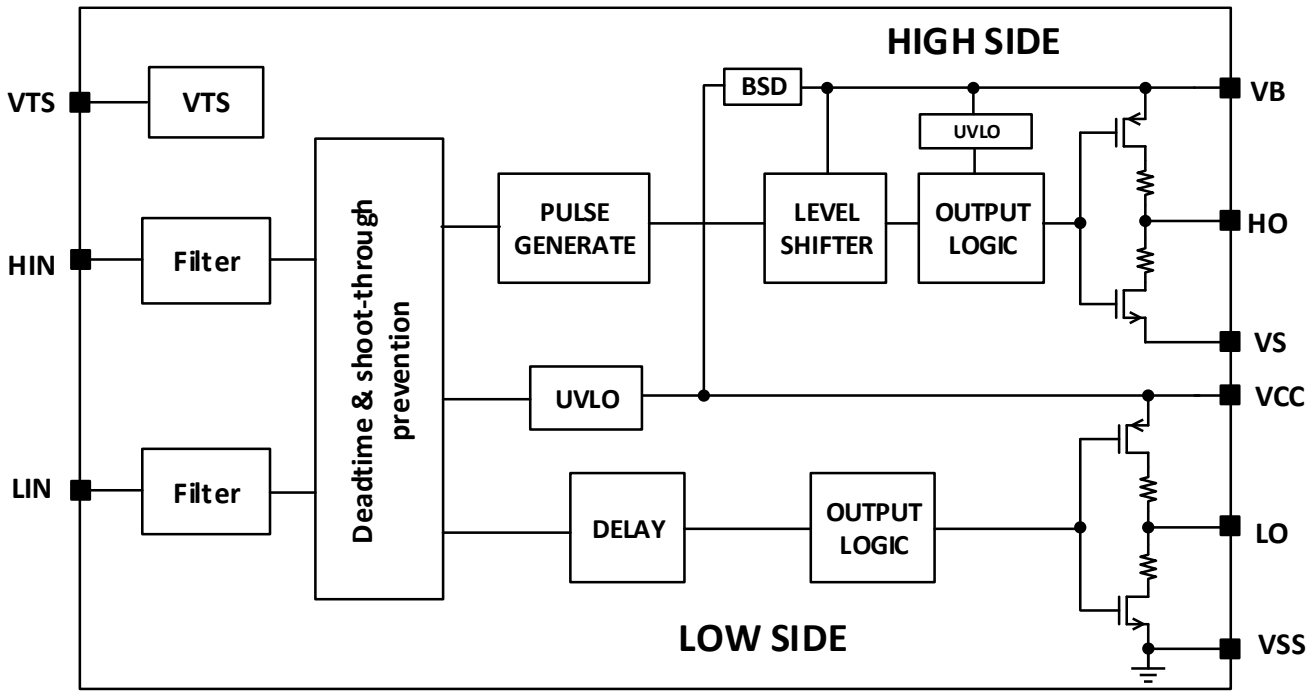
PAD Configuration



PAD Definitions

PIN NAME	PIN FUNCTION
VCC	Low side and main power supply
HIN	Logic input for high side gate driver output
LIN	Logic input for low side gate driver output
VSS	Ground
VTS	Temperature-sensing voltage output
LO	Low side gate drive output
VS	High side floating supply return
HO	High side gate drive output
VB	High side floating supply

Functional Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at T_A=25°C, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_{CC}	Low side supply voltage	-0.3	25	V
V_{IN}	Logic input voltage	V_{SS}-0.3	VCC+0.3	
V_B	High-side floating well supply voltage	-0.3	625	
V_S	High-side floating well supply return voltage	V_B - 25	V_B + 0.3	
V_{HO}	Floating gate drive output voltage	V_S -0.3	V_B + 0.3	
V_{LO}	Low side output voltage	V_{SS}-0.3	V_{CC} + 0.3	
VSS	Power Ground	V_{CC}-25	V_{CC}+0.3	
dV_S/dt	Allowable Vs Offset Supply Transient relative VSS	—	50	V/ns
P_D	Package Power Dissipation @ TA ≤25°C	—	0.625	W
Rth_{JA}	Thermal Resistance, Junction to Ambient	—	200	°C /W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_{CC}	Low-side supply voltage	10	20	V
V_{IN}	HIN &LIN input voltage	V_{SS}	VCC	
V_B	High side floating well supply voltage	VS +10	VS +20	
V_S	High side floating well supply offset voltage	VSS-6	600	
$V_S(t)$	Transient high-side floating supply voltage[Note1]	-50	600	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{LO}	Low-side output voltage	VSS	V_{CC}	
VSS	Power ground	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Operational for transient negative VS of VSS - 50 V with a 50 ns pulse width. Guaranteed by design.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and TA = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
t_{on}	Turn-on propagation delay (without Gate resistor)	400	530	750	ns
t_{off}	Turn-off propagation delay (without Gate resistor)	400	530	750	
t_r	Turn-on rise time (without Gate resistor)	-	120	230	
t_f	Turn-off rise time (without Gate resistor)	-	60	110	
DT	Deadtime is shoot through prevention	400	540	680	
MDT	Matching delay, max (t_{on}, t_{off}) – min (t_{on}, t_{off})	-	-	60	
MT	Matching delay ON and OFF, PW_{IN} - PW_{OUT}.	-	-	50	
PM	Pulse width distortion	-	-	75	

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, TA = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
UV_{CCR}	V_{CC} supply under-voltage positive going threshold	8	8.9	9.8	V
UV_{CCT}	V_{CC} supply under-voltage negative going threshold	7.4	8.2	9	
UV_{CCHYS}	V_{CC} supply under-voltage hysteresis	0.3	0.7	-	
UV_{BSR}	V_{BS} supply under-voltage positive going threshold	8	8.9	9.8	
UV_{BST}	V_{BS} supply under-voltage negative going threshold	7.4	8.2	9	
UV_{BSHYS}	V_{BS} supply under-voltage hysteresis	0.3	0.7	-	
I_{LK}	High-side floating well offset supply leakage	-	-	50	μA
I_{QBS}	Quiescent V_{BS} supply current	-	70	120	
I_{QCC}	Quiescent V_{CC} supply current	-	360	-	
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	-	0.9	1.4	V
V_{OL}	Low level output voltage drop, V_O	-	0.4	0.6	
RP	R connected to PMOS	750	1000	1250	Ω
RN	R connected to NMOS	150	200	250	
V_{IH}	Logic “1” input voltage	2.5	-	-	V
V_{IL}	Logic “0” input voltage	-	-	0.8	
IIN+	Input bias current (HO/LO = High)	-	6	15	μA
IIN-	Input bias current (HO/LO = Low)	-	-	1	
$R_{DS(on)}$	Bootstrap emulator on resistance (VCC=15V)	-	420	-	Ω
Vts	High temperature sensing voltage output@25degree C	600	790	980	mV
	High temperature sensing voltage output@100degree C	1.8	2.25	2.7	V

Function Timing Diagram

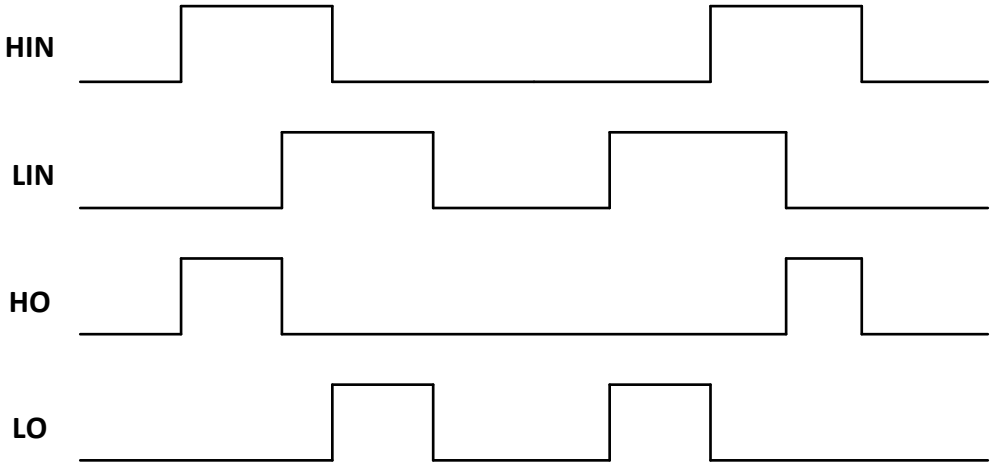


Fig.1 Input / Output Timing Diagram

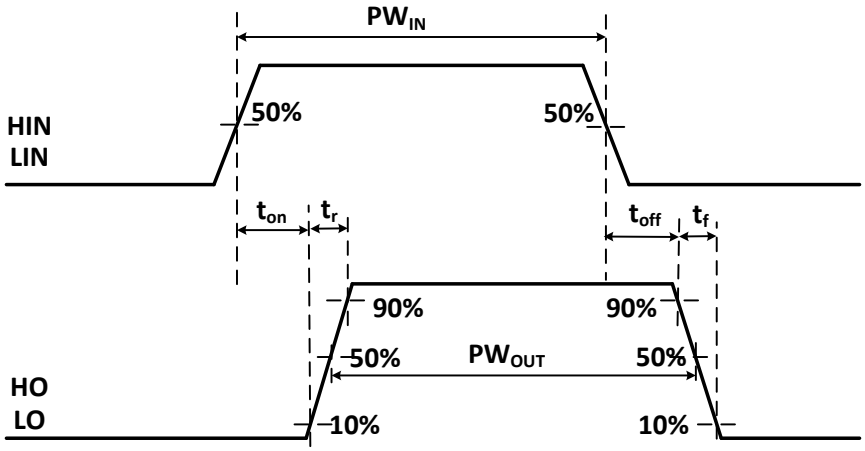


Fig.2 Switching Time Waveform Definitions

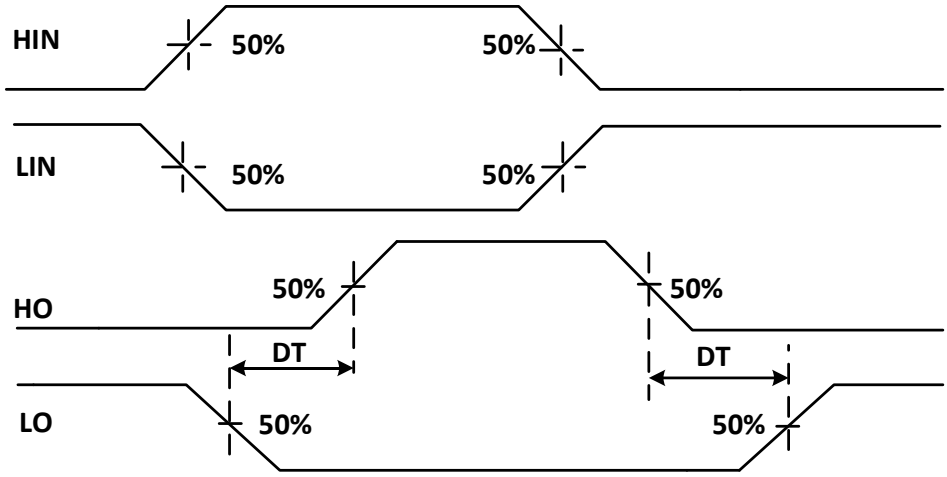


Fig.3 Dead time Waveform Definitions

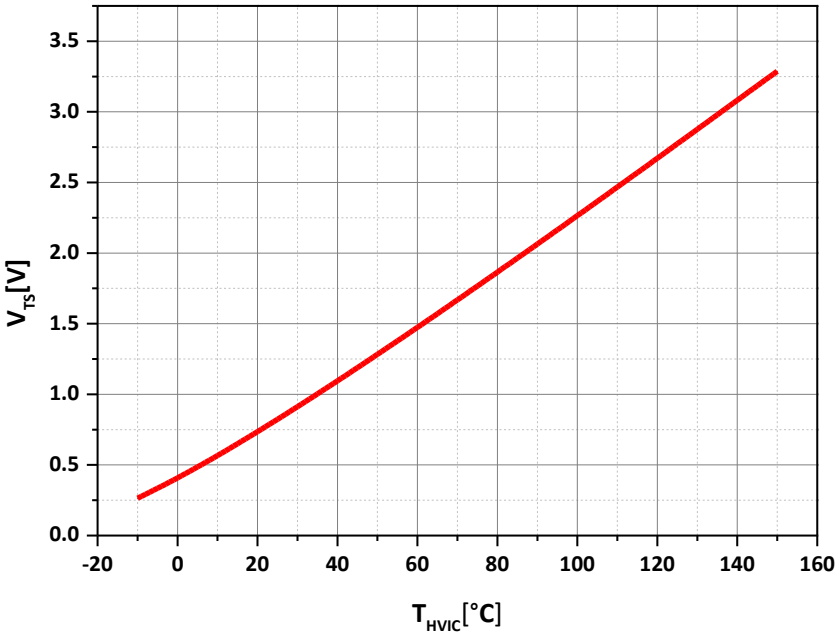


Fig.4 Temperature Profile of V_{TS} (Typical)

Revision Information

Rev 0.0	2019.7.19 approved by Jing