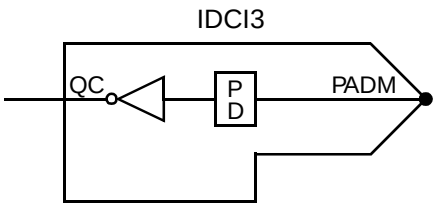
Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCI3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCI3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	12.7	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.62 0.72	0.76 0.87	0.85 0.98	0.92 1.06	0.98 1.14

Delay will vary with input conditions. See page 2-17 for interconnect estimates.