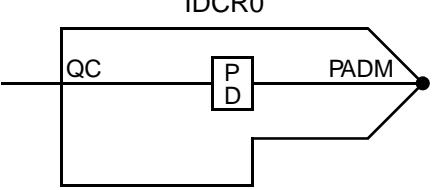


AMI5HG 0.5 micron CMOS Gate Array

Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

| Logic Symbol | Truth Table | Pin Loading | | | | | | | | | | |
|---|---|-------------|----|---|---|---|---|---|------|------|---------|--|
|  | <table border="1"><thead><tr><th>PADM</th><th>QC</th></tr></thead><tbody><tr><td>L</td><td>L</td></tr><tr><td>H</td><td>H</td></tr></tbody></table> | PADM | QC | L | L | H | H | <table border="1"><thead><tr><th>Padm</th><th>Load</th></tr></thead><tbody><tr><td>4.90 pF</td><td></td></tr></tbody></table> | Padm | Load | 4.90 pF | |
| PADM | QC | | | | | | | | | | | |
| L | L | | | | | | | | | | | |
| H | H | | | | | | | | | | | |
| Padm | Load | | | | | | | | | | | |
| 4.90 pF | | | | | | | | | | | | |

HDL Syntax

Verilog IDCR0 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

| Parameter | Value | Units |
|--|-------|---------|
| Static I_{DD} ($T_J = 85^\circ C$) | TBD | nA |
| EQL_{pd} | 2.1 | Eq-load |

See page 2-15 for power equation.

Note: This special purpose, "resistive input" pad is not intended for use as a general input pad.