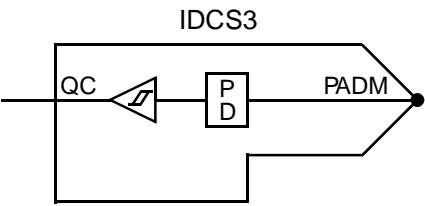


AMI5HG 0.5 micron CMOS Gate Array

Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC											
L	L											
H	H											
	Load											
PADM	4.90 pF											

HDL Syntax

Verilog IDCS3 *inst_name* (QC, PADM);

VHDL *inst_name*: IDCS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	TBD	nA
EQL_{pd}	17.0	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	t_{PLH}	1.37	1.49	1.58	1.65	1.72
			t_{PHL}	1.01	1.19	1.30	1.39	1.47

Delay will vary with input conditions. See page 2-17 for interconnect estimates.