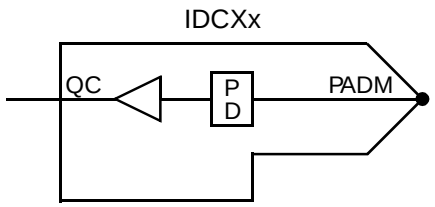
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.90	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	0.0	TBD	10.4
IDCX6	0.0	TBD	18.1

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
IDCX3	From: PADM	t_{PLH}	0.63	0.79	0.90	1.00	1.09
	To: QC	t_{PHL}	0.63	0.76	0.88	0.98	1.07
	Number of Equivalent Loads		**1**	**11**	**22**	**32**	**43 (max)**
IDCX6	From: PADM	t_{PLH}	0.60	0.69	0.75	0.80	0.86
	To: QC	t_{PHL}	0.61	0.66	0.73	0.81	0.90

Delay will vary with input conditions. See page 2-17 for interconnect estimates.