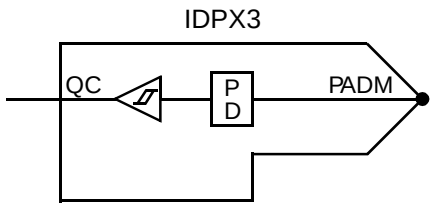
## Description

IDPX3 is a non-inverting, PCI-level input buffer piece. IDPX3 is for the 33MHz PCI ODPSXE16 piece.

**Logic Symbol**




**Truth Table**

| PADM | QC |
|---|---|
| L | L |
| H | H |

### HDL Syntax

Verilog ..... IDPX3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPX3 port map (QC, PADM);

## Pin Loading

| Pin Name | Load |
|---|---|
| | IDPX3 |
| PADM (pF) | 4.90 |

## Power Characteristics

| Cell | Equivalent Gates | Power Characteristics[a] | |
|---|---|---|---|
| | | Static $I_{DD}$ ($T_J$ = 85°C) (nA) | $EQL_{pd}$ (Eq-load) |
| IDPX3 | 0.0 | TBD | 12.6 |

a. See page 2-15 for power equation.

## Propagation Delays (ns)

Conditions: $T_J$ = 25°C, $V_{DD}$ = 5.0V, Typical Process

| | Number of Equivalent Loads | | 1 | 11 | 22 | 32 | 43 (max) |
|---|---|---|---|---|---|---|---|
| IDPX3 | From: PADM | $t_{PLH}$ | 0.58 | 0.75 | 0.86 | 0.94 | 1.02 |
| | To: QC | $t_{PHL}$ | 0.71 | 0.82 | 0.95 | 1.07 | 1.20 |

Delay will vary with input conditions. See page 2-17 for interconnect estimates.