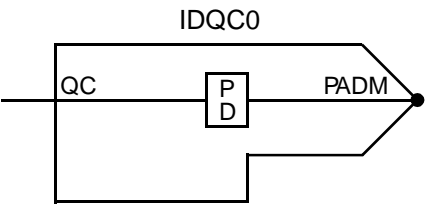


AMI5HG 0.5 micron CMOS Gate Array

Description

IDQCO is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QO</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QO	L	L	H	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QO											
L	L											
H	H											
	Load											
PADM	4.90 pF											

HDL Syntax

Verilog IDQCO *inst_name* (QO, PADM);

VHDL *inst_name*: IDQCO port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	TBD	nA
EQL_{pd}	2.1	Eq-load

See page 2-15 for power equation.

Design Notes:

The IDQCO cell is for backward compatibility with existing oscillator methodologies.