Integrated Device Technology, Inc.

FOUR-BIT CMOS MICROPROCESSOR SLICE

IDT39C01C
IDT39C01D
IDT39C01E

MICROSLICE™ PRODUCT

FEATURES:

- Low-power
  - —I_{CC} (max.)
    - Military — 35mA
    - Commercial — 30mA
- Fast
  - —IDT39C01C — meets 2901C speeds
  - —IDT39C01D — 20% speed upgrade
  - —IDT39C01E — 40% speed upgrade
- Eight-function ALU
  - —Performs addition, two subtraction operations and five logic functions on two source operands
- Expandable
  - —Longer word lengths achieved through cascading any number of IDT39C01s
- Four status flags
  - —Carry, overflow, negative and zero
- Pin compatible and functionally equivalent to the 2901A,B,C
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

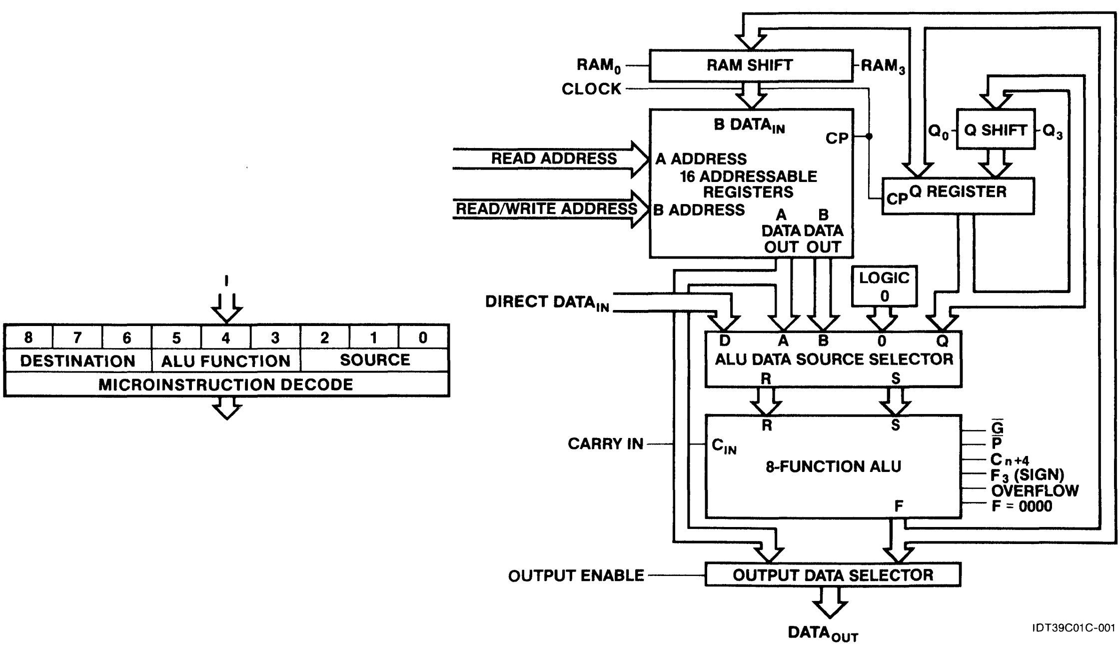
The IDT39C01Cs are high-speed, cascadable ALUs which can be used to implement CPUs, peripheral controllers and programmable microprocessors. The IDT39C01's microinstruction flexibility allows for easy emulation of most digital computers.

This extremely low-power yet high-speed ALU consists of a 16-word by 4-bit dual-port RAM, a high-speed ALU, and the required shifting, decoding and multiplexing logic. It is expandable in 4-bit increments, contains a flag output along with three-state data outputs, and can easily use either a ripple carry or full lookahead carry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU destination register, ALU source operands and the ALU function.

The IDT39C01C is fabricated using CEMOS™, a single poly, double metal CMOS technology designed for high-performance and high-reliability.

The IDT39C01C is a pin-compatible, performance-enhanced, functional replacement for all versions of the 2901.

FUNCTIONAL BLOCK DIAGRAM



IDT39C01C-001

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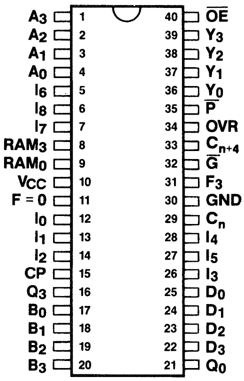
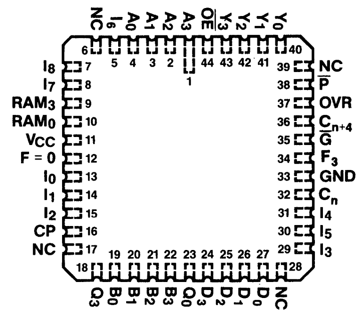


DIP
TOP VIEW

IDT39C01C-002



LCC
TOP VIEW

IDT39C01C-003

FLATPACK
(Consult Factory)

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_3	I	Four address inputs to the register file which selects one register and displays its contents through the A-port.
B_0-B_3	I	Four address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B-port. It also selects the location into which new data can be written when the clock goes LOW.
I_0-I_8	I	Nine instruction control lines which determine what data source will be applied to the ALU $I_{0, 1, 2}$, what function the ALU will perform $I_{3, 4, 5}$, and what data is to be deposited in the Q Register or the register file $I_{6, 7, 8}$.
D_0-D_3	I	Four-bit direct data inputs which are the ALU data source for entering external data into the device. D_0 is the LSB.
Y_0-Y_3	O	Four three-state output lines which, when enabled, display either the four outputs of the ALU or the data on the A-port of the register stack. This is determined by the destination code $I_{6, 7, 8}$.
F_3	O	Most significant ALU output bit (sign-bit).
F=0	O	Open drain output which goes HIGH if the F_0-F_3 ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+4}	O	Carry-out of the internal ALU.
Q_3 RAM_3	I/O	Bidirectional lines controlled by $I_{6, 7, 8}$. Both are three-state output drivers connected to the TTL-compatible CMOS inputs. When the destination code on $I_{6, 7, 8}$ indicates an up shift, the three-state outputs are enabled and the MSB of the Q Register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_3 and RAM_3 lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable which, when pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{G}$,$\overline{P}$	O	Carry generate and carry propagate output of the ALU. These are used to perform a carry-lookahead operation.
OVR	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
CP	I	Clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 16x4 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.

DEVICE ARCHITECTURE:

The IDT39C01 CMOS bit-slice microprocessor is configured four bits wide and is cascadable to any number of bits (4,8,12,16, etc.). Key elements which make up this four-bit-slice microprocessor are: (1) the register file (16x4 dual-port RAM) with shifter, (2) ALU, and (3) Q Register and shifter.

REGISTER FILE—RAM data is read from the A-port as controlled by the 4-bit A address field input. Data, as defined by the B address field input, can be simultaneously read from the B-port of the RAM. This same code can be applied to the A select and B select field with the identical data appearing at both the RAM A-port and B-port outputs simultaneously. New data is written into the file (word) defined by the B address field of the RAM when activated by the RAM write enable. The RAM data input field is driven by a 3-input multiplexer that is used to shift the ALU output data (F). It is capable of shifting the data up one position, down one position, or no shift at all. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins. For a shift up operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. During a shift down operation the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled. Four-bit latches hold the RAM data while the clock is LOW with the A-port output and B-port output each driving separate latches. The data to be written into the RAM is applied from the ALU F output.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer with both having an inhibit capability. Both multiplexers are controlled by the I_0, I_1, I_2 inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q, and "0" inputs as source operands to the ALU. Microinstruction inputs (I_3, I_4, I_5) are used to select the ALU function. This high-speed ALU also incorporates a carry-in (C_n) input, carry propagate ($\overline{P}$) output, carry generate ($\overline{G}$) output and carry-out (C_{n+4}) all aimed at accelerating arithmetic operations by the use of carry-lookahead logic. The overflow output pin (OVR) will be HIGH when arithmetic operations exceed the two's complement number range. The ALU data outputs (F_0, F_1, F_2, F_3) are routed to the RAM Q Register inputs and the Y outputs under control of the I_6, I_7, I_8 control signal inputs. The MSB of the ALU is output as F_3 so the user can examine the sign-bit without enabling the three-state outputs. An open drain output, F=0, is HIGH when $F_0 = F_1 = F_2 = F_3 = 0$ so that the user can determine when the ALU output is zero by wire-ORing these outputs together.

Q REGISTER—The Q Register is a separate 4-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q Register. In either the shift-up or shift-down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_3, which operate comparably to the RAM shifter. They are controlled by the I_6, I_7, I_8 inputs.

The clock input of the IDT39C01 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and RAM EN is enabled, new data will be written into the RAM file defined by the B address field.

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	$R + S$
SUBR	L	L	H	1	S Minus R	$S - R$
SUBS	L	H	L	2	R Minus S	$R - S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \nabla S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \nabla S}$

ALU DESTINATION CONTROL

MNEMONIC	MICROCODE				RAM FUNCTION		Q REGISTER FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	OCTAL CODE	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB; DOWN is toward LSB.

SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL							
		0	1	2	3	4	5	6	7
				ALU SOURCE					
		A,Q	A,B	0,Q	0,B	O,A	D,A	D,Q	D,0
0	R Plus S, C_n = L	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	S Minus R, C_n = L	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D - 1	Q - D - 1	-D - 1
	C_n = H	Q - A	B - A	Q	B	A	A - D	Q - D	-D
2	R Minus S, C_n = L	A - Q - 1	A - B - 1	-Q - 1	-B - 1	-A - 1	D - A - 1	D - Q - 1	D - 1
	C_n = H	A - Q	A - B	-Q	-B	-A	D - A	D - Q	D
3	**R OR S**	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	**R AND S**	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	**$\overline{R}$ AND S**	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	**R EX-OR S**	$A \nabla Q$	$A \nabla B$	Q	B	A	$D \nabla A$	$D \nabla Q$	D
7	**R EX-NOR S**	$\overline{A \nabla Q}$	$\overline{A \nabla B}$	Q	B	$\overline{A}$	$\overline{D \nabla A}$	$\overline{D \nabla Q}$	$\overline{D}$

+ = PLUS; - = MINUS; $\wedge$ = AND; ∇ = EX-OR; V = OR

ALU LOGIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$, $I_{2,1,0}$	GROUP	FUNCTION
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \nabla Q$
6 1		$A \nabla B$
6 5		$D \nabla A$
6 6		$D \nabla Q$
7 0	EX-NOR	$\overline{A \nabla Q}$
7 1		$\overline{A \nabla B}$
7 5		$\overline{D \nabla A}$
7 6		$\overline{D \nabla Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

ALU ARITHMETIC MODE FUNCTIONS

OCTAL	$C_n = L$		$C_n = H$	
$I_{5,4,3}$, $I_{2,1,0}$	GROUP	FUNCTION	GROUP	FUNCTION
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

DEFINITIONS

$P_0 = R_0 + S_0$
$P_1 = R_1 + S_1$
$P_2 = R_2 + S_2$
$P_3 = R_3 + S_3$
$G_0 = R_0S_0$
$G_1 = R_1S_1$
$G_2 = R_2S_2$
$G_3 = R_3S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

+ = OR

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4}, AND OVR

$I_{5,4,3}$	FUNCTION	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \nabla C_4$
1	S - R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R - S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	$R \vee S$	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	$R \wedge S$	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	← Same as $R \wedge S$ equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	$R \nabla S$	← Same as $\overline{R \nabla S}$ equations, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \nabla S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + \overline{C_n})}$	See Note 2

NOTES:
1. + = OR
2. $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \nabla [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = +5.0V ± 5%   Min. = +4.75V   Max. = +5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = +5.0V ± 10%   Min. = +4.50V   Max. = +5.50V (Military)
V_{LC} = +0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(3)	MAX.	UNITS
I_{IH}	Output Short Circuit Current (All Inputs)	V_{CC} = Max. V_{IN} = V_{CC}		—	0.1	5	μA
I_{IL}	Input Low Current (All Inputs)	V_{CC} = Max. V_{IN} = GND		—	-0.1	-5	μA
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} = or V_{IL}	I_{OH} = -1.0mA (MIL.)	2.4	4.3	—	V
			I_{OH} = -1.6mA (COM'L.)	2.4	4.3	—	
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} = or V_{IL}	I_{OL} = 16mA (MIL.)	—	0.3	0.5	V
			I_{OL} = 20mA (COM'L.)	—	0.3	0.5	
V_{IH}	Input High Voltage	(1)		2.0	—	—	V
V_{IL}	Input Low Voltage	(1)		—	—	0.8	V
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = HIGH Z		-40	—	40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0V(2)		-30	—	-130	mA

NOTES:

1. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
2. Not more than one output should be shorted at a time. Duration of the short circuit test shall not exceed one second.
3. V_{CC} = +5.0V @ T_A +25°C.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = +5.0V ± 5% Min. = +4.75V Max. = +5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% Min. = +4.50V Max. = +5.50V (Military)
V_{LC} = +0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.[3]	MAX.	UNITS
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = H			—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = L			—	—	—	mA
I_{CCT}	Quiescent Input Power Supply[4] Current (per Input @ TTL High)	V_{CC} = Max., V_{IN} = 3.4V, f_{CP} = 0			—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L		MIL.	—	—	—	mA/ MHz
				COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[5]	V_{CC} = Max., Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	IDT39C01C f_{CP} = 10MHz	MIL.	—	—	—	mA
				COM'L.	—	—	—	
			IDT39C01D f_{CP} = 15MHz	MIL	—	—	—	
				COM'L.	—	—	—	
			IDT39C01E f_{CP} = 17.5MHz	MIL.	—	—	—	
				COM'L.	—	—	—	
		V_{CC} = Max., Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IN} = 3.4V, V_{IN} = 0	IDT39C01C f_{CP} = 10MHz	MIL.	—	—	35	
				COM'L.	—	—	30	
			IDT39C01D f_{CP} = 15MHz	MIL.	—	—	40	
				COM'L.	—	—	35	
			IDT39C01E f_{CP} = 17.5MHz	MIL.	—	—	45	
				COM'L.	—	—	40	

NOTES:

4. I_{CCQT} is derived by measuring the total current with all the inputs tied togetherat 3.4V, subtracting I_{CCQH}, then dividing by the total number of inputs.
5. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock Input Frequency.

IDT39C01C
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01C over the -55°C to +125°C and 0°C to +70°C temperature ranges. V_{CC} is specified at 5V ± 10%. All times are in nanoseconds and are measured between the 1.5V signal level. The input switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	32	31	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=432 or 632)	31	32	MHz
Minimum Clock LOW Time	15	15	ns
Minimum Clock HIGH Time	15	15	ns
Minimum Clock Period	32	31	ns

COMBINATIONAL PROPAGATION DELAYS(1) (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		F_3		C_{n+4}		$\overline{G},\overline{P}$		F=0		OVR		RAM_0 RAM_3		Q_0 Q_3		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Address	48	40	48	40	48	40	44	37	48	40	48	40	48	40	—	—	ns
D	37	30	37	30	37	30	34	30	40	38	37	30	37	30	—	—	ns
C_n	25	22	25	22	21	20	—	—	28	25	25	22	28	25	—	—	ns
$I_{0,1,2}$	40	35	40	35	40	35	44	37	44	37	40	35	40	35	—	—	ns
$I_{3,4,5}$	40	35	40	35	40	35	40	35	40	38	40	35	40	35	—	—	ns
$I_{6,7,8}$	29	25	—	—	—	—	—	—	—	—	—		29	26	29	26	ns
A Bypass ALU (I=2XX)	40	35	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock ⟋	40	35	40	35	40	35	40	35	40	35	40	35	40	35	33	28	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	15	15	2	1(3)	30, 15+TPWL(4)		2	1	ns
B Destination Address	15	15	Do not change(2)				2	1	ns
D	—(1)	—	—	—	25	25	0	0	ns
C_n	—	—	—	—	20	20	0	0	ns
$I_{0,1,2}$	—	—	—	—	30	30	0	0	ns
$I_{3,4,5}$	—	—	—	—	30	30	0	0	ns
$I_{6,7,8}$	10	10	Do not change(2)				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	—	—	—	—	12	12	0	0	ns

OUTPUT ENABLE/DISABLE TIMES
(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L
$\overline{OE}$	Y	25	23	25	23

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the H→L transition occurs.

IDT39C01D AC ELECTRICAL CHARACTERISTICS

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01D over the -55°C to +125°C and 0°C to +70°C temperature ranges. V_{CC} is specified at 5V ± 10%. All times are in nanoseconds and are measured between the 1.5V signal level. The input switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	27	23	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=432 or 632)	37	43	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	27	23	ns

COMBINATIONAL PROPAGATION DELAYS(1) (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		F_3		C_{n+4}		$\overline{G}$,$\overline{P}$		F=0		OVR		RAM_0 RAM_3		Q_0 Q_3		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Address	33	30	33	30	33	30	33	28	33	30	33	30	33	30	—	—	ns
D	24	21	23	20	23	20	21	20	25	24	24	21	25	22	—	—	ns
C_n	18	17	17	16	14	14	—	—	19	18	17	16	19	18	—	—	ns
$I_{0,1,2}$	28	26	27	25	26	24	28	24	29	25	27	24	27	25	—	—	ns
$I_{3,4,5}$	27	26	27	24	26	24	26	24	27	26	26	24	27	26	—	—	ns
$I_{6,7,8}$	18	16	—	—	—	—	—	—	—	—	—		21	21	21	21	ns
A Bypass ALU (I=2XX)	26	24	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock _/‾	27	24	26	23	26	23	25	23	27	24	26	24	27	24	20	19	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	11	10	0	0(3)	24, 11+TPWL(4)	21, 10+TPWL(4)	2	1	ns
B Destination Address	11	10	Do not change(2)				2	1	ns
D	—(1)	—	—	—	16	16	0	0	ns
C_n	—	—	—	—	13	13	0	0	ns
$I_{0,1,2}$	—	—	—	—	19	19	0	0	ns
$I_{3,4,5}$	—	—	—	—	19	19	0	0	ns
$I_{6,7,8}$	7	7	Do not change(2)				0	0	ns
$RAM_{0,3}$,$Q_{0,3}$	—	—	—	—	9	9	0	0	ns

OUTPUT ENABLE/DISABLE TIMES

(C_L=5pF, measured to 0.5V change of V_{OUT})

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L
$\overline{OE}$	Y	16	14	18	16

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the H→L transition occurs.

IDT39C01E
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01E over the -55°C to +125°C and 0°C to +70°C temperature ranges. V_{CC} is specified at 5V ± 10%. All times are in nanoseconds and are measured between the 1.5V signal level. The input switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	21	20	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=432 or 632)	46	50	MHz
Minimum Clock LOW Time	10	8	ns
Minimum Clock HIGH Time	10	8	ns
Minimum Clock Period	21	20	ns

COMBINATIONAL PROPAGATION DELAYS(1) (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		F_3		C_{n+4}		$\overline{G}$,$\overline{P}$		F=0		OVR		RAM_0 RAM_3		Q_0 Q_3		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Address	26	22	26	22	26	22	26	21	26	22	26	22	26	22	—	—	ns
D	18	16	17	15	17	15	16	15	19	18	18	16	19	16	—	—	ns
C_n	13	13	13	12	10	10	—	—	14	13	13	12	14	13	—	—	ns
$I_{0,1,2}$	21	20	20	19	19	18	21	18	22	19	20	18	20	19	—	—	ns
$I_{3,4,5}$	20	20	20	18	19	18	19	18	20	20	19	18	20	20	—	—	ns
$I_{6,7,8}$	13	12	—	—	—	—	—	—	—	—	—		16	16	16	16	ns
A Bypass ALU (I=2XX)	19	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock _/‾	20	18	19	17	19	17	19	17	20	18	19	18	20	18	15	15	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	8	7	0	0(3)	18,8 +TPWL(4)	15, 7 + TPWL(4)	2	1	ns
B Destination Address	8	7	Do not change(2)				2	1	ns
D	—(1)	—	—	—	12	12	0	0	ns
C_n	—	—	—	—	10	10	0	0	ns
$I_{0,1,2}$	—	—	—	—	14	14	0	0	ns
$I_{3,4,5}$	—	—	—	—	14	14	0	0	ns
$I_{6,7,8}$	5	5	Do not change(2)				0	0	ns
$RAM_{0,3}$,$Q_{0,3}$	—	—	—	—	7	7	0	0	ns

OUTPUT ENABLE/DISABLE TIMES
(C_L=5pF, measured to 0.5V change of V_{OUT})

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L
$\overline{OE}$	Y	14	10	12	12

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the H→L transition occurs.

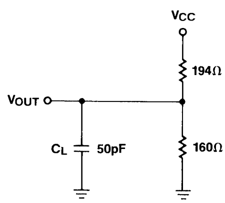
AC TEST CONDITIONS

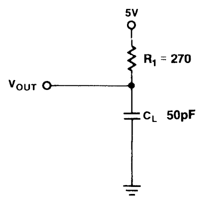
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1, 2

CAPACITANCE (T_A = +25° C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.



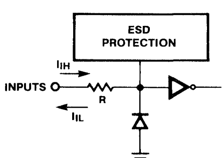


IDT39C01C-006

Figure 1. All Outputs (Except f = 0)

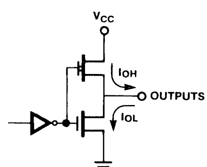
Figure 2. Open Drain Output (f = 0)

INPUT/OUTPUT INTERFACE CIRCUITRY



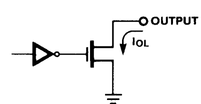
IDT39C01C-007

Figure 1. Input Structure (All Inputs)



IDT39C01C-008

Figure 2. Output Structure (All Outputs Except F = 0)



IDT39C01C-009

Figure 3. Output Structure (F = 0 Only)

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