



Integrated Device Technology, Inc.

CMOS CARRY LOOKAHEAD GENERATOR

IDT39C02A

MICROSLICE™ PRODUCT

FEATURES:

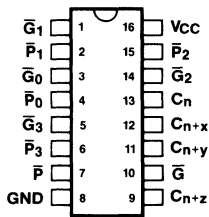
- Provides lookahead carries across any number of 4-bit microprocessor ALUs
- Very high-speed and output drive over full temperature and voltage supply extremes
- 6ns typical propagation delay
- $I_{OL} = 32mA$ over full military temperature range
- CMOS power levels ($5\mu W$ typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than bipolar ($5\mu A$ max.)
- 100% product assurance screening to MIL-STD-883, Class B available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT39C02A is a high-speed carry lookahead generator built using advanced CEMOS™ II, a dual metal $1.5\mu m$ CMOS technology. The IDT39C02A is generally used with an arithmetic logic unit to provide high-speed lookahead over larger word lengths.

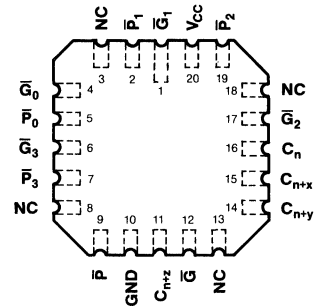
The IDT39C02A is a pin-compatible, performance enhanced, functional replacement for all versions of the 2902.

PIN CONFIGURATIONS



SSDFCT182-001

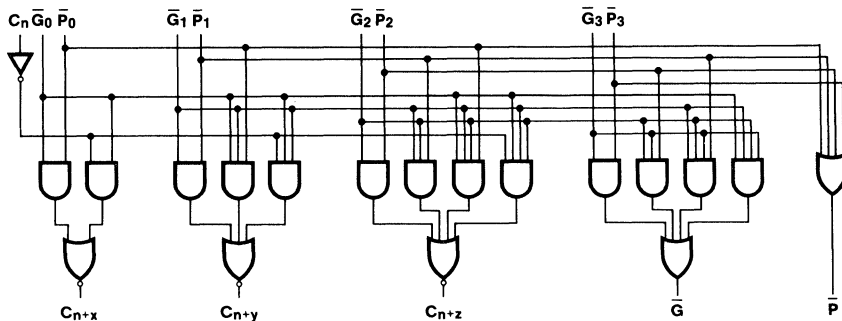
DIP
TOP VIEW



SSDFCT182-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT182-003

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

$$T_A = 0^\circ\text{C to } +70^\circ\text{C}$$

$$V_{CC} = 5.0\text{V} \pm 5\%$$

$$\text{Min.} = 4.75\text{V}$$

$$\text{Max.} = 5.25\text{V (Commercial)}$$

$$T_A = -55^\circ\text{C to } +125^\circ\text{C}$$

$$V_{CC} = 5.0\text{V} \pm 10\%$$

$$\text{Min.} = 4.50\text{V}$$

$$\text{Max.} = 5.50\text{V (Military)}$$

$$V_{LC} = 0.2\text{V}$$

$$V_{HC} = V_{CC} - 0.2\text{V}$$

SYMBOL	PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN.	TYP. ⁽²⁾	MAX.	UNIT	
V _{IH}	Input HIGH Level	Guaranteed Logic High Level	2.0	—	—	V	
V _{IL}	Input LOW Level	Guaranteed Logic Low Level	—	—	0.8	V	
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}	—	—	5	μA	
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND	—	—	-5	μA	
I _{SC}	Short Circuit Current	V _{CC} = Max. ⁽³⁾	-60	-120	—	mA	
V _{OH}	Output HIGH Voltage	V = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -300μA	V _{HC}	V _{CC}	—	V
		I _{OH} = -12mA MIL	2.4	4.3	—		
		I _{OH} = -15mA COM	2.4	4.3	—		
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 300μA	—	GND	V _{LC}	V
		I _{OL} = 32mA MIL	—	0.3	0.5		
		I _{OL} = 48mA COM	—	0.3	0.5		
I _{CCOC}	Quiescent Power Supply Current (CMOS Inputs)	V _{CC} = Max. V _{HC} ≤ V _{IN} ≤ V _{LC} f = 0	—	0.001	2.0	mA	
I _{CCOT}	Quiescent Power Supply Current (TTL Inputs)	V _{CC} = Max. V _{IN} = 3.4V ⁽⁴⁾	—	0.5	2.5	mA	
I _{CCD}	Dynamic Power Supply Current	V _{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	V _{HC} ≤ V _{IN} ≤ V _{LC}	—	0.15	—	mA/ MHz
I _{CC}	Total Power Supply ⁽⁵⁾ Current	V _{CC} = Max. f = 10 MHz Outputs Open 50% Duty Cycle One Input Toggling	V _{HC} ≤ V _{IN} ≤ V _{LC}	—	1.5	—	mA
		V _{IN} = 3.4V ⁽⁴⁾	—	2.0	—		
		All Inputs V _{IN} = 3.4V ⁽⁴⁾	—	16.0	—		

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- I_{CC} = I_{CCOC} + (I_{CCOT} × N_T) + (I_{CCD} × f × N) + (I_{CCOT} × D × N_D)
 N = Total number of inputs toggling.
 f = Frequency in MHz.
 D = Percent high duty cycle.
 N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
 N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G_0}, \overline{G_1}, \overline{G_2}, \overline{G_3}$	Carry Generate Inputs (Active LOW)
$\overline{P_0}, \overline{P_1}, \overline{P_2}, \overline{P_3}$	Carry Propagate Inputs (Active LOW)
$C_{n+x} - C_{n+z}$	Carry Outputs
G	Carry Generate Output (Active LOW)
P	Carry Propagate Output (Active LOW)

TRUTH TABLE

INPUTS										OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3		C_{n+x}	C_{n+y}	C_{n+z}	G	P
X	H	H								L				
L	H	X								L				
X	L	X								H				
H	X	L								H				
X	X	X	H	H							L			
X	H	H	H	H	X						L			
L	H	X	H	X	X						L			
X	X	X	L	X	X						L			
X	L	X	X	L	X						H			
H	X	L	X	L	X						H			
X	X	X	X	X	H	H						L		
X	X	X	H	H	H	X						L		
L	H	X	H	X	H	X						L		
X	X	X	X	X	L	X						H		
X	X	X	L	X	X	L						H		
X	L	X	X	L	X	L						H		
H	X	L	X	L	X	L						H		
X	X		X	X	X	X	H	H					H	
X			X	X	H	H	H	X					H	
X			H	X	H	X	H	X					H	
X			X	X	X	X	L	X					L	
X			X	X	L	X	X	X					L	
X			L	X	X	L	X	L					L	
L			X	X	X	L	X						L	
		H		X		X		X						H
		X		H		X		X						H
		X		X		H		X						H
		X		X		X		H						H
		L		L		L		L						L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_N to $C_{N+x}, C_{N+y}, C_{N+z}$	$C_L = 50$ pf $R_L = 500\Omega$	6.0	3.0	14.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay $P_0, P_1,$ or $P_2,$ to $C_{N+x}, C_{N+y}, C_{N+z}$		6.0	2.0	9.0	2.0	11.5	ns
t_{PLH} t_{PHL}	Propagation Delay $G_0, G_1,$ or $G_2,$ to $C_{N+x}, C_{N+y}, C_{N+z}$		6.0	2.0	9.5	2.0	11.5	ns
t_{PLH} t_{PHL}	Propagation Delay $P_1, P_2,$ or $P_3,$ to G		7.0	3.0	12.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay G_N to G		7.5	3.0	12.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_N to P		6.0	2.5	11.0	2.5	12.5	ns