Integrated Device Technology, Inc.

16-WORD BY 4-BIT DUAL-PORT RAM

ADVANCE INFORMATION
IDT39C705A/B
IDT39C707/A

FEATURES:

- Fast
  - —Available in either industry-standard speed or 20% speed upgraded versions
- Low-power CEMOS™
  - —Military — 50mA (max.)
  - —Commercial — 40mA (max.)
- 16-word x 4-bit, dual-port CMOS RAM
- Non-inverting data output with respect to data input
- Easily cascadable with separate Chip Select and Write Enable
- Separate 4-bit latches with enables for each output port (IDT39C707/A has separate output control)
- IDT39C705A/B pin-compatible to all versions of the 29705
- IDT39C707/A pin-compatible to all versions of the 29707
- Available in 28-pin DIP and LCC
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C705s are high-performance 16-word by 4-bit, dual-port RAMs. Addressing any of the 16-words is performed via the 4-bit A address field with the data appearing on the A output port. The same respective operation holds true for the B address input/output port and can happen simultaneously with the A-port operation. New incoming data is written into the 4-bit RAM word selected by the B address. The D inputs are used to load new data into the device.

Featured are two separate output ports which allow any two 4-bit words to be read from these outputs simultaneously. Also featured is a 4-bit latch for each of the two output ports with a common Latch Enable (LE) input being used to control all eight latches. Two Write Enable ($\overline{WE}$) inputs are designed such that Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) inputs can be connected to the RAM to operate in an edge-triggered mode. The Write Enable inputs control the writing of new data into the RAM. Data is written into the B address field when both Write Enables are LOW. If either of the Write Enables are HIGH, no data is written into the RAM.

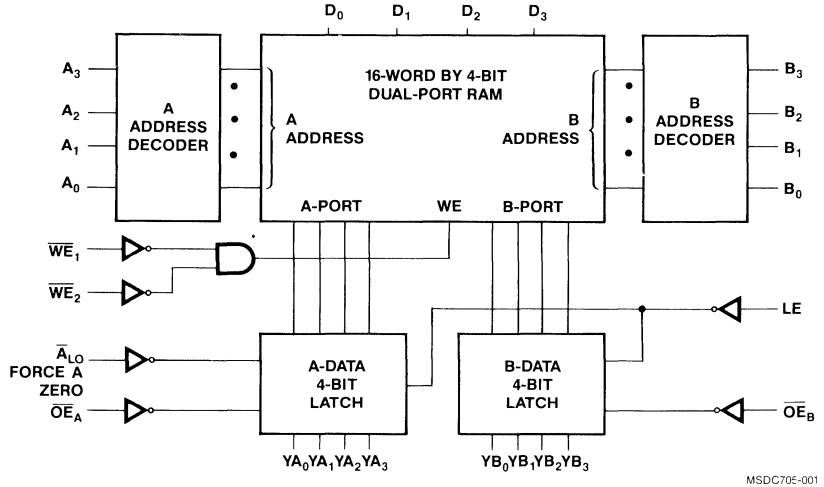
Three-state outputs allow several devices to be easily cascaded for increased memory size. When $\overline{OE}_A$ input is HIGH, the A output port is in the high impedance mode. The same respective operation occurs for the $\overline{OE}_B$ input.

The IDT39C707s function identically to the IDT39C705s, except each output port has a separate Latch Enable (LE) input. Also, an extra Write Enable ($\overline{WE}$) may be connected directly to the IEN of the IDT39C203/A for improved cycle times when compared to the IDT39C705s. The $\overline{WE}$/BLE input can then be connected directly to the system clock.

These performance-enhanced, pin-compatible replacements for all respective versions of the 29705s and 29707s are fabricated using IDTs high-speed, high-reliability CEMOS technology. Military product is 100% screened to MIL-STD-883, Class B, making them ideally suited to military temperature applications.

3

FUNCTIONAL BLOCK DIAGRAM
IDT39C705A/B



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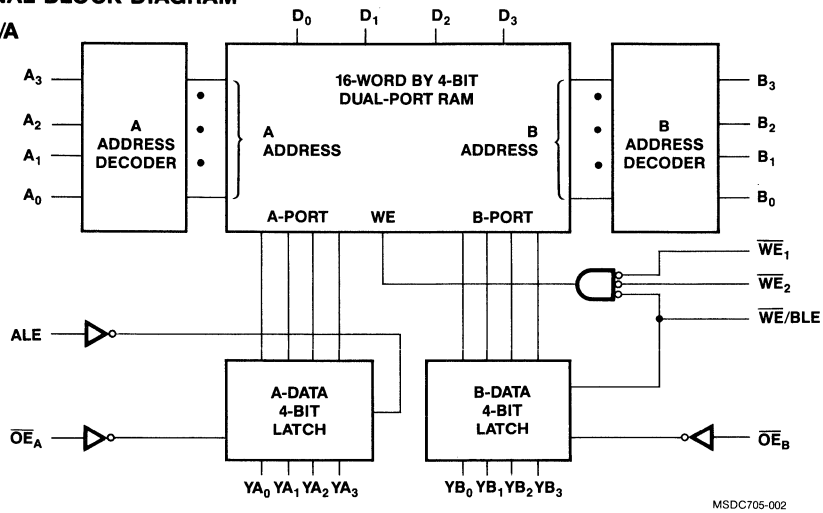
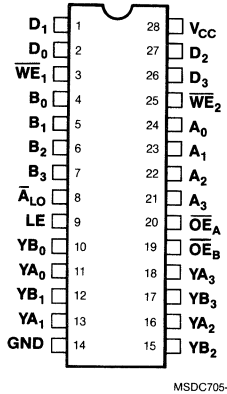
FUNCTIONAL BLOCK DIAGRAM

IDT39C707/A



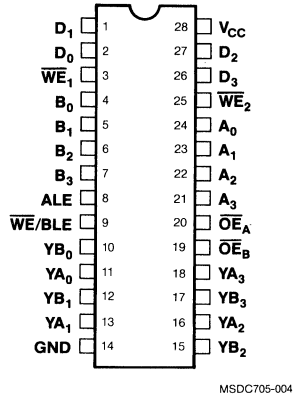
PIN CONFIGURATIONS

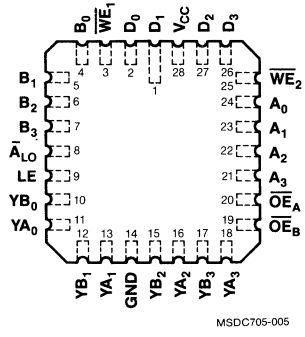
IDT39C705A/B



DIP
TOP VIEW

IDT39C707/A





LCC
TOP VIEW