Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT39C821-26

FEATURES:

- Equivalent to AMD's Am29821-26 Bipolar Registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel registers with positive edge-triggered D-type flip-flops
  —Non-inverting CP-Y t_{PD} = 7.5ns typ.
  —Inverting CP-Y t_{PD} = 7.5ns typ.
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on clock INPUT
- Clamp diodes on all inputs for ringing suppression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
  —6pF inputs (typ.)
  —8pF outputs (typ.)
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's Bipolar Am29800 series (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available.

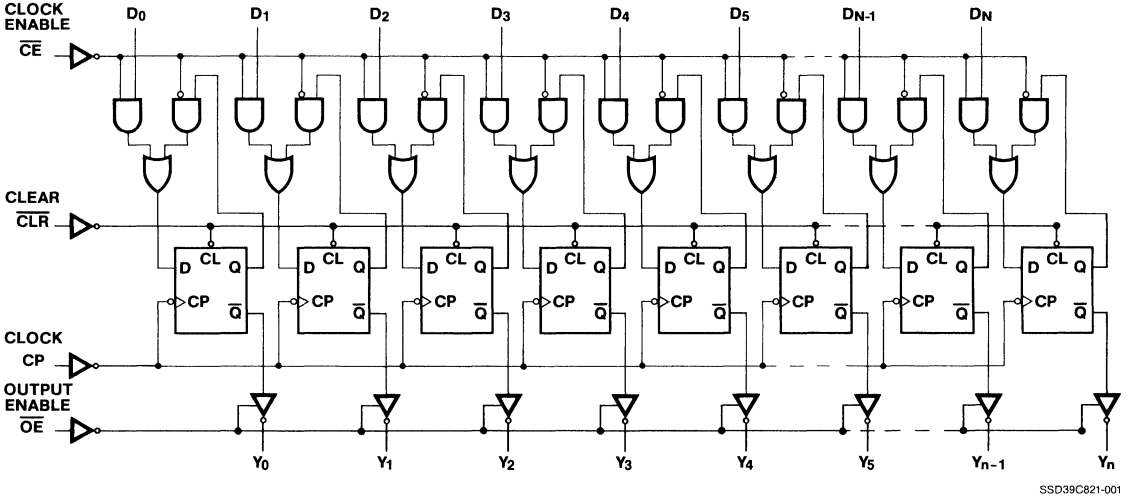
DESCRIPTION:

The IDT39C800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT39C820 Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT39C821 and IDT39C822 are buffered, 10-bit wide versions of the popular '374/'534 functions. The IDT39C823 and IDT39C824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT39C825 and IDT39C826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

cAll of the IDT39C800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



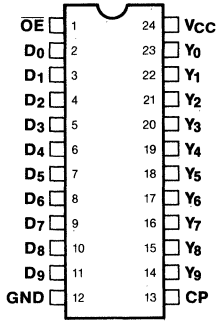
SSD39C821-001

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

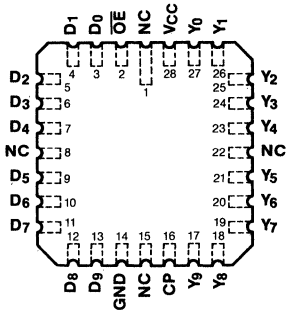
LOGIC SYMBOLS

IDT39C821/IDT39C822 10-BIT REGISTERS



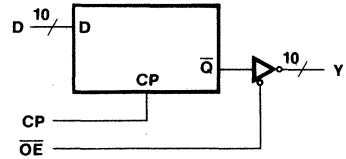
DIP
TOP VIEW

SSD39C821-005



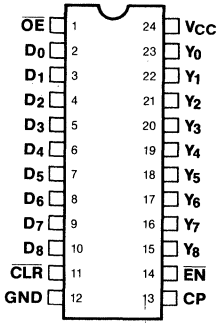
LCC
TOP VIEW

SSD39C821-006



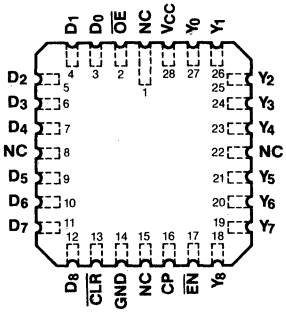
SSD39C821-002

IDT39C823/IDT39C824 9-BIT REGISTERS



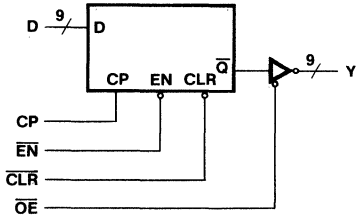
DIP
TOP VIEW

SSD39C821-007



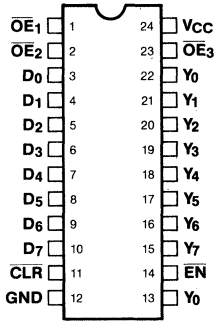
LCC
TOP VIEW

SSD39C821-008



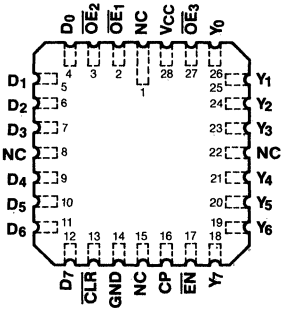
SSD39C821-003

IDT39C825/IDT39C826 8-BIT REGISTERS



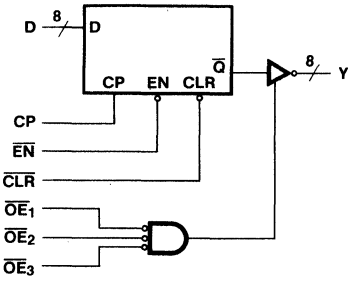
DIP
TOP VIEW

SSD39C821-009



LCC
TOP VIEW

SSD39C821-010



SSD39C821-004

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D_i	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and noninverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_i outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_i, $\overline{Y}_i$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

PRODUCT SELECTOR GUIDE

	DEVICE		
	10-BIT	9-BIT	8-BIT
Noninverting	IDT39C821	IDT39C823	IDT39C825
Inverting	IDT39C822	IDT39C824	IDT39C826

FUNCTION TABLES

IDT39C821/23/25

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	Y_i	
H	X	L	L	↑	L	Z	Hi-Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

IDT39C822/24/26

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	$\overline{Y}_i$	
H	X	L	L	↑	H	Z	Hi-Z
H	X	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

5

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)

T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA MIL.	2.4	4.0	—	
			I_{OH} = -24mA COM.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM.	—	—	0.5	
V_H	Input Hysteresis on Clock Only	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETERS	DESCRIPTION		TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50pF R_L = 500Ω	—	12	—	12	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	20	—	20	ns
t_S	Data to CP Setup Time		C_L = 50pF R_L = 500Ω	4		4		ns
t_H	Data to CP Hold Time			2		2		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time			4		4		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time			4		4		ns
t_H	Enable ($\overline{EN}$) Hold Time			2		2		ns
t_{PHL}	Propagation Delay, Clear to Y_i				20		20	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time			7		7		ns
t_{PWH}	Clock Pulse Width	HIGH		7		7		ns
t_{PWL}		LOW		7		7		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			7		7		ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ ↓ to Y_i		C_L = 300pF R_L = 500Ω		23		25	ns
t_{ZH} t_{ZL}			C_L = 50pF R_L = 500Ω		14		15	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i		C_L = 50pF R_L = 500Ω		16		18	ns
t_{HZ}[2] t_{LZ}			C_L = 5pF R_L = 500Ω		9		10	ns

NOTE:
1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.