Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT39C841-46

FEATURES:

- Equivalent to AMD's Am29841-46 Bipolar Registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel latches
  —Noninverting transparent t_{PD} = 5.5ns typ.
  —Inverting transparent t_{PD} = 6.0ns typ.
- Buffered common latch enable, clear and preset input
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on latch enable input
- Clamp diodes on all inputs for ringing supression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
  —6pF inputs (typ.)
  —8pF outputs (typ.)
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's Bipolar Am29800 Series (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available

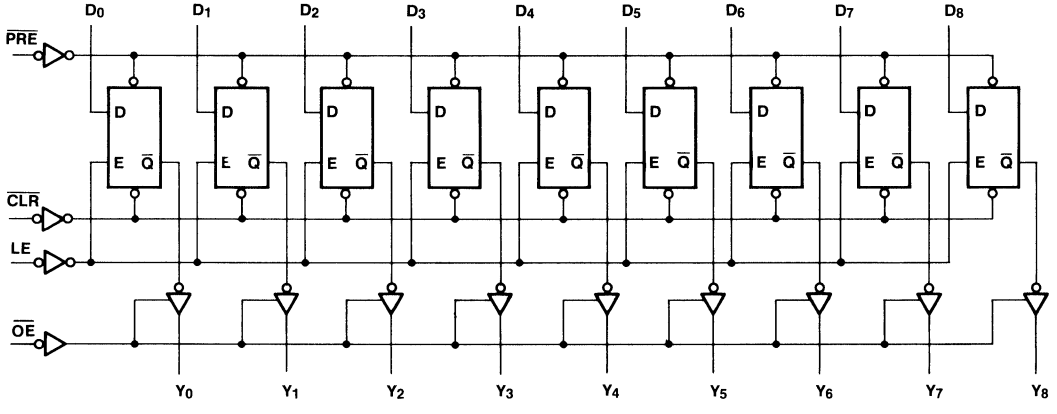
DESCRIPTION:

The IDT39C800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT39C840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT39C841 and IDT39C842 are buffered, 10-bit wide versions of the popular '373 function. The IDT39C843 and IDT39C844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance systems. The IDT39C845 and IDT39C846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT39C800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



DSR39C841-001

PRODUCT SELECTOR GUIDE

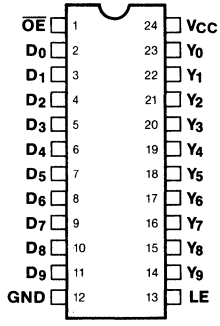
	DEVICE		
	10-BIT	**9-BIT**	**8-BIT**
Noninverting	IDT39C841	IDT39C843	IDT39C845
Inverting	IDT39C842	IDT39C844	IDT39C846

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

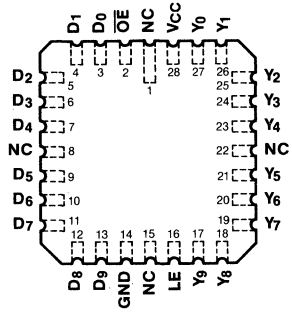
LOGIC SYMBOLS

IDT39C841/IDT39C842 10-BIT LATCHES



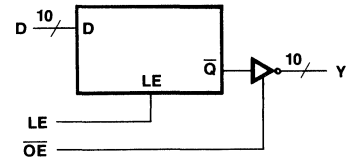
DIP
TOP VIEW

DSR39C841-005



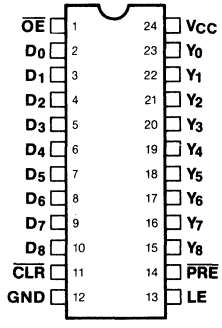
LCC
TOP VIEW

DSR39C841-006



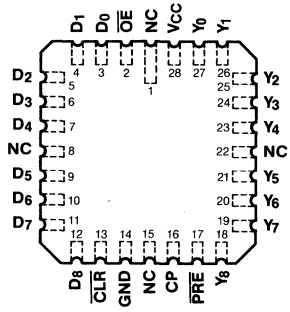
DSR39C841-002

IDT39C843/IDT39C844 9-BIT LATCHES



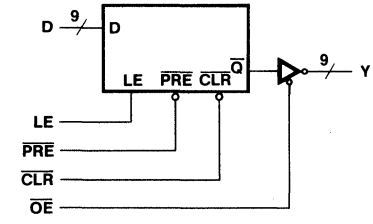
DIP
TOP VIEW

DSR39C841-007



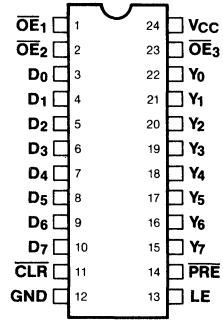
LCC
TOP VIEW

DSR39C841-008



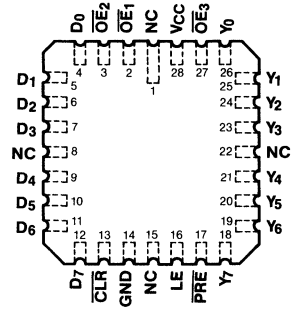
DSR39C841-003

IDT39C845/IDT39C846 8-BIT LATCHES



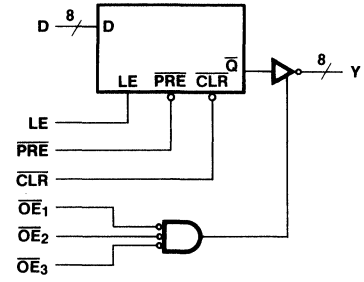
DIP
TOP VIEW

DSR39C841-009



LCC
TOP VIEW

DSR39C841-010



DSR39C841-004

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT39C841/43/45 (Non-inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_i	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_i	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.
IDT39C842/44/46 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_i	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_i	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES

IDT39C841/43/45

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	L	Z	Hi-Z
H	H	H	H	H	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

IDT39C842/44/46

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS *may cause permanent damage to the device.* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)

T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA	2.4	4.0	—	
			I_{OH} = -24mA COM'L.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM'L.	—	—	0.5	
V_H	Input Hysteresis on LE	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETERS	DESCRIPTION		TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} (IDT39C841, 43, 45) t_{PHL}	Data (D_i) to Output (Y_i) (LE = HIGH)		C_L = 50pF R_L = 500Ω	—	9.5	—	11	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	13	—	15	ns
t_S	Data to LE Setup Time		C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time			2.5	—	3	—	ns
t_{PLH} (IDT39C842, 44, 46) t_{PHL}	Data (D_i) to Output (Y_i) (LE = HIGH)		C_L = 50pF R_L = 500Ω	—	10	—	12	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	13	—	15	ns
t_S	Data to LE Setup Time		C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time			2.5	—	3	—	ns
t_{PLH} t_{PHL}	Latch Enable (LE) to Y_i		C_L = 50pF R_L = 500Ω	—	12	—	16	ns
t_{PLH} t_{PHL}			C_L = 300 pF R_L = 500Ω	—	16	—	20	ns
t_{PLH}	Propagation Delay, Preset to Y_i		C_L = 50pF R_L = 500Ω	—	12	—	14	ns
t_S	Preset Recovery ($\overline{PRE}$ ⎍) Time			—	14	—	17	ns
t_{PHL}	Propagation Delay, Clear to Y_i			—	13	—	15	ns
t_S	Clear Recovery ($\overline{CLR}$ ⎍) Time			—	14	—	17	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50pF R_L = 500Ω	6	—	6	—	ns
t_{PWL}	Preset Pulse Width	LOW		8	—	9	—	ns
t_{PWL}	Clear Pulse Width	LOW		8	—	9	—	ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ ⎍ to Y_i		C_L = 300pF R_L = 500Ω	—	23	—	25	ns
t_{ZH} t_{ZL}			C_L = 50pF R_L = 500Ω	—	14	—	15	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ ⎍ to Y_i		C_L = 50pF R_L = 500Ω	—	12	—	12	ns
t_{HZ}[2] t_{LZ}			C_L = 5pF R_L = 500Ω	—	9	—	10	ns

NOTE:
1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.