



Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS MICROCYCLE LENGTH CONTROLLER

ADVANCE INFORMATION IDT49C25

MICROSLICE™ PRODUCT

FEATURES:

- Similar function to AMD's Am2925 bipolar controller with improved speeds and output drive over full temperature and voltage supply extremes
- Four microcode-controlled clock outputs allow clock cycle length control for 15 to 30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- System controls for $\overline{\text{RUN}}/\overline{\text{HALT}}$ and Single Step — Switch-debounced inputs provide flexible halt controls
- Low input/output capacitance — 6pF inputs (typ.) — 8pF outputs (typ.)
- CMOS power levels
- Available in 300 mil 24-pin THINDIP package
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's bipolar Am2900 series (5 μ A max.)
- 100% product assurance screening to MIL-STD-883, Class B is available

DESCRIPTION:

The IDT49C25 is a single-chip general purpose clock generator/driver built using advanced CEMOS™, a dual metal CMOS technology. It has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meets a variety of system speed requirements.

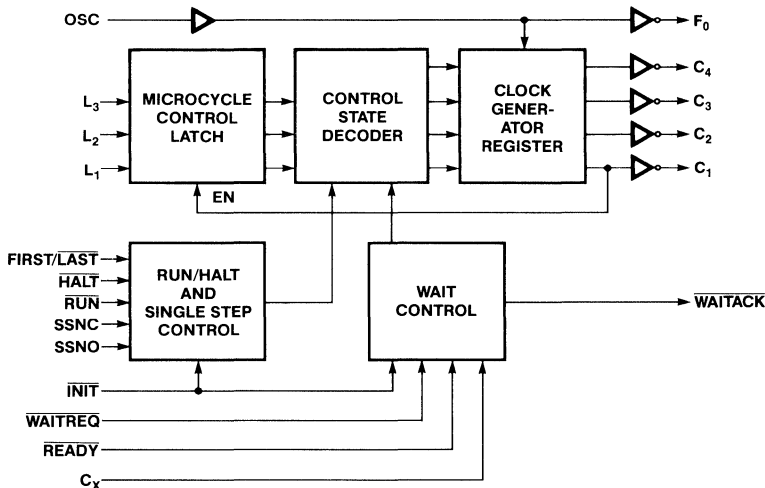
The IDT49C25 generates four different simultaneous clock output waveforms tailored to meet the needs of the IDT39C000 CMOS family and other MOS and bipolar microprocessor-based systems. One-of-eight cycle lengths may be generated under microprogram control using the Cycle Length inputs L_1 , L_2 and L_3 .

A buffered oscillator output, F_0 , is provided for external system timing in addition to the four microcode controlled clock outputs C_1 , C_2 , C_3 and C_4 .

System control functions include $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, Single-Step, Initialize and Ready/Wait controls. In addition, the FIRST/LAST input determines where a halt occurs and the C_X input determines the end point timing of wait cycles. WAITACK indicates that the IDT49C25 is in a wait state.

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FUNCTIONAL BLOCK DIAGRAM



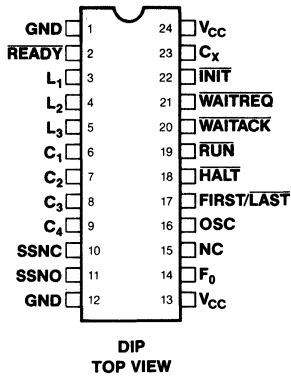
MSD49C25-001

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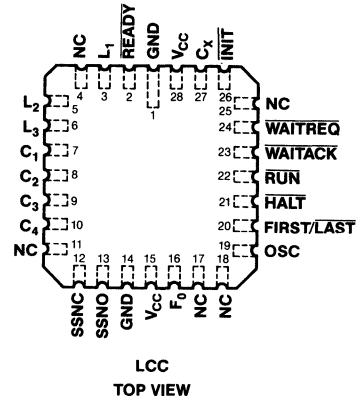
MILITARY AND COMMERCIAL TEMPERATURE RANGES

JULY 1986

PIN CONFIGURATIONS



MSD49C25-002



MSD49C25-003