Integrated Device Technology, Inc

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C401
IDT49C401A

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - —30% faster than four 2901Cs and one 2902A
- Low-power CEMOS™
  - —Military — 150mA (max.)
  - —Commercial — 125mA (max.)
- Functionally equivalent to four 2901s and on 2902
- Pin-compatible, performance-enhanced replacement for IMI4X2901B
- Independent, simultaneous access to two 16-word x 16-bit register files
- Expanded destination functions with eight new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Cascadable
- Available in a 64-pin DIP
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

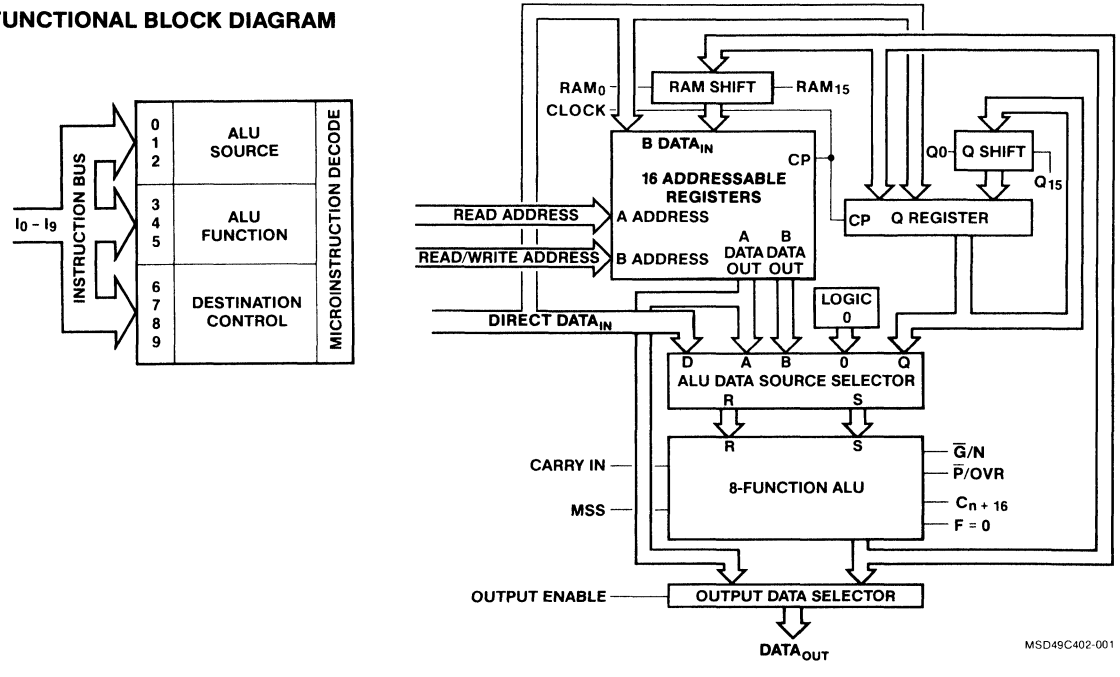
The IDT49C401s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902, with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C401s include all of the normal functions associated with standard 2901 bit-slice operation: (a) a 3-bit instruction field (I_0,I_1,I_2) which controls the source operand selection for the ALU; (b) a 3-bit microinstruction field (I_3,I_4,I_5) used to control the eight possible functions of the ALU, and; (c) sixteen destination control functions which are selected by the microcode inputs (I_6,I_7,I_8,I_9). Eight of the sixteen destination control functions reflect the standard 2901 operation, while the other eight additional destination control functions allow for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and new combinations of destination functions with the RAM A-port output available at the Y output pins of the device. Also featured is an on-chip dual-port RAM that contains 16 words by 16 bits.

The IDT49C401s are fabricated using CEMOS, a single poly, double metal CMOS technology designed for high-performance and high-reliability. These performance enhanced devices feature both bipolar speed and bipolar output drive capabilities while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

3

FUNCTIONAL BLOCK DIAGRAM



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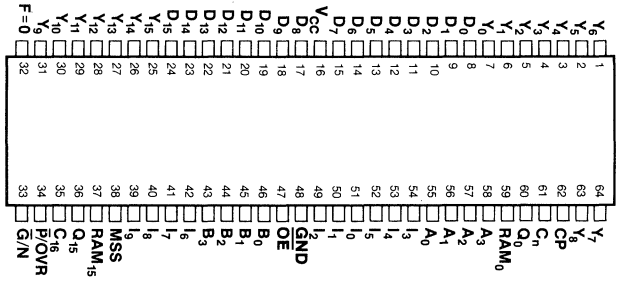
PIN CONFIGURATION



DIP
TOP VIEW

DEVICE ARCHITECTURE

The IDT49C401 CMOS Bit-Slice Microprocessors are configured sixteen bits wide and are cascadable to any number of bits (16, 32, 48, 64). Key elements which make up these sixteen-bit slice microprocessors are the (1) register file (16 x 16 dual-port RAM) with shifter, (2) ALU, and (3) Q Register and shifter.

REGISTER FILE—A 16-bit data word from one of the 16 RAM registers can be read from the A-port as selected by the 4-bit A address field. Simultaneously, the same data word or any other word from the 16 RAM registers can be read from the B-port as selected by the 4-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A-port and B-port data during the clock (CP) LOW time, eliminating any data races. During clock HIGH these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involve the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output while the RAM_{15} I/O input is selected as the input to the MSB.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the $I_{(0,1,2)}$ inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3,4,5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}$/OVR are aimed at accelerating arithmetic operations. For intermediate and least-significant slices, the MSS pin is programmed LOW selecting the carry-generate ($\overline{G}$) and carry-propagate ($\overline{P}$) output functions to be used by carry-lookahead logic. For the most-significant slice, MSS is programmed high, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign-bit (F_{15}) allows the ALU sign-bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign-bit, as logically determined from the Exclusive-OR of the carry-in and carry-out of the most-significant bit of the ALU. For all 16-bit applications, the MSS pin on the IDT49C401s is tied high or not connected since only one device is needed. With MSS open or tied high, internal circuitry will direct pins 33 and 34 to function as F_{15} and OVR, respectively. It is in this 16-bit operating mode that the IDT49C401s function identically to the IMI4X2901B. The ALU data outputs are available at the three-state outputs $Y_{(0-15)}$, or as inputs to the RAM register file and Q Register under control of the $I_{(6,7,8,9)}$ instruction inputs.

Q REGISTER—The Q Register is a separate 16-bit register intended for multiplication and division routines, and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift-up or shift-down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6,7,8,9)}$ inputs.

The clock input of the IDT49C401 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6,7,8,9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_3	I	Four address inputs to the register file which selects one register and displays its contents through the A-port.
B_0-B_3	I	Four address inputs to the register file which selects one of the registers in the file, the contents of which are displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0-I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0,1,2)}$, what function the ALU will perform $I_{(3,4,5)}$, and what data is to be deposited in the Q Register or the register file $I_{(6,7,8,9)}$. Original 2901 destinations are selected if I_9 is disconnected. In this mode, proper I_9 bias is controlled by an internal pullup resistor to V_{CC}.
D_0-D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0-Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A-port of the register stack. This is determined by the destination code $I_{(6,7,8,9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, or as F_{15}, the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F=0	O	Open drain output which goes HIGH if the F_0-F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the internal ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6,7,8,9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6,7,8,9)}$ indicates an up shift, the three-state outputs are enabled and the MSB of the Q Register is available on the Q_{15} pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry-lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64x16 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to V_{CC} provides declaration that the device is the most significant slice and will define pins as OVR and F_{15}.

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R $\vee$ S
AND	H	L	L	4	R AND S	R $\wedge$ S
NOTRS	H	L	H	5	R AND S	$\overline{R}$ $\wedge$ S
EXOR	H	H	L	6	R EX-OR S	$\overline{R \vee S}$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \vee S}$

ALU ARITHMETIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$ $I_{2,1,0}$	C_n = L		C_n = H	
	GROUP	FUNCTION	GROUP	FUNCTION
0 0	ADD	A + Q	ADD Plus One	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

ALU LOGIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$ $I_{2,1,0}$	GROUP	FUNCTION
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \triangledown Q$
6 1		$A \triangledown B$
6 5		$D \triangledown A$
6 6		$D \triangledown Q$
7 0	EX-NOR	$\overline{A \triangledown Q}$
7 1		$\overline{A \triangledown B}$
7 5		$\overline{D \triangledown A}$
7 6		$\overline{D \triangledown Q}$
7 2	INVERT	Q
7 3		B
7 4		A
7 7		D
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL 0	1	2	3	4	5	6	7
		ALU SOURCE							
		A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0	C_n = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S Minus R	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D - 1	Q - D - 1	-D - 1
	C_n = H	Q - A	B - A	Q	B	A	A - D	Q - D	-D
2	C_n = L R Minus S	A - Q - 1	A - B - 1	-Q - 1	-B - 1	-A - 1	D - A - 1	D - Q - 1	D - 1
	C_n = H	A - Q	A - B	-Q	-B	-A	D - A	D - Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ▽ Q	A ▽ B	Q	B	A	D ▽ A	D ▽ Q	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; - = Minus; ∧ = AND; ▽ = EX-OR; ∨ = OR

ALU DESTINATION CONTROL

MNE-MONIC	MICROCODE I_9	I_8	I_7	I_6	HEX CODE	RAM FUNCTION SHIFT	RAM FUNCTION LOAD	Q REGISTER FUNCTION SHIFT	Q REGISTER FUNCTION LOAD	Y OUTPUT	RAM SHIFTER RAM_0	RAM SHIFTER RAM_{15}	Q SHIFTER Q_0	Q SHIFTER Q_{15}	
OREG	H	L	L	L	8	X	NONE	NONE	F → Q	F	X	X	X	X	
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	
RAMA	H	L	H	L	A	NONE	F → B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F → B	X	NONE	F	X	X	X	X	Existing 2901 Functions
RAMQD	H	H	L	L	C	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}	
RAMD	H	H	L	H	D	DOWN	F/2 → B	X	NONE	F	F_0	IN_{15}	Q_0	X	
RAMQU	H	H	H	L	E	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}	
RAMU	H	H	H	H	F	UP	2F → B	X	NONE	F	IN_0	F_{15}	X	Q_{15}	
DFF	L	L	L	L	0	NONE	D→B	NONE	F→Q	F	X	X	X	X	
DFA	L	L	L	H	1	NONE	D→B	NONE	F→Q	A	X	X	X	X	
FDF	L	L	H	L	2	NONE	F→B	NONE	D→Q	F	X	X	X	X	
FDA	L	L	H	H	3	NONE	F→B	NONE	D→Q	A	X	X	X	X	New Added IDT49C401 Functions
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2→Q	F	X	X	Q_0	IN_{15}	
DXF	L	H	L	H	5	NONE	D→B	X	NONE	F	X	X	Q_0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q→Q	F	X	X	IN_0	Q_{15}	
XDF	L	H	H	H	7	X	NONE	NONE	D→Q	F	X	X	X	Q_{15}	

X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB; DOWN is toward LSB.

3

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	1.0	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-1.0	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	—	0.3	0.5	
			I_{OL} = 24mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	—	-40	µA
			V_O = V_{CC}	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		-30	—	-135	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H		—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L		—	—	—	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	—	70	150	
			COM'L.	—	70	125	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock Input frequency.

IDT49C401A AC ELECTRICAL CHARACTERISTICS

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C401A over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

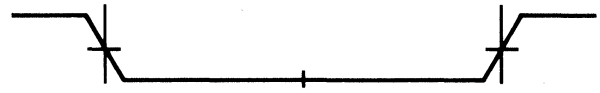
CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	28	24	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=C32 or E32)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	36	31	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) G, P		(MSS = H) F_{15}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	—	—	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	—	—	ns
C_n	29	26	—	—	26	24	25	23	20	18	29	26	23	21	—	—	ns
$I_{0,1,2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	—	—	ns
$I_{3,4,5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	—	—	ns
$I_{6,7,8,9}$	25	23	—	—	—	—	—	—	—	—	—	—	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock —	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	11	10	0[3]	0[3]	24[4]	21[4]	0	0	ns
B Destination Address	11	10	Do not change[2]				0	0	ns
D	—[1]	—	—	—	12/22[5]	10/20[5]	0	0	ns
C_n	—	—	—	—	17	15	0	0	ns
$I_{0,1,2}$	—	—	—	—	28	25	0	0	ns
$I_{3,4,5}$	—	—	—	—	28	25	0	0	ns
$I_{6,7,8,9}$	11	10	Do not change[2]				0	0	ns
$RAM_{0,15}$,$Q_{0,15}$	—	—	—	—	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).

IDT49C401 AC ELECTRICAL CHARACTERISTICS

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C401 over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

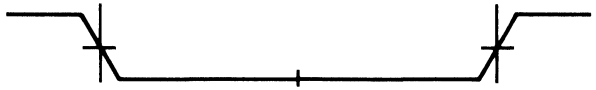
	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) G, P		(MSS = H) F_{i5}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	—	—	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	—	—	ns
C_n	29	26	—	—	29	26	27	25	20	18	29	26	23	21	—	—	ns
$I_{0,1,2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	—	—	ns
$I_{3,4,5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	—	—	ns
$I_{6,7,8,9}$	26	24	—	—	—	—	—	—	—	—	—	—	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock —	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:



INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	20	18	0[3]	0[3]	50[4]	48[4]	0	0	ns
B Destination Address	20	18	Do not change[2]				0	0	ns
D	—[1]	—	—	—	30/40[5]	26/36[5]	0	0	ns
C_n	—	—	—	—	35	32	0	0	ns
$I_{0,1,2}$	—	—	—	—	45	41	0	0	ns
$I_{3,4,5}$	—	—	—	—	45	41	0	0	ns
$I_{6,7,8,9}$	12	11	Do not change[2]				0	0	ns
$RAM_{0,15}, Q_{0,15}$	—	—	—	—	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q REGISTER). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q REGISTER).

3

IDT49C401
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	25	23	25	23

IDT49C401A
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	22	20	20	18

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Fig. 1

TEST LOAD CIRCUITS

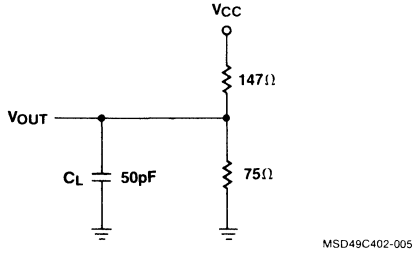


Figure 1. Switching Test Circuit (all outputs)

INPUT/OUTPUT INTERFACE CIRCUITRY

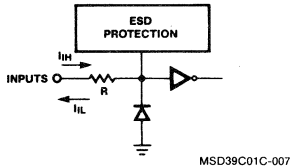


Figure 2. Input Structure (All Inputs)

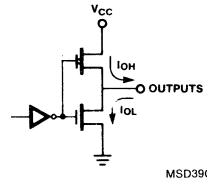


Figure 3. Output Structure (All Outputs Except F = 0)

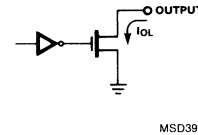


Figure 4. Output Structure (F = Only)