Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTER WITH SPC™
(Serial Protocol Channel)

ADVANCE INFORMATION
IDT49C818

FEATURES:

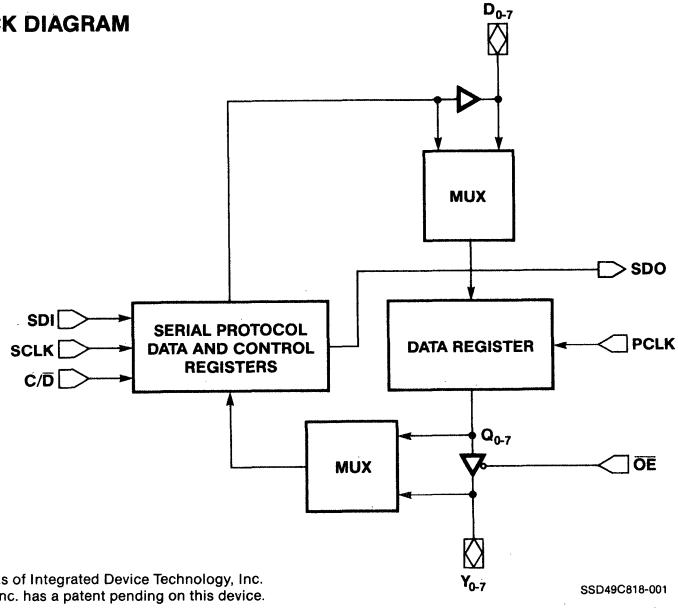
- High-speed non-inverting 8-bit parallel register for any data path, control path or pipelining application
- Pin-out similar to the Am29818 and 54/74S818, but uses an improved protocol for the serial interface
- New, unique command capability which allows for multiplicity of diagnostic functions
- High-speed Serial Protocol Channel (SPC) which provides access to octal data register using four pins
- Controllability
  - —Serial scan of new machine state
  - —Form temporary connections between D and Y buses
  - —Load new machine state "on the fly" synchronous with PCLK
  - —Temporarily force Y output bus
  - —Temporarily force data out the D input bus (as in loading Writeable Control Store — WCS)
- Observability
  - —Directly observe D and Y buses
  - —Serial scan out current machine state
  - —Capture machine state "on the fly" synchronous with PCLK
  - —WCS pipeline register
  - —Load WCS from serial input
  - —Read WCS via serial scan
- Ideal for diagnostic scan testing

DESCRIPTION:

The IDT49C818 is a high-speed, general-purpose octal register with a Serial Protocol Channel (SPC). The D-to-Y path of the octal register provides a data path that is designed for normal system operation wherever a high-speed clocked register is required. The IDT49C818 is pin-out similar to the 29818 and 54/74S818, but uses the serial data, clock and mode pins as SPC to communicate with the serial command and data registers.

The command and data registers are used to observe and control the operation of the octal data registers. The serial command and data registers can be accessed while the system is performing normal system function. Diagnostic operations then can be performed "on the fly", synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in (SDI) and data out (SDO) pins which can participate in a serial scan loop throughout the system where normal data, address, status and control registers are replaced with the IDT49C818. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results. An "oscilloscope mode" can be achieved by loading data from the SPC serial data register into the octal data register synchronous to the system clock (PCLK) using a diagnostic command which transfers data synchronously. When repeated every Nth clock, the repeating states of the system can be observed on an oscilloscope. When used as a pipeline register, WCS loading can be accomplished by scanning in data through the SPC port and enabling the data onto the D bus pins.

FUNCTIONAL BLOCK DIAGRAM

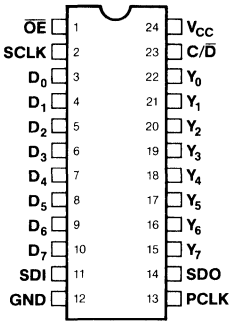


SSD49C818-001

CEMOS and SPC are trademarks of Integrated Device Technology, Inc.
Integrated Device Technology, Inc. has a patent pending on this device.

Printed in U.S.A.

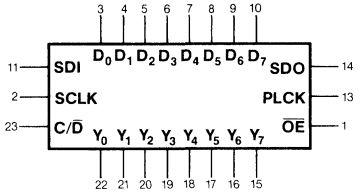
PIN CONFIGURATION



DIP
TOP VIEW

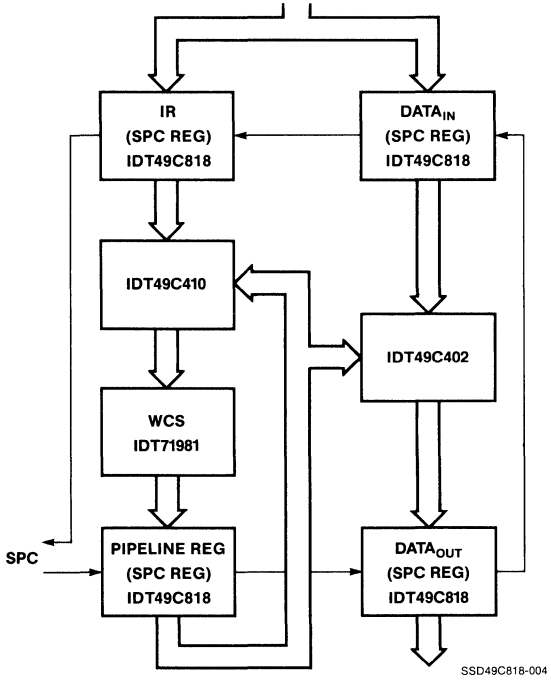
SSD49C818-002

LOGIC SYMBOL



SSD49C818-003

TYPICAL MICROPROGRAM APPLICATION



SSD49C818-004

5