HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH

IDT54/74AHCT373

Integrated Device Technology, Inc.

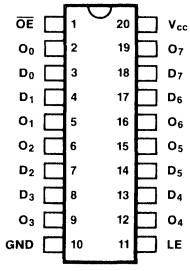
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal transparent latch with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

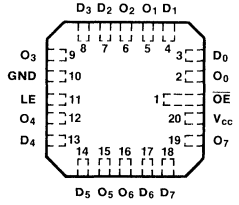
The IDT54/74AHCT373 are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. This octal latch has 3-state output and is intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSD54/74AHCT373-001

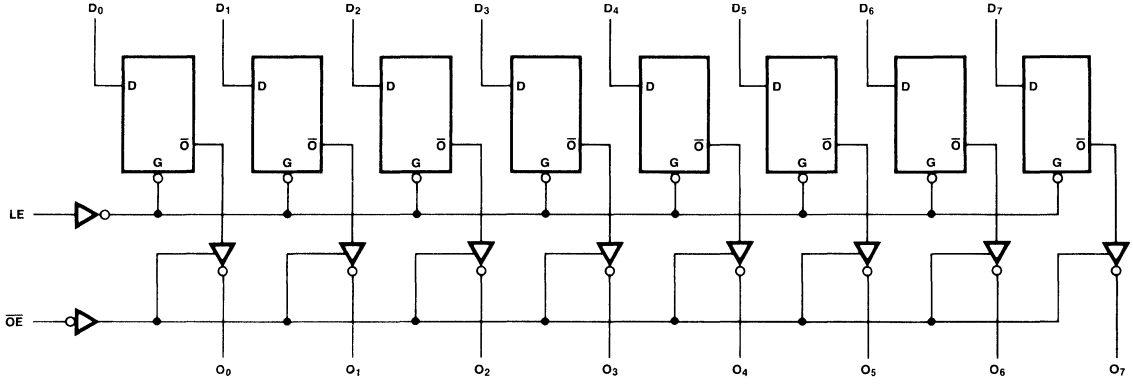
DIP
TOP VIEW



SSD54/74AHCT373-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT373-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250kHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{LE}$	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
O_0-O_7	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50 pf R_L = 500Ω	10.0	2.0	16.0	2.0	19.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	20.0	5.0	24.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	2.0	12.0	2.0	16.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		20.0	6.0	23.0	6.0	27.0	ns
t_S	Set-up Time HIGH or LOW D_N to LE		4.0	10.0	—	10.0	—	ns
t_H	Hold Time HIGH or LOW D_N to LE		3.0	7.0	—	7.0	—	ns
t_W	LE Pulse Width HIGH or LOW		7.0	10.0	—	10.0	—	ns