



Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH (3-STATE)

IDT54/74AHCT533

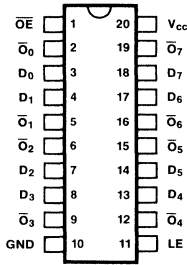
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 11ns typical clock to output
- $I_{OL} = 14\text{mA}$ over full military temperature range
- CMOS power levels ($5\mu\text{W}$ typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS ($5\mu\text{A}$ max.)
- Octal transparent latch with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

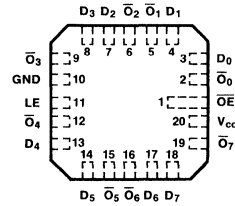
The IDT54/74AHCT533 are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AHCT533 consist of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\bar{O}E$) is LOW. When $\bar{O}E$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSD54/74FCT533-001

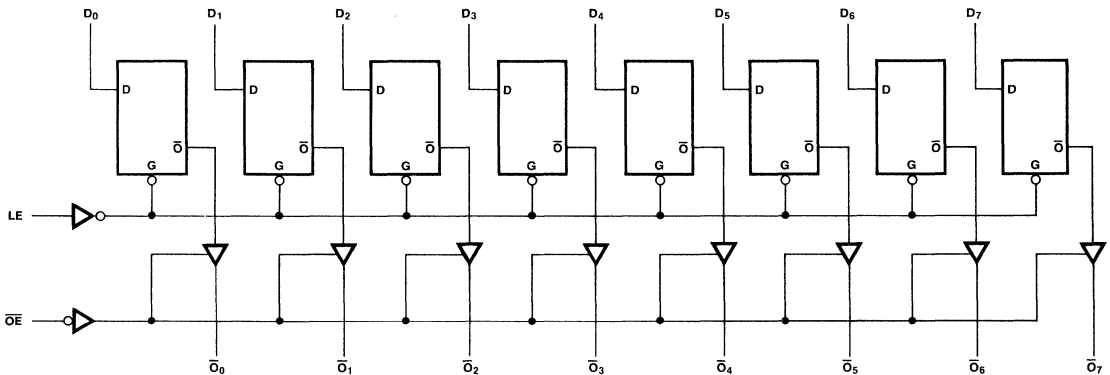
DIP
TOP VIEW



SSD54/74FCT533-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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SSDAHCT533-003

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING⁽¹⁾

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I _{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
 T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
 V_{LC} = 0.2V
 V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN.	TYP. ⁽²⁾	MAX.	UNIT	
V _{IH}	Input HIGH Level	Guaranteed Logic High Level	2.0	—	—	V	
V _{IL}	Input LOW Level	Guaranteed Logic Low Level	—	—	0.8	V	
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}	—	—	5	μA	
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND	—	—	-5	μA	
I _{SC}	Short Circuit Current	V _{CC} = Max. ⁽³⁾	-60	-100	—	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OH} = -32μA	V _{HC}	V _{CC}	—	V	
		V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -150μA	V _{HC}	V _{CC}		—
			I _{OH} = -1.0mA MIL	2.4	4.3		—
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OL} = 300μA	—	GND	V _{LC}	V	
		V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 300μA	—	GND		V _{LC}
			I _{OL} = 14mA MIL	—	—		0.4
			I _{OL} = 24mA COM	—	—		0.5

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.



POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS ⁽¹⁾		MIN.	TYP. ⁽²⁾	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V$ ⁽³⁾		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	$V_{CC} = \text{Max.}$ Outputs Open OE = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 1.0\text{MHz}$ 50% Duty Cycle OE = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	—	0.4	2.6	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 250\text{KHz}$ 50% Duty Cycle OE = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient and maximum loading.

3. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

4. $I_{CC} = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$

$I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$

I_{CCQ} = Quiescent Current

I_{CCT} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	Output Enable Input (Active LOW)
$\overline{O_0}$ - $\overline{O_7}$	Complementary 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D _N	LE	\overline{OE}	$\overline{O_N}$
H	H	L	L
L	H	L	H
X	X	H	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t _{PLH} t _{PHL}	Propagation Delay D _N to $\overline{O_N}$	C _L = 50pf R _L = 500Ω	11.0	4.0	19.0	4.0	24.0	ns
t _{ZH} t _{ZL}	Output Enable Time		15.0	4.0	18.0	4.0	20.0	ns
t _{HZ} t _{LZ}	Output Disable Time		11.0	2.0	16.0	2.0	22.0	ns
t _{PLH} t _{PHL}	Propagation Delay LE to $\overline{O_N}$		15.0	4.0	23.0	4.0	28.0	ns
t _S	Set Up Time HIGH or LOW D _N to LE		7.0	15.0	—	15.0	—	ns
t _H	Hold Time HIGH or LOW D _N to LE		5.0	7.0	—	7.0	—	ns
t _w	LE Pulse Width HIGH or LOW		7.0	15.0	—	15.0	—	ns

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