



FAST CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521/A/B/C

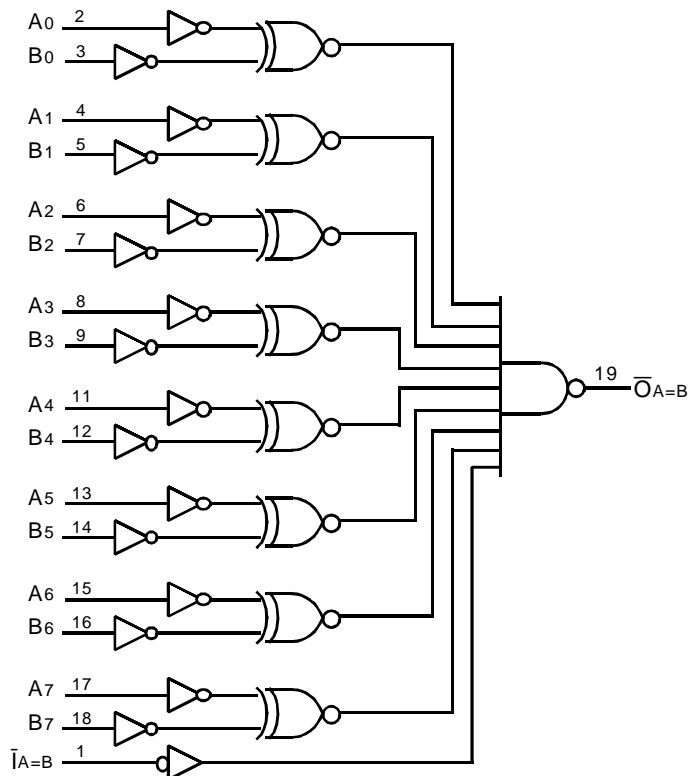
FEATURES:

- IDT54/74FCT521 equivalent to FAST™ speed
- IDT54/74FCT521A 35% faster than FAST
- IDT54/74FCT521B 50% faster than FAST
- IDT54/74FCT521C 60% faster than FAST
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B
- Available in the following packages:
 - Commercial: SOIC
 - Military: CERDIP, LCC, CERPACK

DESCRIPTION:

The FCT521 is an 8-bit identity comparator built using an advanced dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a low output when the two words match bit for bit. The expansion input $\bar{I}_{A=B}$ also serves as an active low enable input.

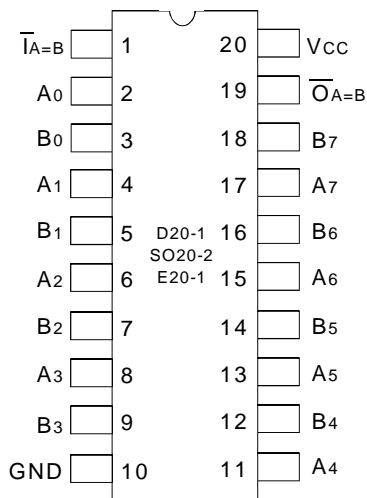
FUNCTIONAL BLOCK DIAGRAM



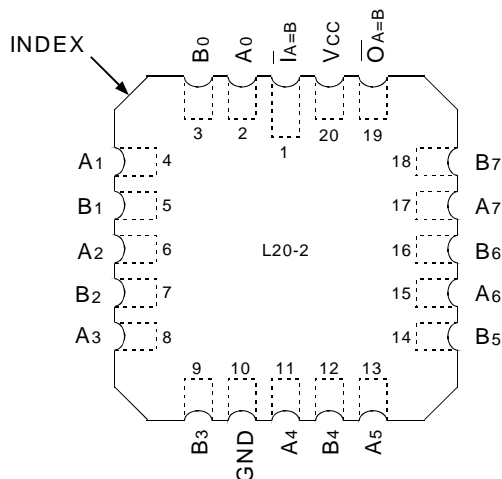
MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 2000

PIN CONFIGURATION



CERDIP/ SOIC/ CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7	-0.5 to +7	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

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NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$A_0 - A_7$	Word A Inputs
$B_0 - B_7$	Word B Inputs
$\bar{I}_A = B$	Expansion or Enable Input (Active LOW)
$\bar{O}_A = B$	Identity Output (Active LOW)

FUNCTION TABLE (1)

INPUTS		OUTPUT
$\bar{I}_A = B$	A, B	$\bar{O}_A = B$
L	$A = B^*$	L
L	$A \neq B$	H
H	$A = B^*$	H
H	$A \neq B$	H

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
* $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	5	μA
			$V_i = 2.7V$	—	—	5 ⁽⁴⁾	
I_{IL}	Input LOW Current		$V_i = 0.5V$	—	—	-5 ⁽⁴⁾	
			$V_i = GND$	—	—	-5	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	—	
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3	—	
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$		—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND	$V_{LC}^{(4)}$	
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3	0.5	
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3	0.5	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁵⁾	V _{CC} = Max. Outputs Open f _i = 10MHz One Bit Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2	5	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_iN_i)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL

Symbol	Parameter	Condition ⁽¹⁾	IDT74FCT521		IDT74FCT521A		IDT74FCT521B		IDT74FCT521C		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay A _n or B _n to $\bar{O}_A = B$	C _L = 50pF R _L = 500Ω	1.5	11	1.5	7.2	1.5	5.5	1.5	4.5	ns
t _{PLH} t _{PHL}	Propagation Delay $\bar{I}_A = B$ to $\bar{O}_A = B$		1.5	10	1.5	6	1.5	4.6	1.5	4.1	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

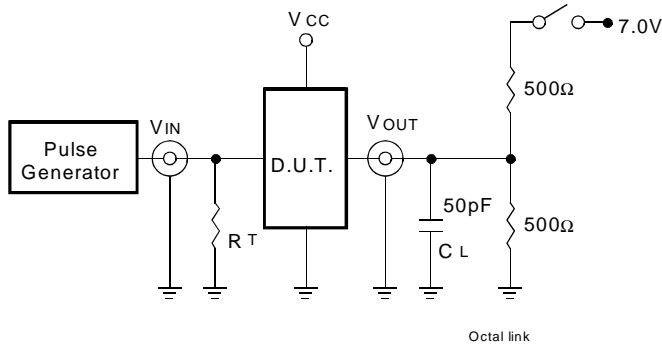
Symbol	Parameter	Condition ⁽¹⁾	IDT54FCT521		IDT54FCT521A		IDT54FCT521B		IDT54FCT521C		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay A _n or B _n to $\bar{O}_A = B$	C _L = 50pF R _L = 500Ω	1.5	15	1.5	9.5	1.5	7.3	1.5	5.1	ns
t _{PLH} t _{PHL}	Propagation Delay $\bar{I}_A = B$ to $\bar{O}_A = B$		1.5	9	1.5	7.8	1.5	6	1.5	4.5	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

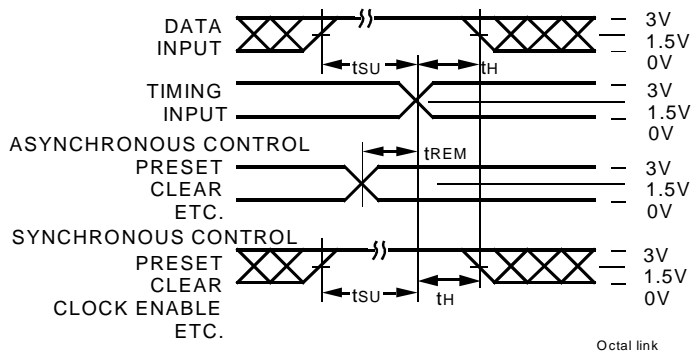
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DEFINITIONS:

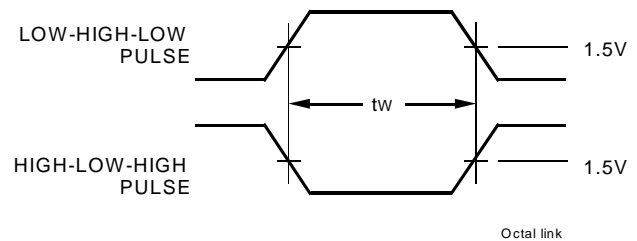
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

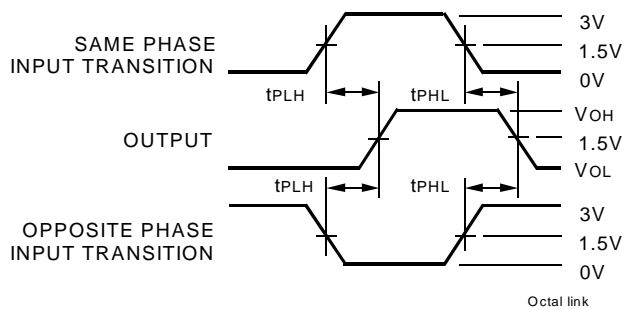
SET-UP, HOLD, AND RELEASE TIMES



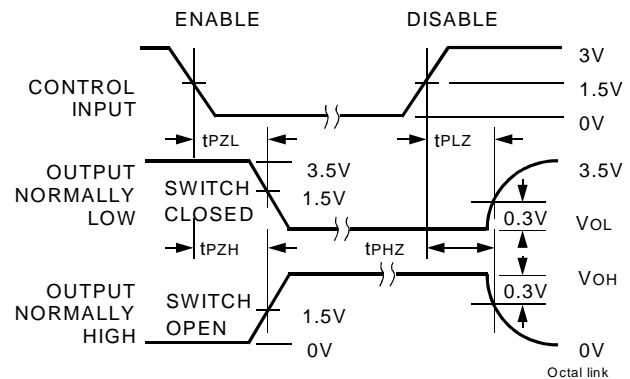
PULSE WIDTH



PROPAGATION DELAY



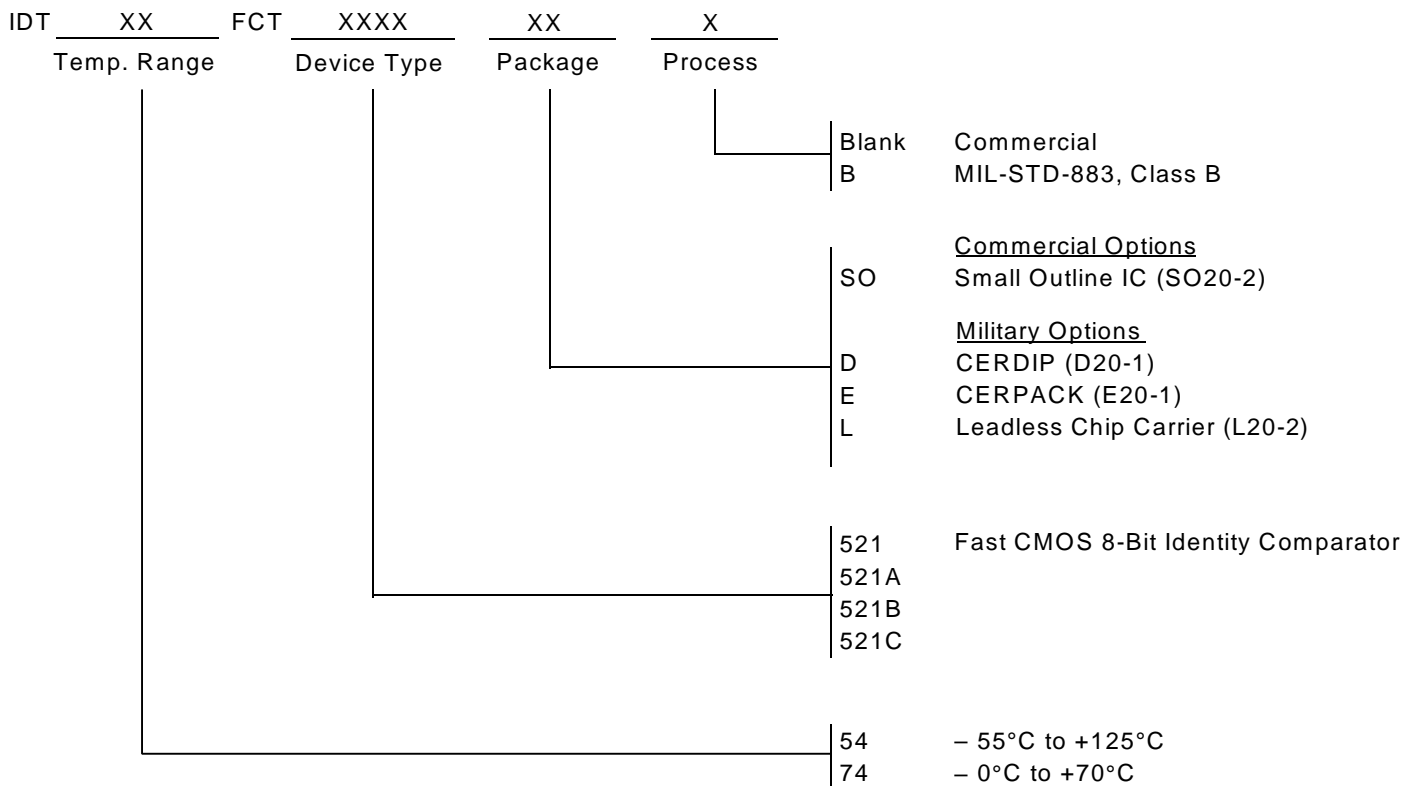
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o \leq 50\Omega$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION



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