Description

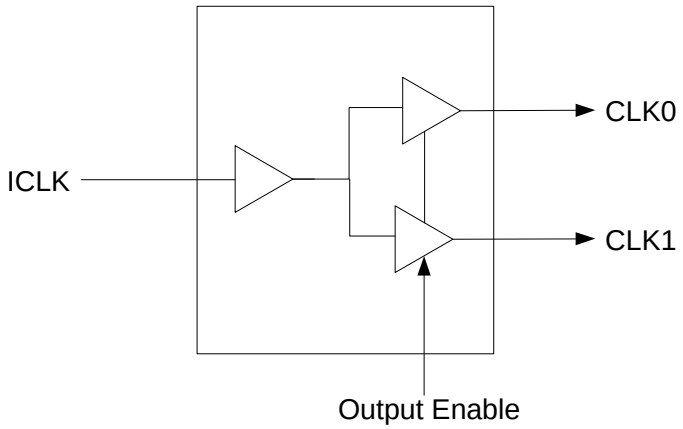
The IDT5P30017 is a low skew, single input to two output, clock buffer. The device operates from a single 1.8 to 3.3 volt supply and has a 1.8 to 3.3 volt tolerant input, making it ideal for level translation.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

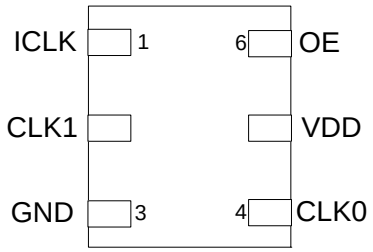
Features

- Low skew outputs (50 ps)
- Packaged in 6-pin DFN (1.4 x 1.4mm)
- RoHS (lead-free) compliant package
- Low power CMOS technology
- Operating voltages of 1.8 V to 3.3 V
- Frequency range of operation: 0 to 200MHz
- Output Enable pin tri-states outputs
- Industrial temperature range

Block Diagram



Pin Assignment (6-pin DFN)



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Clock Input. 1.8 to 3.3 V tolerant input.
2	CLK1	Output	Clock Output 1.
3	GND	Power	Connect to ground.
4	CLK0	Output	Clock Output 0.
5	VDD	Power	Connect to +1.8 V or +3.3 V.
6	OE	Input	Output Enable with 250kohm internal series resistor. Tri-states outputs when low.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD on pin 5 and GND, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the IDT5P30017 is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P30017. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	0.5 to 5.0V
Output Enable and All Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (industrial)	-40 to +85 °C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (industrial)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	1.71		3.6	V

DC Electrical Characteristics

VDD=1.8 to 3.3V ±5%, Ambient temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		3.465	V
Input High Voltage	V_{IH}	Note 1, ICLK, OE	0.65VDD		3.465	V
Input Low Voltage	V_{IL}	Note 1, ICLK, OE			0.35VDD	V
Output High Voltage	V_{OH}	I_{OH} = -2 mA	0.75VDD			V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA			0.25VDD	V
Operating Supply Current	IDD	No load, 133 MHz		TBD		mA
Nominal Output Impedance	Z_O			40		W
Input Capacitance	C_{IN}	ICLK, OE pin		5		pF
Short Circuit Current	I_{OS}			±40		mA

Notes: 1. Nominal switching threshold is VDD/2

AC Electrical Characteristics

VDD =2.5 - 3.3V, Ambient Temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	20% to 80%, Note 3		1.0	1.5	ns
Output Fall Time	t_{OF}	80% to 20%, Note 3		1.0	1.5	ns
Propagation Delay	Note 1		TBD	3	5	ns
Output to Output Skew	Note 2	Rising edges at VDD/2		0	±50	ps

Notes: 1. With rail to rail input clock

2. Between any 2 outputs with equal loading.

3. Measured with a 15 pF load.

VDD = 1.8 - 2.4V, Ambient Temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	20% to 80%, Note 3		1.0	1.5	ns
Output Fall Time	t_{OF}	80% to 20%, Note 3		1.0	1.5	ns
Propagation Delay	Note 1		TBD	3	5	ns
Output to Output Skew	Note 2	Rising edges at VDD/2		0	±50	ps

Notes: 1. With rail to rail input clock

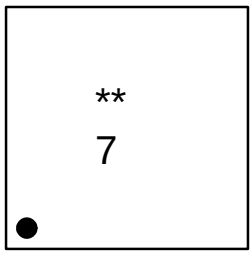
2. Between any 2 outputs with equal loading.

3. Measured with a 5 pF load.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W
Thermal Resistance Junction to Top of Case	Ψ_{JT}	Still air		20		°C/W

Marking Diagram

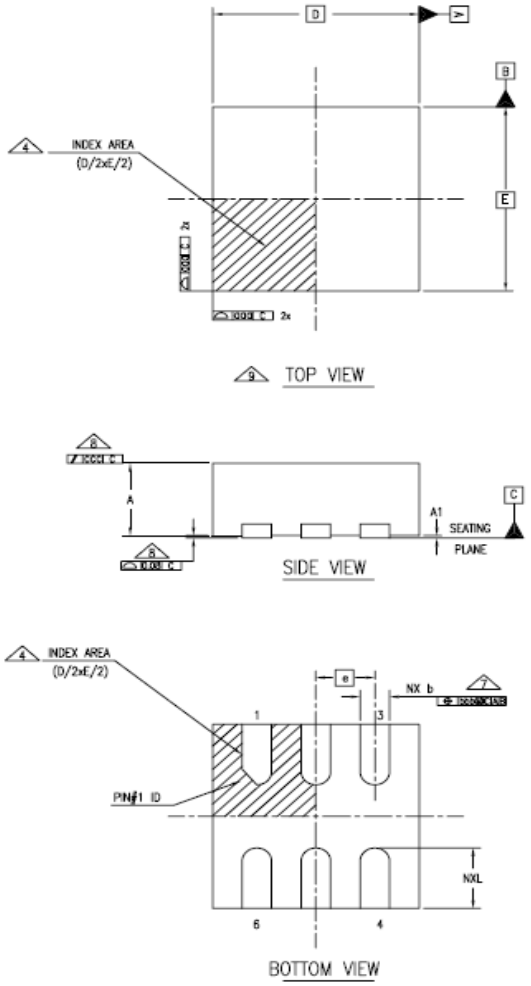


Notes:

1. “**” is the lot sequence number.
2. “7” is the truncated part number.
3. Bottom marking: country of origin.

Package Outline and Package Dimensions (6-pin DFN 1.4x1.4mm, 0.4mm pitch)

Package dimensions are kept current with JEDEC Publication No. 95,



	Millimeters	
Symbol	**Min**	**Max**
A	.51	0.6
A1	0	0.05
N	6	
D	1.40 BASIC	
E	1.40 BASIC	
e	0.40 BASIC	
b	0.15	0.25
L	0.36	0.56

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P30017NDGI	see page 5	Tray	6-pin DFN	-40 to +85°C
5P30017NDGI8		Tape and Reel	6-pin DFN	-40 to +85°C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
D	J. Chao	04/02/12	1. Corrected VDD typo of 1.14V; changed to 1.71V 2. Added "Frequency range of operation: 0 to 200MHz" in Features bullets on page 1
E	R. Willner	05/14/12	1. Updated Supply Voltage (VDD) from 1.8~3.3V to 0.5~5.0V 2. Updated "Operating Voltage" and "Input High Voltage" specs from 3.6V max to 3.465V max. 3. Removed "Case Temperature" spec from Thermal Characteristics 4. Added marking diagram
F	B. Chandhoke	12/08/14	1. Updated to latest doc template. 2. Moved from Preliminary to Final.

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