HIGH-SPEED 2.5V
256/128K x 72
SYNCHRONOUS
DUAL-PORT STATIC RAM
WITH 3.3V OR 2.5V INTERFACE

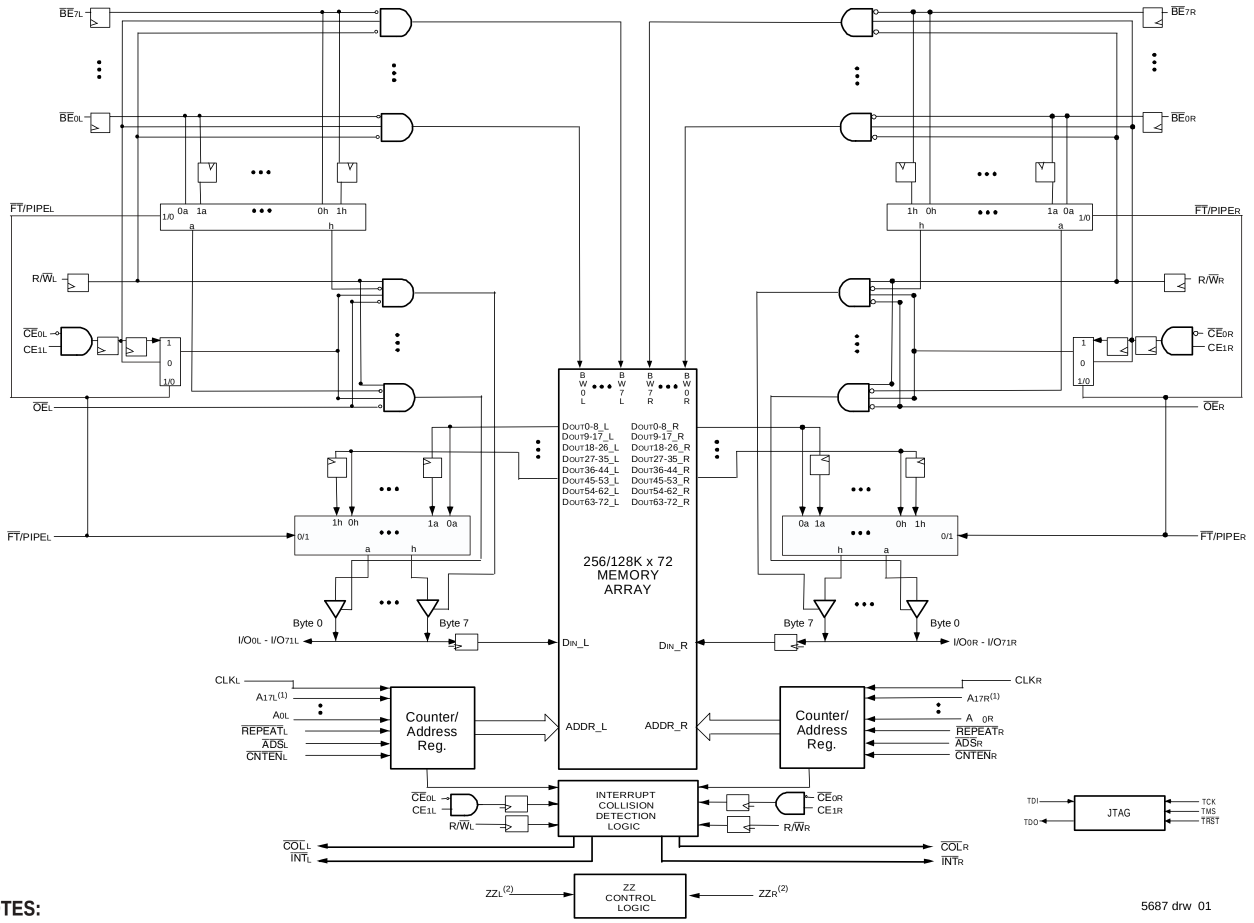
IDT70T3719/99M

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features:

- **True Dual-Port memory cells which allow simultaneous access of the same memory location**
- **High-speed data access**
  - *Commercial: 3.6ns (166MHz)/ 4.2ns (133MHz)(max.)*
  - *Industrial: 4.2ns (133MHz) (max.)*
- **Selectable Pipelined or Flow-Through output mode**
- **Counter enable and repeat features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Interrupt and Collision Detection Flags**
- **Full synchronous operation on both ports**
  - *6ns cycle time, 166MHz operation (23.9Gbps bandwidth)*
  - *Fast 3.6ns clock to data out*
  - *Self-timed write allows fast cycle time*
  - *1.7ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 166MHz*
  - *Data input, address, byte enable and control registers*
- **Separate byte controls for multiplexed bus and bus matching compatibility**
- **Dual Cycle Deselect (DCD) for Pipelined Output Mode**
- **2.5V (±100mV) power supply for core**
- **LVTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port**
- **Industrial temperature range (-40°C to +85°C) is available at 133MHz**
- **Available in a 324-pin Green Ball Grid Array (BGA)**
- **Includes JTAG Functionality**
- **Green parts available, see ordering information**

Functional Block Diagram



5687 drw 01

NOTES:

1. Address A17 is a NC for the IDT70T3799.
2. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}$x and OPTx and the sleep mode pins themselves (ZZx) are not affected during sleep mode.

FEBRUARY 2018

Description:

The IDT70T3719/99M is a high-speed 256K/128K x 72 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70T3719/99M has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70T3719/99M can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) is at 2.5V.

Pin Configuration (2,3,4,5)

70T3719/99M
BBG-324(6)

324-Pin BGA
Top View(7)

06/27/05

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	I/O$_{39R}$	I/O$_{38R}$	I/O$_{37R}$	I/O$_{36R}$	$\overline{\text{COL}}_L$	A$_{15L}$	A$_{12L}$	A$_{8L}$	$\overline{\text{BE}}_{7L}$	$\overline{\text{BE}}_{2L}$	CE$_{1L}$	$\overline{\text{ADS}}_L$	A$_{6L}$	A$_{1L}$	I/O$_{32R}$	I/O$_{33R}$	I/O$_{34R}$	I/O$_{35R}$	A
B	I/O$_{39L}$	I/O$_{38L}$	I/O$_{37L}$	I/O$_{36L}$	TDO	A$_{17L}$(1)	A$_{13L}$	A$_{10L}$	$\overline{\text{BE}}_{6L}$	$\overline{\text{BE}}_{5L}$	$\overline{\text{BE}}_{1L}$	$\overline{\text{OE}}_L$	$\overline{\text{REPEAT}}_L$	A$_{0L}$	I/O$_{32L}$	I/O$_{33L}$	I/O$_{34L}$	I/O$_{35L}$	B
C	I/O$_{40R}$	I/O$_{41R}$	I/O$_{42R}$	I/O$_{43R}$	$\overline{\text{INT}}_L$	A$_{16L}$	A$_{11L}$	A$_{7L}$	$\overline{\text{BE}}_{0L}$	$\overline{\text{CE}}_{0L}$	R/$\overline{\text{W}}_L$	$\overline{\text{CNTEN}}_L$	A$_{4L}$	A$_{3L}$	I/O$_{31R}$	I/O$_{30R}$	I/O$_{29R}$	I/O$_{28R}$	C
D	I/O$_{40L}$	I/O$_{41L}$	I/O$_{42L}$	I/O$_{43L}$	TDI	NC	A$_{14L}$	A$_{9L}$	$\overline{\text{BE}}_{4L}$	$\overline{\text{BE}}_{3L}$	CLK$_L$	A$_{5L}$	A$_{2L}$	ZZ$_L$	I/O$_{31L}$	I/O$_{30L}$	I/O$_{29L}$	I/O$_{28L}$	D
E	I/O$_{47R}$	I/O$_{46R}$	I/O$_{45R}$	I/O$_{44R}$	PL/$\overline{\text{FT}}_L$	V$_{DD}$	V$_{DDQL}$	V$_{DDQR}$	V$_{DDQR}$	V$_{DDQL}$	V$_{DDQL}$	V$_{DDQR}$	V$_{DDQR}$	OPT$_L$	I/O$_{24R}$	I/O$_{25R}$	I/O$_{26R}$	I/O$_{27R}$	E
F	I/O$_{47L}$	I/O$_{46L}$	I/O$_{45L}$	I/O$_{44L}$	V$_{DD}$	V$_{DD}$	V$_{DDQL}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{DD}$	V$_{DD}$	V$_{DD}$	V$_{DD}$	I/O$_{24L}$	I/O$_{25L}$	I/O$_{26L}$	I/O$_{27L}$	F
G	I/O$_{48R}$	I/O$_{49R}$	I/O$_{50R}$	I/O$_{51R}$	V$_{DDQR}$	V$_{DDQR}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{DDQR}$	V$_{DDQR}$	I/O$_{23R}$	I/O$_{22R}$	I/O$_{21R}$	I/O$_{20R}$	G
H	I/O$_{48L}$	I/O$_{49L}$	I/O$_{50L}$	I/O$_{51L}$	V$_{DDQL}$	V$_{DDQL}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{DDQL}$	V$_{DDQL}$	I/O$_{23L}$	I/O$_{22L}$	I/O$_{21L}$	I/O$_{20L}$	H
J	I/O$_{55R}$	I/O$_{54R}$	I/O$_{53R}$	I/O$_{52R}$	V$_{DDQR}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{DDQR}$	I/O$_{16R}$	I/O$_{17R}$	I/O$_{18R}$	I/O$_{19R}$	J
K	I/O$_{55L}$	I/O$_{54L}$	I/O$_{53L}$	I/O$_{52L}$	V$_{DDQR}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{DDQR}$	I/O$_{16L}$	I/O$_{17L}$	I/O$_{18L}$	I/O$_{19L}$	K
L	I/O$_{56R}$	I/O$_{57R}$	I/O$_{58R}$	I/O$_{59R}$	V$_{DDQL}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{DDQL}$	I/O$_{15R}$	I/O$_{14R}$	I/O$_{13R}$	I/O$_{12R}$	L
M	I/O$_{56L}$	I/O$_{57L}$	I/O$_{58L}$	I/O$_{59L}$	V$_{DDQL}$	V$_{DD}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{DDQL}$	V$_{DDQL}$	I/O$_{15L}$	I/O$_{14L}$	I/O$_{13L}$	I/O$_{12L}$	M
N	I/O$_{63R}$	I/O$_{62R}$	I/O$_{61R}$	I/O$_{60R}$	V$_{DDQR}$	V$_{DDQR}$	V$_{DDQL}$	V$_{DDQL}$	V$_{SS}$	V$_{SS}$	V$_{DD}$	V$_{DDQR}$	V$_{DDQR}$	V$_{DDQR}$	I/O$_{8R}$	I/O$_{9R}$	I/O$_{10R}$	I/O$_{11R}$	N
P	I/O$_{63L}$	I/O$_{62L}$	I/O$_{61L}$	I/O$_{60L}$	ZZ$_R$	TMS	V$_{DD}$	V$_{DD}$	V$_{DD}$	V$_{DDQL}$	V$_{DDQL}$	V$_{DD}$	V$_{DD}$	OPT$_R$	I/O$_{8L}$	I/O$_{9L}$	I/O$_{10L}$	I/O$_{11L}$	P
R	I/O$_{64R}$	I/O$_{65R}$	I/O$_{66R}$	I/O$_{67R}$	$\overline{\text{COL}}_R$	A$_{17R}$(1)	A$_{12R}$	A$_{9R}$	$\overline{\text{BE}}_{4R}$	$\overline{\text{CE}}_{0R}$	$\overline{\text{OE}}_R$	A$_{6R}$	A$_{2R}$	A$_{1R}$	I/O$_{7R}$	I/O$_{6R}$	I/O$_{5R}$	I/O$_{4R}$	R
T	I/O$_{64L}$	I/O$_{65L}$	I/O$_{66L}$	I/O$_{67L}$	PL/$\overline{\text{FT}}_R$	A$_{16R}$	A$_{13R}$	A$_{7R}$	$\overline{\text{BE}}_{7R}$	$\overline{\text{BE}}_{3R}$	CE$_{1R}$	$\overline{\text{ADS}}_R$	A$_{4R}$	A$_{0R}$	I/O$_{7L}$	I/O$_{6L}$	I/O$_{5L}$	I/O$_{4L}$	T
U	I/O$_{71R}$	I/O$_{70R}$	I/O$_{69R}$	I/O$_{68R}$	TCK	$\overline{\text{INT}}_R$	A$_{14R}$	A$_{10R}$	$\overline{\text{BE}}_{2R}$	$\overline{\text{BE}}_{6R}$	$\overline{\text{BE}}_{1R}$	R/$\overline{\text{W}}_R$	$\overline{\text{REPEAT}}_R$	A$_{3R}$	I/O$_{0R}$	I/O$_{1R}$	I/O$_{2R}$	I/O$_{3R}$	U
V	I/O$_{71L}$	I/O$_{70L}$	I/O$_{69L}$	I/O$_{68L}$	$\overline{\text{TRST}}$	NC	A$_{15R}$	A$_{11R}$	A$_{8R}$	$\overline{\text{BE}}_{5R}$	$\overline{\text{BE}}_{0R}$	CLK$_R$	$\overline{\text{CNTEN}}_R$	A$_{5R}$	I/O$_{0L}$	I/O$_{1L}$	I/O$_{2L}$	I/O$_{3L}$	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

5687 tbl 01

NOTES:

1. Pin is a NC for IDT70T3799.
2. All V$_{DD}$ pins must be connected to 2.5V power supply.
3. All V$_{DDQ}$ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V$_{DD}$ (2.5V), and 2.5V if OPT pin for that port is set to V$_{SS}$ (0V).
4. All V$_{SS}$ pins must be connected to ground supply.
5. Package body is approximately 19mm x 19mm x 1.76mm, with 1.0mm ball-pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables (Input)[6]
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable (Input)
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable (Input)
A_{0L} - A_{17L}[5]	A_{0R} - A_{17R}[5]	Address (Input)
I/O_{0L} - I/O_{71L}	I/O_{0R} - I/O_{71R}	Data Input/Output
CLK_L	CLK_R	Clock (Input)
$PL/\overline{FT}_L$	$PL/\overline{FT}_R$	Pipeline/Flow-Through (Input)
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable (Input)
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable (Input)
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat[3]
$\overline{BE}_{0L}$ - $\overline{BE}_{7L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{7R}$	Byte Enables (9-bit bytes) (Input)[6]
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)[1] (Input)
OPT_L	OPT_R	Option for selecting V_{DDQX}[1,2] (Input)
ZZ_L	ZZ_R	Sleep Mode pin[4] (Input)
V_{DD}		Power (2.5V)[1] (Input)
V_{SS}		Ground (0V) (Input)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz) (Input)
TMS		Test Mode Select (Input)
$\overline{TRST}$		Reset (Initialize TAP Controller) (Input)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag (Output)
$\overline{COL}_L$	$\overline{COL}_R$	Collision Alert (Output)

5687 tbl 02

NOTES:

1. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to V_{DD} (2.5V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to V_{SS} (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
3. When $\overline{REPEAT}_X$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_X$.
4. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., $PL/\overline{FT}_X$ and OPT_X and the sleep mode pins themselves (ZZ_X) are not affected during sleep mode. It is recommended that boundry scan not be operated during sleep mode.
5. Address A_{17x} is a NC for the IDT70T3799M.
6. Chip Enables and Byte Enables are double buffered when $PL/\overline{FT} = V_{IH}$, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control (1,2,3,4,5)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	Byte Enables	R/$\overline{W}$	ZZ	I/O Operation[6]	MODE
X	↑	H	X	All $\overline{BE}$ = X	X	L	All Bytes= High-Z	Deselected: Power Down
X	↑	X	L	All $\overline{BE}$ = X	X	L	All Bytes = High-Z	Deselected: Power Down
X	↑	L	H	All $\overline{BE}$ = H	X	L	All Bytes = High-Z	All Bytes Deselected
X	↑	L	H	$\overline{BE}_n$ = L, All other $\overline{BE}$ = H	L	L	$Byte_n = D_{IN}$, All other Bytes = High-Z	Write to Byte X Only
X	↑	L	H	$\overline{BE}_{4-7}$ = L, $\overline{BE}_{0-3}$ = H	L	L	$Byte_{4-7} = D_{IN}$, $Byte_{0-3}$ = High-Z	Write to Lower Bytes Only
X	↑	L	H	$\overline{BE}_{4-7}$ = H, $\overline{BE}_{0-3}$ = L	L	L	$Byte_{4-7}$ = High-Z, $Byte_{0-3} = D_{IN}$	Write to Upper Bytes Only
X	↑	L	H	$\overline{BE}_{0-7}$ = L	L	L	$Byte_{0-7} = D_{IN}$	Write to All Bytes
L	↑	L	H	$\overline{BE}_n$ = L, All other $\overline{BE}$ = H	H	L	$Byte_n = D_{OUT}$, All other Bytes = High-Z	Read Byte X Only
L	↑	L	H	$\overline{BE}_{4-7}$ = L, $\overline{BE}_{0-3}$ = H	H	L	$Byte_{4-7} = D_{OUT}$, $Byte_{0-3}$ = High-Z	Read Lower Bytes Only
L	↑	L	H	$\overline{BE}_{4-7}$ = H, $\overline{BE}_{0-3}$ = L	H	L	$Byte_{4-7}$ = High-Z, $Byte_{0-3} = D_{OUT}$	Read Upper Bytes Only
L	↑	L	H	All $\overline{BE}$ = L	H	L	All Bytes = D_{OUT}	Read All Bytes
H	X	X	X	All $\overline{BE}$ = X	X	L	All Bytes = High-Z	Outputs Disabled
X	X	X	X	All $\overline{BE}$ = X	X	H	All Bytes = High-Z	Sleep Mode

5687 tbl 03

NOTES:

1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = X.
3. $\overline{OE}$ and ZZ are asynchronous input signals.
4. It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.
5. For the examples shown here, $\overline{BE}_n$ may correspond to any of the eight byte enable signals.

Truth Table II—Address Counter Control (1,2)

Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$[4]	$\overline{CNTEN}$	$\overline{REPEAT}$[4,6]	I/O[3]	MODE
An	X	An	↑	L	X	H	$D_{I/O}(n)$	External Address Used
X	An	An + 1	↑	H	L[5]	H	$D_{I/O}(n+1)$	Counter Enabled-Internal Address generation
X	An + 1	An + 1	↑	H	H	H	$D_{I/O}(n+1)$	Enabled Address Blocked-Counter disabled (An + 1 reused)
X	X	An	↑	X	X	L	$D_{I/O}(n)$	Counter Set to last valid $\overline{ADS}$ load

5687 tbl 04

NOTES:

1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE}_0$, CE_1, $\overline{BE}_n$ and $\overline{OE}$.
3. Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{REPEAT}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{BE}_n$.
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1, $\overline{BE}_n$.
6. When $\overline{REPEAT}$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}$. This value is not set at power-up: a known location should be loaded via $\overline{ADS}$ during initialization if desired. Any subsequent $\overline{ADS}$ access during operations will update the $\overline{REPEAT}$ address location.

Recommended Operating Temperature and Supply Voltage $^{(1)}$

Grade	Ambient Temperature	GND	VDD
Commercial	0^{O}C to +70^{O}C	0V	2.5V ± 100mV
Industrial	-40^{O}C to +85^{O}C	0V	2.5V ± 100mV

5687 tbl 05

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions with VDDQ at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	2.4	2.5	2.6	V
VDDQ	I/O Supply Voltage$^{(3)}$	2.4	2.5	2.6	V
VSS	Ground	0	0	0	V
VIH	Input High Volltage (Address, Control & Data I/O Inputs)$^{(3)}$	1.7	—	VDDQ + 100mV$^{(2)}$	V
VIH	Input High Voltage – JTAG	1.7	—	VDD + 100mV$^{(2)}$	V
VIH	Input High Voltage - ZZ, OPT, PIPE/$\overline{\text{FT}}$	VDD - 0.2V	—	VDD + 100mV$^{(2)}$	V
VIL	Input Low Voltage	-0.3$^{(1)}$	—	0.7	V
VIL	Input Low Voltage - ZZ, OPT, PIPE/$\overline{\text{FT}}$	-0.3$^{(1)}$	—	0.2	V

5687 tbl 06a

NOTES:
1. VIL (min.) = -1.0V for pulse width less than tCYC/2 or 5ns, whichever is less.
2. VIH (max.) = VDDQ + 1.0V for pulse width less than tCYC/2 or 5ns, whichever is less.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to VSS(0V), and VDDQX for that port must be supplied as indicated above.

Recommended DC Operating Conditions with VDDQ at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	2.4	2.5	2.6	V
VDDQ	I/O Supply Voltage$^{(3)}$	3.15	3.3	3.45	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage (Address, Control &Data I/O Inputs)$^{(3)}$	2.0	—	VDDQ + 150mV$^{(2)}$	V
VIH	Input High Voltage – JTAG	1.7	—	VDD + 100mV$^{(2)}$	V
VIH	Input High Voltage - ZZ, OPT, PIPE/$\overline{\text{FT}}$	VDD - 0.2V	—	VDD + 100mV$^{(2)}$	V
VIL	Input Low Voltage	-0.3$^{(1)}$	—	0.8	V
VIL	Input Low Voltage - ZZ, OPT, PIPE/$\overline{\text{FT}}$	-0.3$^{(1)}$	—	0.2	V

5687 tbl 06b

NOTES:
1. VIL (min.) = -1.0V for pulse width less than tCYC/2, or 5ns, whichever is less.
2. VIH (max.) = VDDQ + 1.0V for pulse width less than tCYC/2 or 5ns, whichever is less.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to VDD (2.5V), and VDDQX for that port must be supplied as indicated above.

Absolute Maximum Ratings (1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM} (V_{DD})	V_{DD} Terminal Voltage with Respect to GND	-0.5 to 3.6	V
$V_{TERM}^{(2)}$ (V_{DDQ})	V_{DDQ} Terminal Voltage with Respect to GND	-0.3 to V_{DDQ} + 0.3	V
$V_{TERM}^{(2)}$ (INPUTS and I/O's)	Input and I/O Terminal Voltage with Respect to GND	-0.3 to V_{DDQ} + 0.3	V
$T_{BIAS}^{(3)}$	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}(For V_{DDQ} = 3.3V)	DC Output Current	50	mA
I_{OUT}(For V_{DDQ} = 2.5V)	DC Output Current	40	mA

5687 tbl 07

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

Capacitance (1)

(T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	15	pF
$C_{OUT}^{(2)}$	Output Capacitance	V_{OUT} = 0V	10.5	pF

5687 tbl 08

NOTES:

1. These parameters are determined by device characterization, but are not production tested.
2. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 2.5V ± 100mV)

Symbol	Parameter	Test Conditions	70T3719/99M		Unit
			Min.	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current(1)	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\lvert I_{LI}\rvert$	JTAG & ZZ Input Leakage Current(1,2)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	±30	µA
$\lvert I_{LO}\rvert$	Output Leakage Current(1,3)	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage(1)	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage(1)	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage(1)	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage(1)	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

5687 tbl 09

NOTES:

1. V_{DDQ} is selectable (3.3V/2.5V) via $\overline{OPT}$ pins. Refer to p.5 for details.
2. Applicable only for TMS, TDI and $\overline{TRST}$ inputs.
3. Outputs tested in tri-state mode.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (3) (V_{DD} = 2.5V ± 100mV)

				70T3719/99M S166 Com'l Only		70T3719/99M S133 Com'l & Ind		
Symbol	Parameter	Test Condition	Version	Typ.(4)	Max.	Typ.(4)	Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}(1)	COM'L S	640	900	520	740	mA
			IND S	—	—	520	900	
I_{SB1}(6)	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}(1)	COM'L S	350	460	280	380	mA
			IND S	—	—	280	470	
I_{SB2}(6)	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(1)	COM'L S	500	650	400	500	mA
			IND S	—	—	400	620	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ $\geq$ V_{DDQ} - 0.2V, V_{IN} $\geq$ V_{DDQ} - 0.2V or V_{IN} $\leq$ 0.2V, f = 0(2)	COM'L S	12	20	12	20	mA
			IND S	—	—	12	25	
I_{SB4}(6)	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ $\leq$ 0.2V and $\overline{CE}_{"B"}$ $\geq$ V_{DDQ} - 0.2V(5) V_{IN} $\geq$ V_{DDQ} - 0.2V or V_{IN} $\leq$ 0.2V Active Port, Outputs Disabled, f = f_{MAX}(1)	COM'L S	500	650	400	500	mA
			IND S	—	—	400	620	
Izz	Sleep Mode Current (Both Ports - TTL Level Inputs)	ZZ_L = ZZ_R = V_{IH} f=f_{MAX}(1)	COM'L S	12	20	12	20	mA
			IND S	—	—	12	25	

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NOTES:

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS".
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 2.5V, T_A = 25°C for Typ, and are not production tested. $I_{DD\ DC}$(f=0) = 30mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ $\leq$ 0.2V means $\overline{CE}_{0X}$ $\leq$ 0.2V and CE_{1X} $\geq$ V_{DD} - 0.2V
   $\overline{CE}_X$ $\geq$ V_{DD} - 0.2V means $\overline{CE}_{0X}$ $\geq$ V_{DD} - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.
6. I_{SB1}, I_{SB2} and I_{SB4} will all reach full standby levels (I_{SB3}) on the appropriate port(s) if ZZ_L and/or ZZ_R = V_{IH}.

AC Test Conditions (VDDQ - 3.3V/2.5V)

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figure 1

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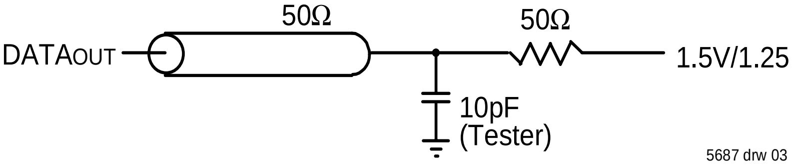

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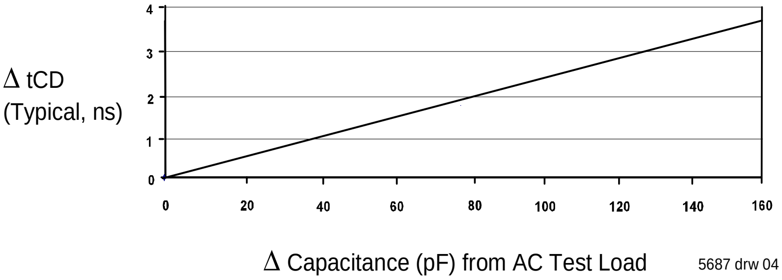
Figure 1. AC Output Test load.



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AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) $^{(2,3)}$ (V_{DD} = 2.5V ± 100mV, T_A = 0°C to +70°C)

		70T3719/99M S166 Com'l Only		70T3719/99M S133 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{CYC1}	Clock Cycle Time (Flow-Through)$^{(1)}$	20	—	25	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)$^{(1)}$	6	—	7.5	—	ns
t_{CH1}	Clock High Time (Flow-Through)$^{(1)}$	8	—	10	—	ns
t_{CL1}	Clock Low Time (Flow-Through)$^{(1)}$	8	—	10	—	ns
t_{CH2}	Clock High Time (Pipelined)$^{(2)}$	2.4	—	3	—	ns
t_{CL2}	Clock Low Time (Pipelined)$^{(1)}$	2.4	—	3	—	ns
t_{SA}	Address Setup Time	1.7	—	1.8	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	ns
t_{SC}	Chip Enable Setup Time	1.7	—	1.8	—	ns
t_{HC}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{SB}	Byte Enable Setup Time	1.7	—	1.8	—	ns
t_{HB}	Byte Enable Hold Time	0.5	—	0.5	—	ns
t_{SW}	R/W Setup Time	1.7	—	1.8	—	ns
t_{HW}	R/W Hold Time	0.5	—	0.5	—	ns
t_{SD}	Input Data Setup Time	1.7	—	1.8	—	ns
t_{HD}	Input Data Hold Time	0.5	—	0.5	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	1.7	—	1.8	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	1.7	—	1.8	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	ns
t_{SRPT}	$\overline{REPEAT}$ Setup Time	1.7	—	1.8	—	ns
t_{HRPT}	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	ns
t_{OE}	Output Enable to Data Valid	—	4.4	—	4.6	ns
$t_{OLZ}^{(4)}$	Output Enable to Output Low-Z	1	—	1	—	ns
$t_{OHZ}^{(4)}$	Output Enable to Output High-Z	1	3.6	1	4.2	ns
t_{CD1}	Clock to Data Valid (Flow-Through)$^{(1)}$	—	12	—	15	ns
t_{CD2}	Clock to Data Valid (Pipelined)$^{(1)}$	—	3.6	—	4.2	ns
t_{DC}	Data Output Hold After Clock High	1	—	1	—	ns
$t_{CKHZ}^{(4)}$	Clock High to Output High-Z	1	3.6	1	4.2	ns
$t_{CKLZ}^{(4)}$	Clock High to Output Low-Z	1	—	1	—	ns
t_{INS}	Interrupt Flag Set Time	—	7	—	7	ns
t_{INR}	Interrupt Flag Reset Time	—	7	—	7	ns
t_{COLS}	Collision Flag Set Time	—	3.6	—	4.2	ns
t_{COLR}	Collision Flag Reset Time	—	3.6	—	4.2	ns
t_{ZZSC}	Sleep Mode Set Cycles	2	—	2	—	cycles
t_{ZZRC}	Sleep Mode Recovery Cycles	3	—	3	—	cycles
Port-to-Port Delay						
t_{CO}	Clock-to-Clock Offset	5	—	6	—	ns
t_{OFS}	Clock-to-Clock Offset for Collision Detection	Please refer to collision Detection Timing Table on Page 19.				

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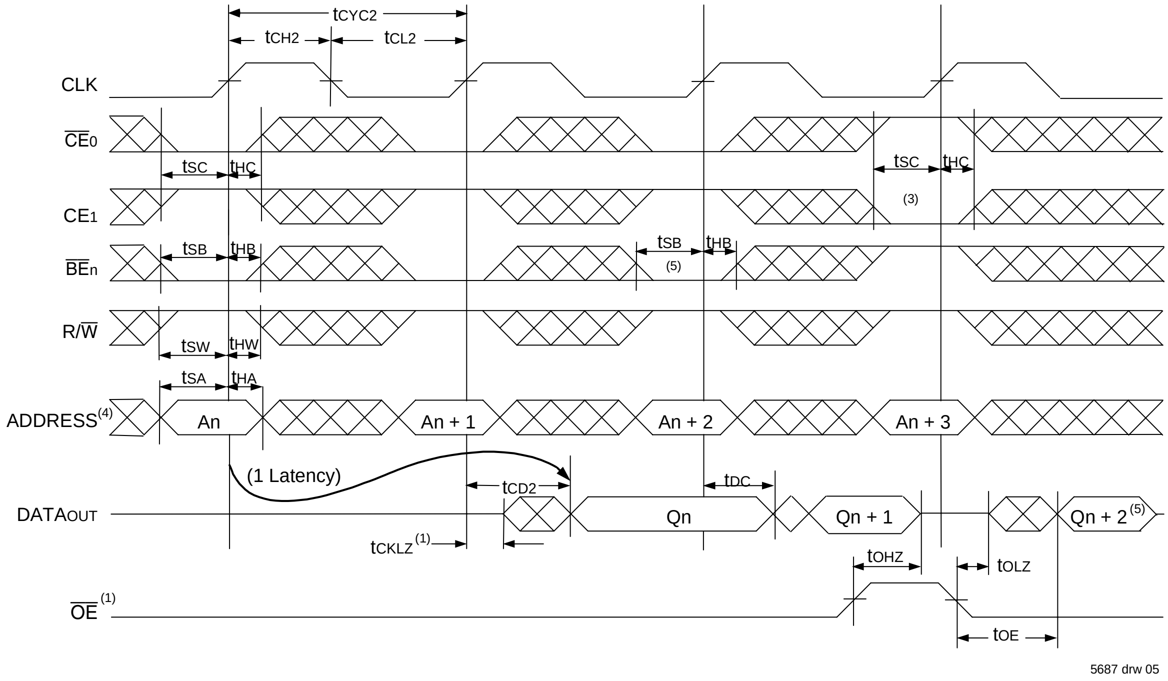
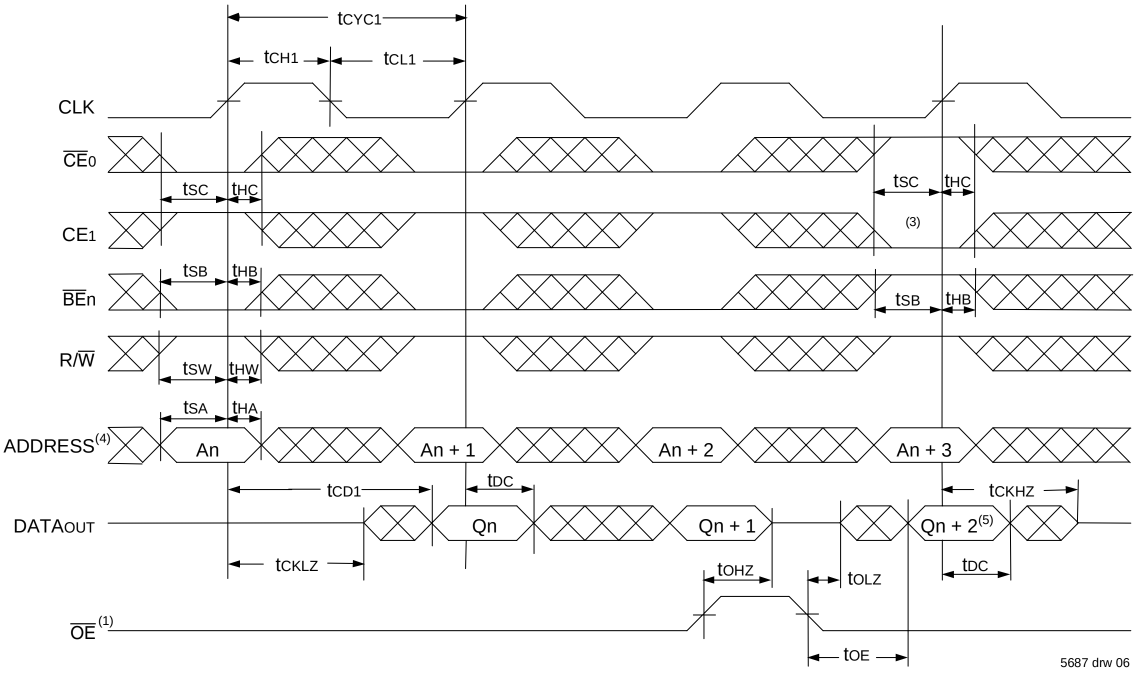
NOTES:

1. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPE$_X$ = V_{DD} (2.5V). Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{SS} (0V) for that port.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$), $\overline{FT}$/PIPE and OPT. $\overline{FT}$/PIPE and OPT should be treated as DC signals, i.e. steady state during operation.
3. These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 6 for details on selecting the desired operating voltage levels for each port.
4. Guaranteed by design (not production tested).

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE'X' = V_{IH})$^{(1,2)}$



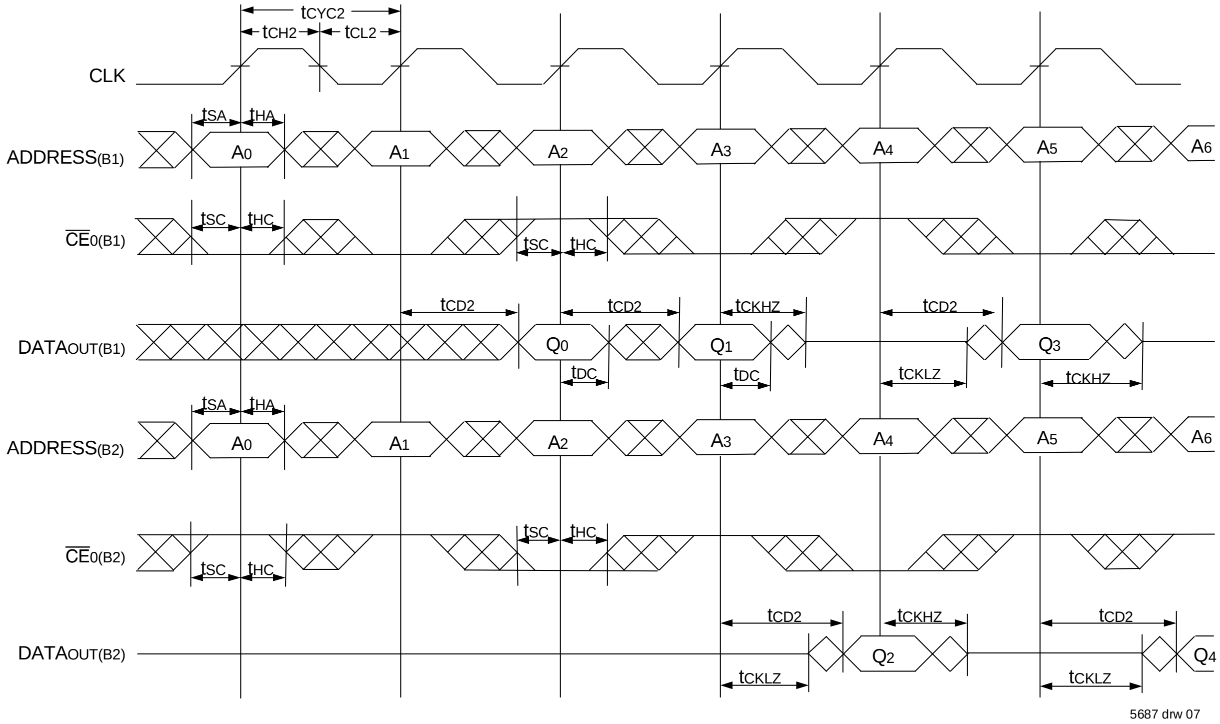
Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}$/PIPE"X" = V_{IL})$^{(1,2,6)}$



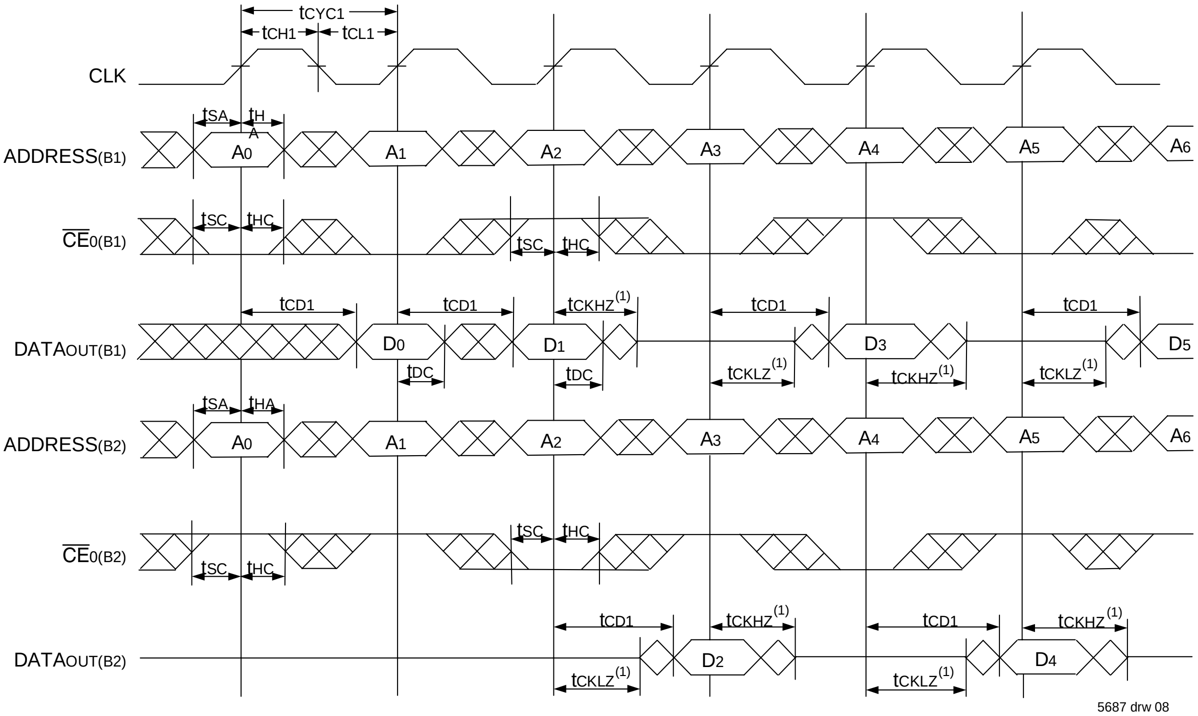
NOTES:

1. $\overline{OE}$ is asynchronously controlled; all other inputs depicted in the above waveforms are synchronous to the rising clock edge.
2. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{REPEAT}$ = V_{IH}.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH}, CE_1 = V_{IL}, $\overline{BE}_n$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{BE}_n$ was HIGH, then the appropriate Byte of $DATA_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read (1,2)



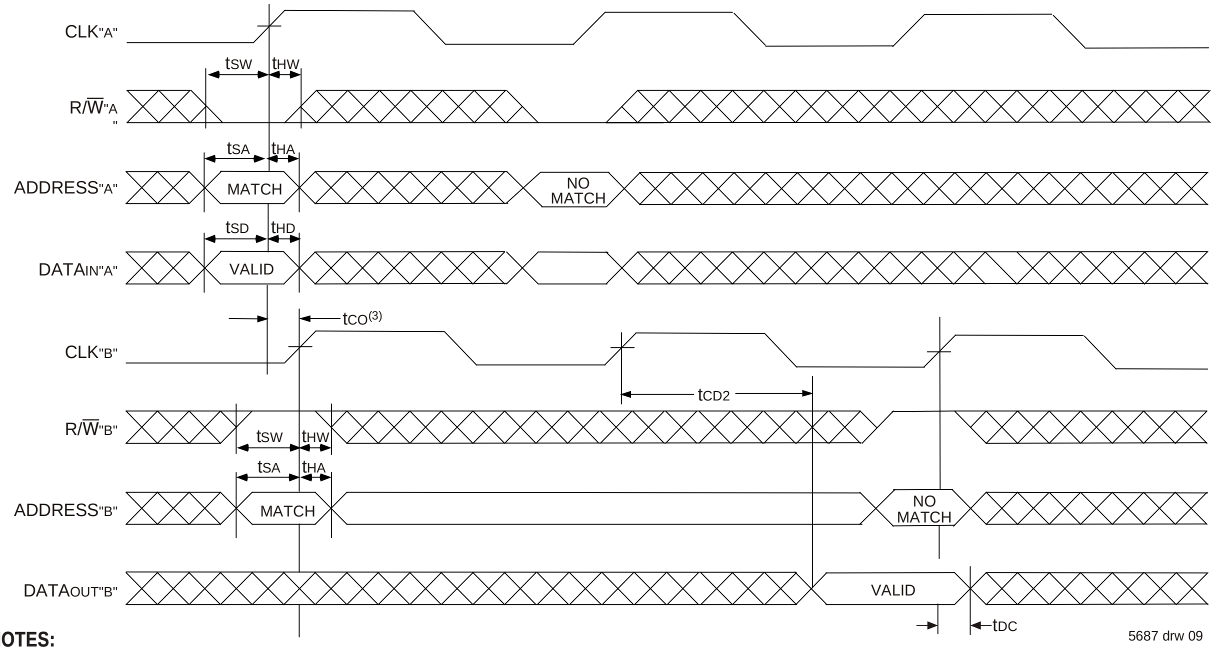
Timing Waveform of a Multi-Device Flow-Through Read (1,2)



NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70T3719/99M for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{BE}_n$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.

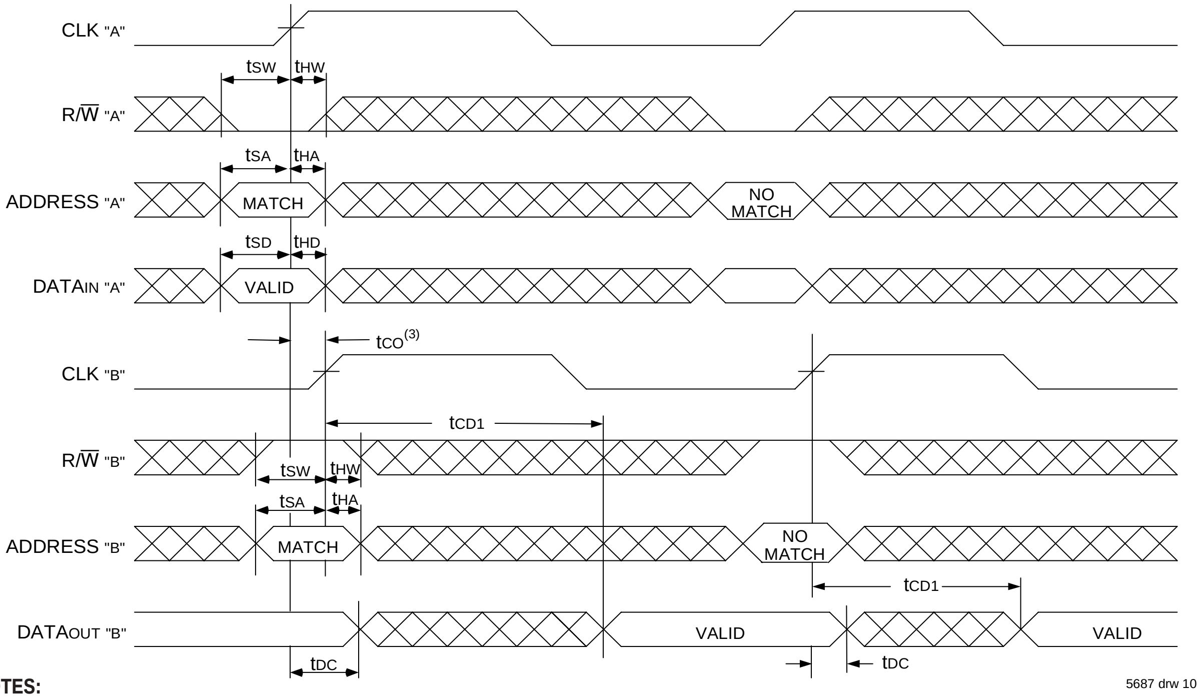
Timing Waveform of Left Port Write to Pipelined Right Port Read (1,2,4)



NOTES:

1. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port "B", which is being read from. $\overline{OE}$ = V_{IH} for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2\ t_{CYC2} + t_{CD2}$). If $t_{CO} >$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

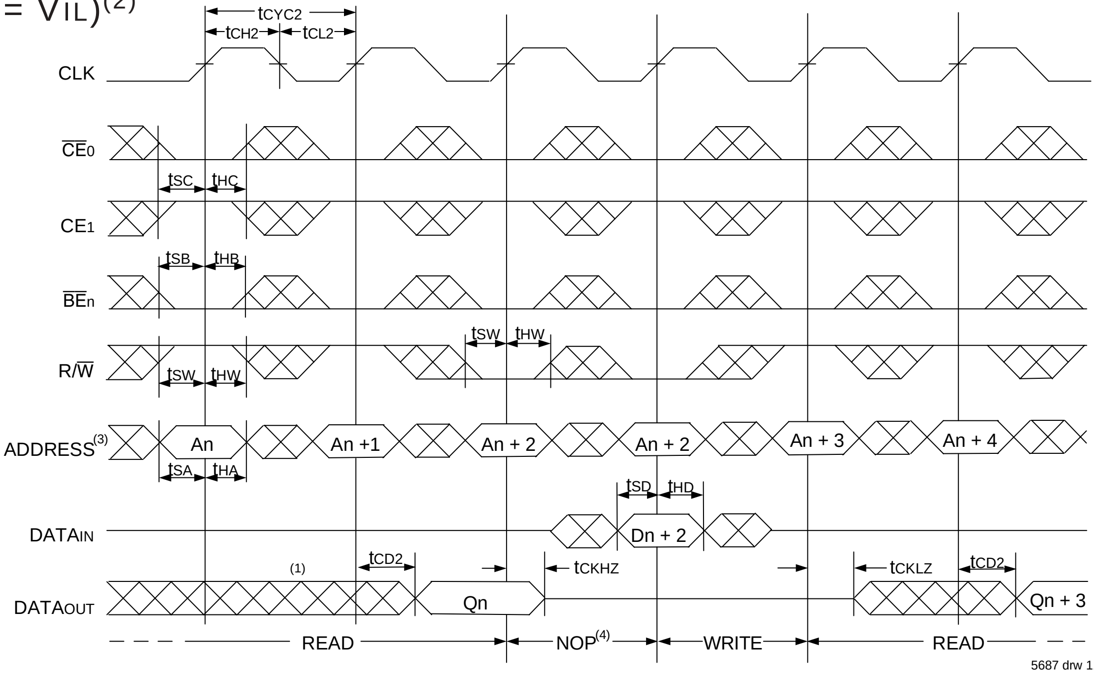
Timing Waveform with Port-to-Port Flow-Through Read (1,2,4)



NOTES:

1. $\overline{CE}_0$, $\overline{BE}$n, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD1}$). If $t_{CO} >$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CD1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

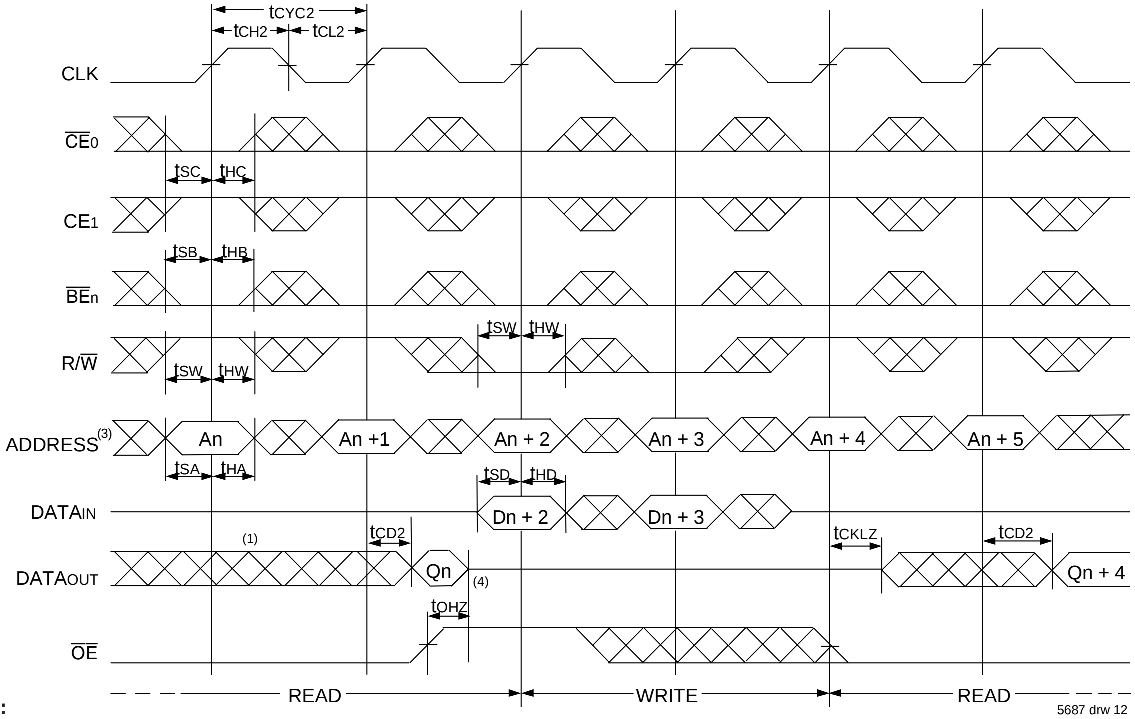
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)[2]



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

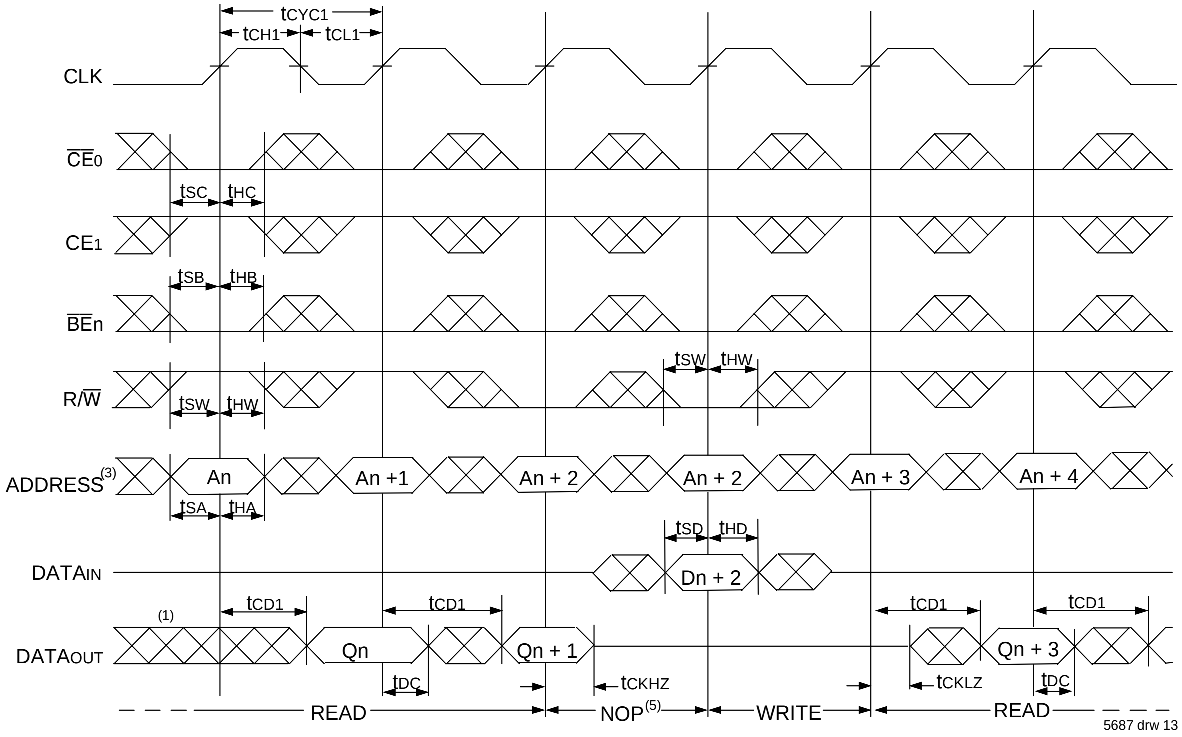
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)[2]



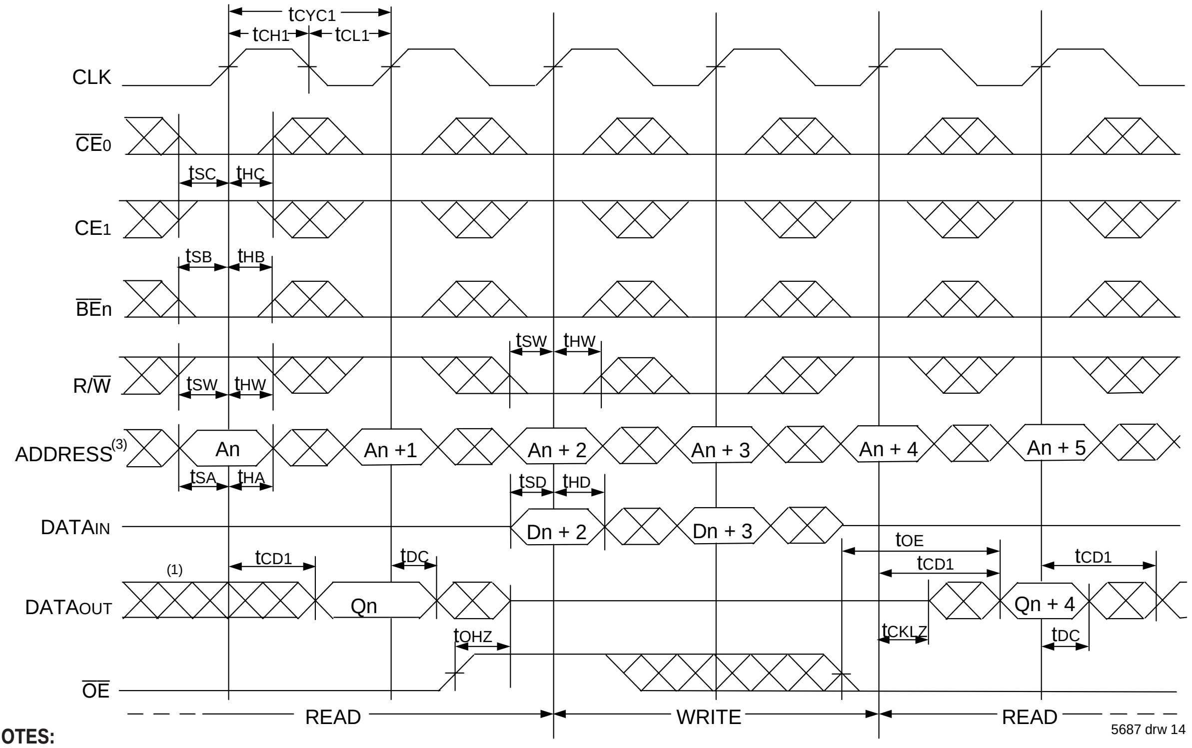
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})$^{(2)}$



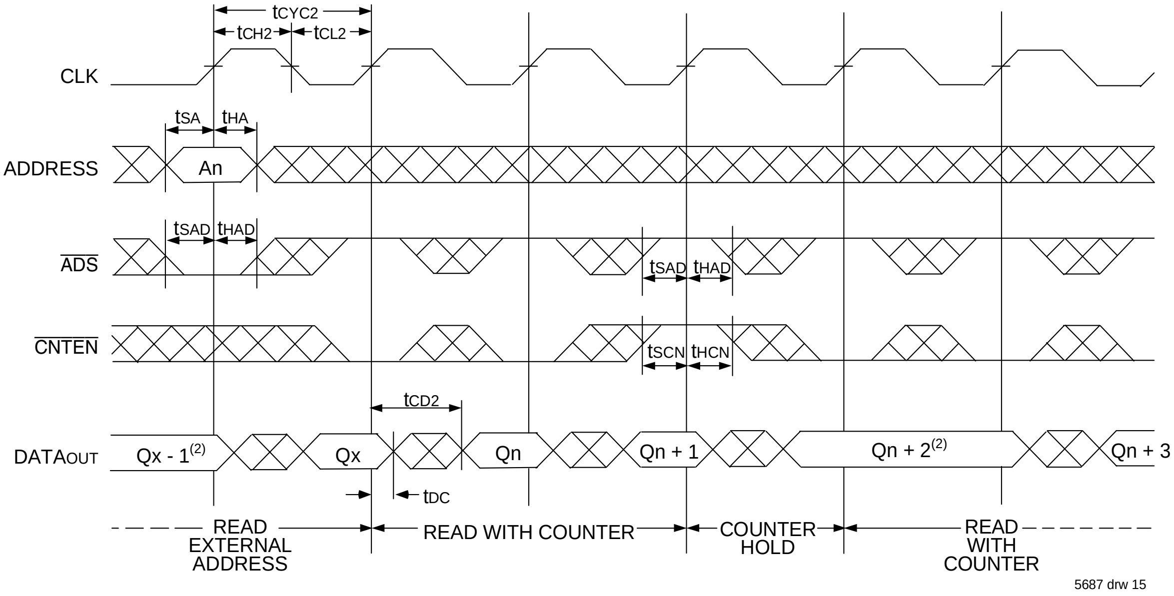
Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)$^{(2)}$



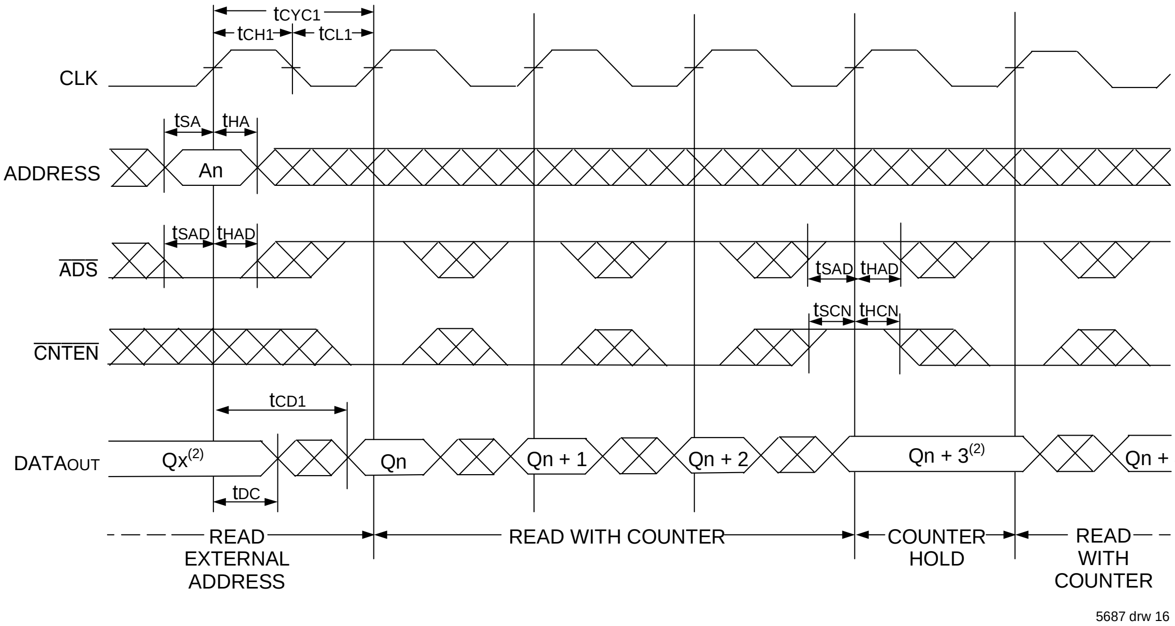
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE}$n, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance [(1)]



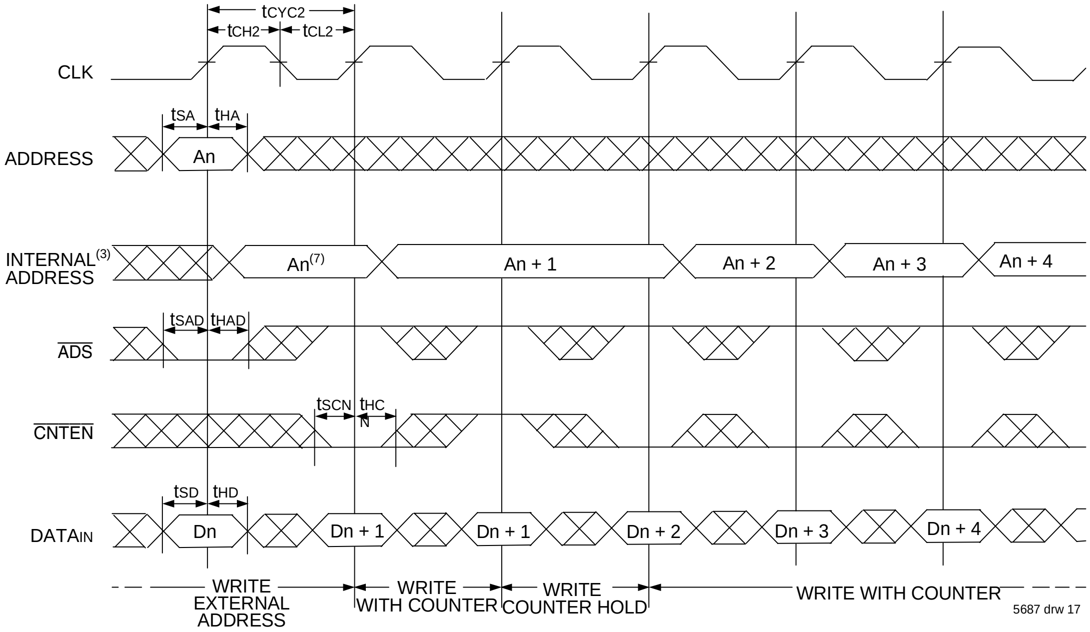
Timing Waveform of Flow-Through Read with Address Counter Advance [(1)]



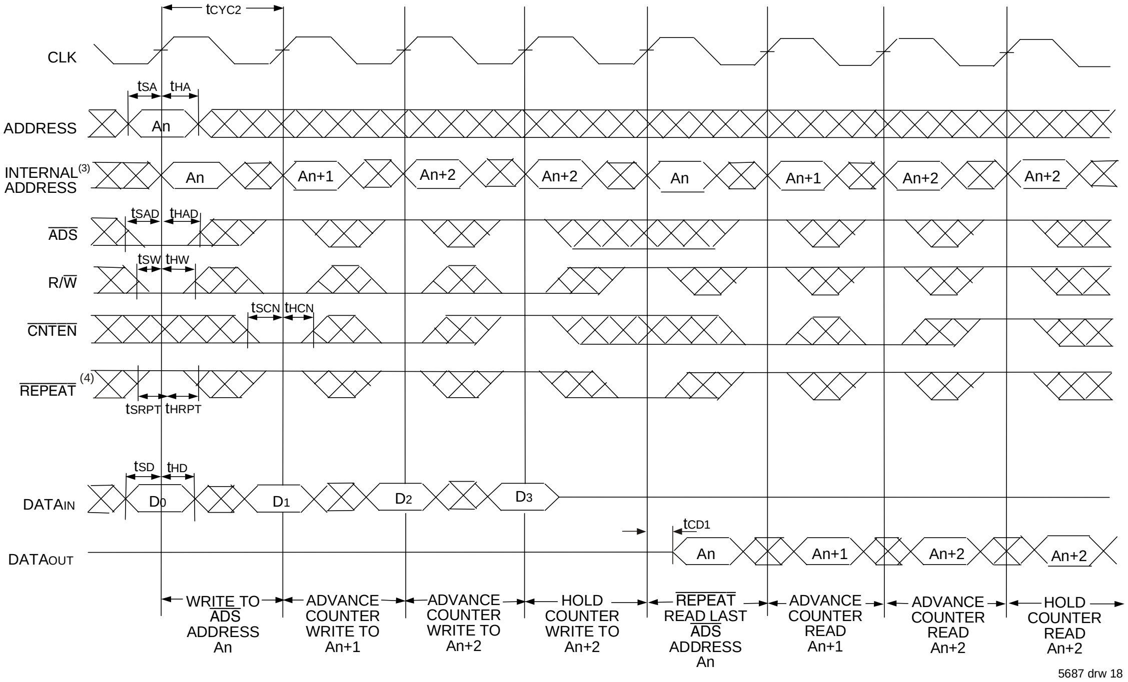
NOTES:

1. $\overline{CE_0}$, $\overline{OE}$, $\overline{BE}n$ = V_{IL}; CE_1, $R/\overline{W}$, and $\overline{REPEAT}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs) (1)



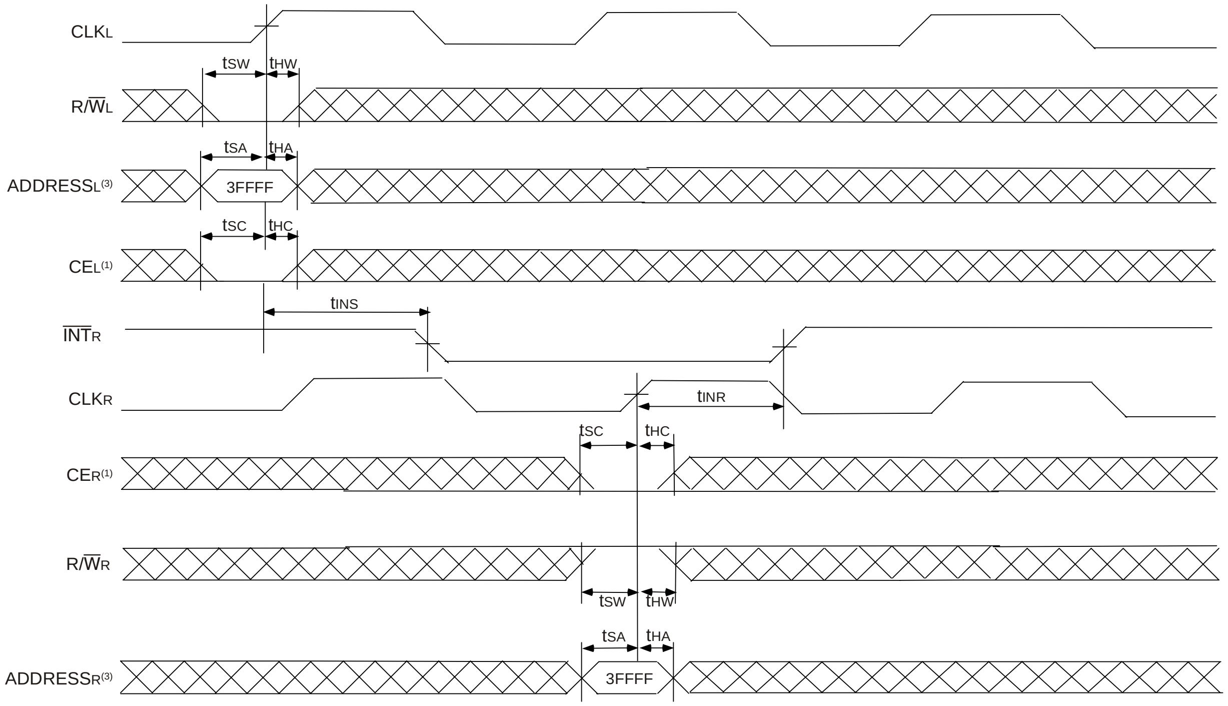
Timing Waveform of Counter Repeat (2,6)



NOTES:

1. $\overline{CE}_0$, $\overline{BE}_n$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{CE}_0$, $\overline{BE}_n$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. No dead cycle exists during $\overline{REPEAT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{REPEAT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. For more information on $\overline{REPEAT}$ function refer to Truth Table II.
5. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.
6. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

Waveform of Interrupt Timing (2)



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NOTES:
1. $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$
2. All timing is the same for Left and Right ports.
3. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

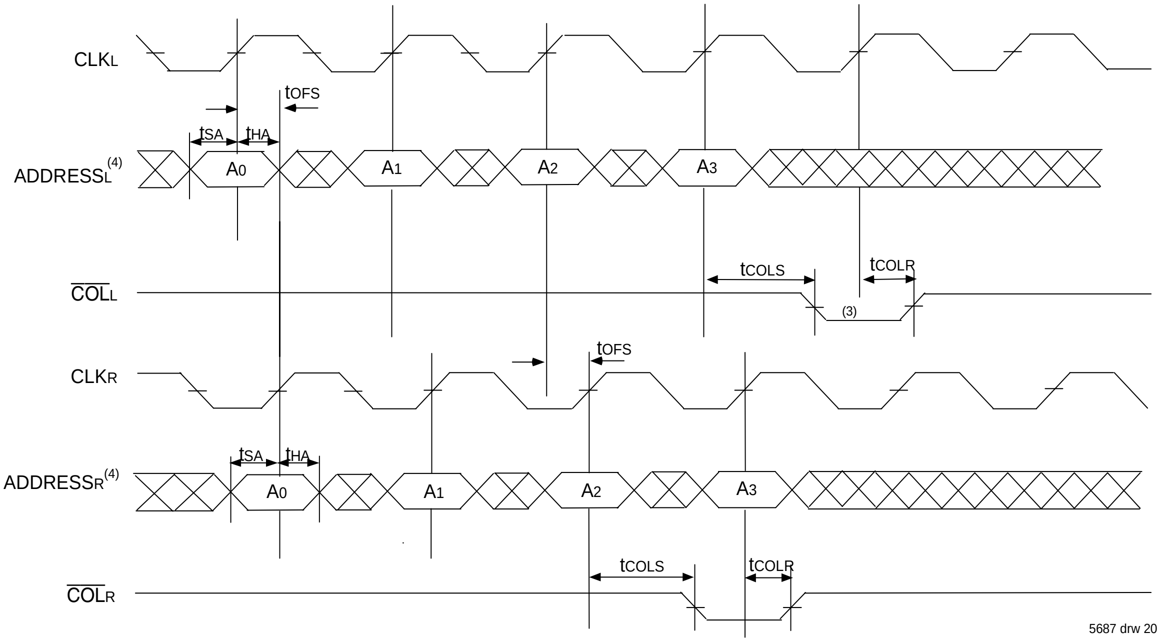
Truth Table III — Interrupt Flag (1)

Left Port						Right Port				
CLK_L	$R/\overline{W}_L$	$\overline{CE}_L$	A_{17L}-A_{0L} (3,4)	$\overline{INT}_L$	CLK_R	$R/\overline{W}_R$ (2)	$\overline{CE}_R$ (2)	A_{17R}-A_{0R} (3,4)	$\overline{INT}_R$	Function
↑	L	L	3FFFF	X	↑	X	X	X	L	Set Right $\overline{INT}_R$ Flag
↑	X	X	X	X	↑	X	L	3FFFF	H	Reset Right $\overline{INT}_R$ Flag
↑	X	X	X	L	↑	L	L	3FFFE	X	Set Left $\overline{INT}_L$ Flag
↑	H	L	3FFFE	H	↑	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

5687 tbl 13

NOTES:
1. $\overline{INT}_L$ and $\overline{INT}_R$ must be initialized at power-up by Resetting the flags.
2. $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$. $R/\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
3. $A17_X$ is a NC for IDT70T3799, therefore Interrupt Addresses are 1FFFF and 1FFFE.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Waveform of Collision Timing(1,2)
Both Ports Writing with Left Port Clock Leading



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NOTES:
1. $\overline{CE}_0$ = V_{IL}, CE_1 = V_{IH}.
2. For reading port, $\overline{OE}$ is a Don't care on the Collision Detection Logic. Please refer to Truth Table IV for specific cases.
3. Leading Port Output flag might output 3t_{CYC2} + t_{COLS} after Address match.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Collision Detection Timing(3,4)

Cycle Time	t_{OFS} (ns)	
	Region 1 (ns) (1)	Region 2 (ns) (2)
5ns	0 - 2.8	2.81 - 4.6
6ns	0 - 3.8	3.81 - 5.6
7.5ns	0 - 5.3	5.31 - 7.1

56876 tbl 14

NOTES:
1. Region 1
   Both ports show collision after 2nd cycle for Addresses 0, 2, 4 etc.
2. Region 2
   Leading port shows collision after 3rd cycle for addresses 0, 3, 6, etc. while trailing port shows collision after 2nd cycle for addresses 0, 2, 4 etc.
3. All the production units are tested to midpoint of each region.
4. These ranges are based on characterization of a typical device.

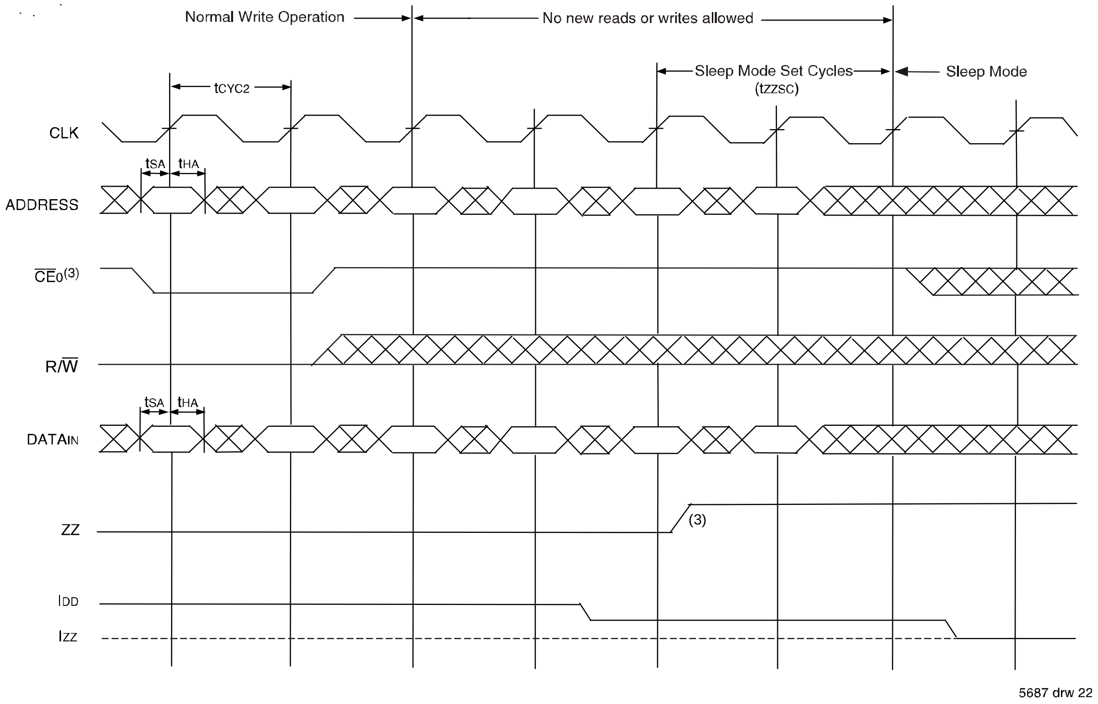
Truth Table IV — Collision Detection Flag

Left Port					Right Port					Function
CLK_L	$R/\overline{W}_L$	$\overline{CE}_L$	A_{17L}-A_{0L}(2)	$\overline{COL}_L$	CLK_R	$R/\overline{W}_R$(1)	$\overline{CE}_R$(1)	A_{17R}-A_{0R}(2)	$\overline{COL}_R$	
↑	H	L	MATCH	H	↑	H	L	MATCH	H	Both ports reading. Not a valid collision. No flag output on either port
↑	H	L	MATCH	L	↑	L	L	MATCH	H	Left port reading, Right port writing. Valid collision, flag output on Left port.
↑	L	L	MATCH	H	↑	H	L	MATCH	L	Right port reading, Left port writing. Valid collision, flag output on Right port.
↑	L	L	MATCH	L	↑	L	L	MATCH	L	Both ports writing. Valid collision. Flag output on both ports.

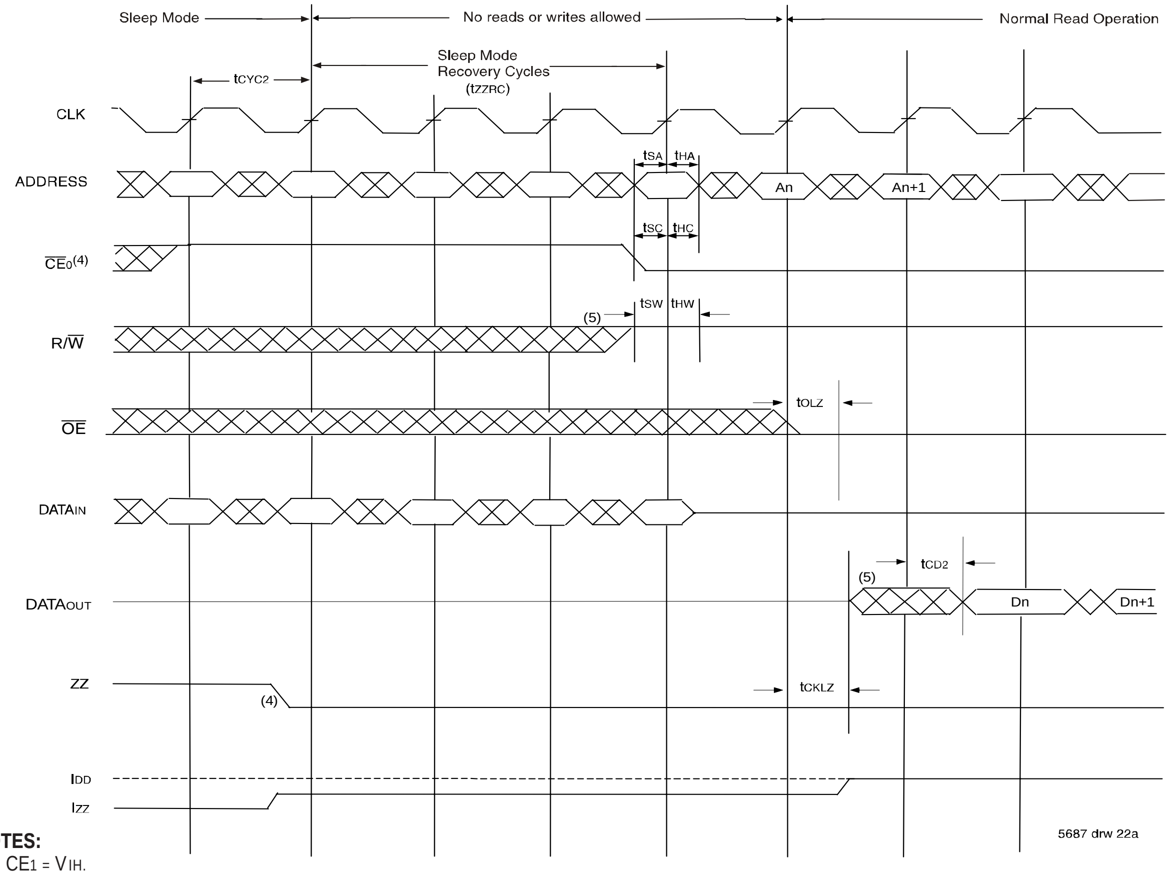
5687 tbl 15

NOTES:
1. $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}. R/$\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
2. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Timing Waveform - Entering Sleep Mode (1,2)



Timing Waveform - Exiting Sleep Mode (1,2)



NOTES:

1. CE1 = VIH.
2. All timing is same for Left and Right ports.
3. CE0 has to be deactivated (CE0 = VIH) three cycles prior to asserting ZZ (ZZx = VIH) and held for two cycles after asserting ZZ (ZZx = VIH).
4. CE0 has to be deactivated (CE0 = VIH) one cycle prior to de-asserting ZZ (ZZx = VIL) and held for three cycles after de-asserting ZZ (ZZx = VIL).
5. The device must be in Read Mode (R/W High) when exiting sleep mode. Outputs are active but data is not valid until the following cycle.

Functional Description

The IDT70T3719/99M provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse width is independent of the cycle time.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{\text{CE}}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70T3719/99Ms for depth expansion configurations. Two cycles are required with $\overline{\text{CE}}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{\text{INT}}_\text{L}$) is asserted when the right port writes to memory location 3FFFE (HEX), where a write is defined as $\overline{\text{CE}}_\text{R}$ = R/$\overline{\text{W}}_\text{R}$ = V_{IL} per the Truth Table I. The left port clears the interrupt through access of address location 3FFFE when $\overline{\text{CE}}_\text{L}$ = V_{IL} and R/$\overline{\text{W}}_\text{L}$ = V_{IH}. Likewise, the right port interrupt flag ($\overline{\text{INT}}_\text{R}$) is asserted when the left port writes to memory location 3FFFF (HEX) and to clear the interrupt flag ($\overline{\text{INT}}_\text{R}$), the right port must read the memory location 3FFFF (1FFFF or 1FFFE for IDT70T3799M). The message (72 bits) at 3FFFE or 3FFFF (1FFFF or 1FFFE for 70T3799M) is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFFE and 3FFFF (1FFFF or 1FFFE for IDT70T3799M) are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Collision Detection

Collision is defined as an overlap in access between the two ports resulting in the potential for either reading or writing incorrect data to a specific address. For the specific cases: (a) Both ports reading - no data is corrupted, lost, or incorrectly output, so no collision flag is output on either port. (b) One port writing, the other port reading - the end result of the write will still be valid. However, the reading port might capture data that is in a state of transition and hence the reading port's collision flag is output. (c) Both ports writing - there is a risk that the two ports will interfere with each other, and the data stored in memory will not be a valid write from either port (it may essentially be a random combination of the two). Therefore, the collision flag is output on both ports. Please refer to Truth Table IV for all of the above cases.

The alert flag ($\overline{\text{COL}}_\text{X}$) is asserted on the 2nd or 3rd rising clock edge of the affected port following the collision, and remains low for one cycle. Please refer to Collision Detection Timing table on Page 19. During that next cycle, the internal arbitration is engaged in resetting the alert flag (this avoids a specific requirement on the part of the user to reset the alert flag). If two collisions occur on subsequent clock cycles, the second collision may not generate the appropriate alert flag. A third collision will generate the alert flag as appropriate. In the event that a user initiates a burst access on both ports with the same starting address on both ports and one or both ports writing during each access (i.e., imposes a long string of collisions on contiguous clock cycles), the alert flag will be asserted and cleared every other cycle. Please refer to the Collision Detection timing waveform on Page 19.

Collision detection on the IDT70T3719/99M represents a significant advance in functionality over current sync multi-ports, which have no such capability. In addition to this functionality the IDT70T3719/99M sustains the key features of bandwidth and flexibility. The collision detection function is very useful in the case of bursting data, or a string of accesses made to sequential addresses, in that it indicates a problem within the burst, giving the user the option of either repeating the burst or continuing to watch the alert flag to see whether the number of collisions increases above an acceptable threshold value. Offering this function on chip also allows users to reduce their need for arbitration circuits, typically done in CPLD's or FPGA's. This reduces board space and design complexity, and gives the user more flexibility in developing a solution.

Sleep Mode

The IDT70T3719/99M is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ (ZZ_X = V_{IH}) and three cycles after de-asserting ZZ (ZZ_X = V_{IL}), the device must be disabled via the chip enable pins. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode (R/$\overline{\text{W}}_\text{X}$ = V_{IH})when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.

Depth and Width Expansion

The IDT70T3719/99M features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70T3719/99M can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 144-bits.

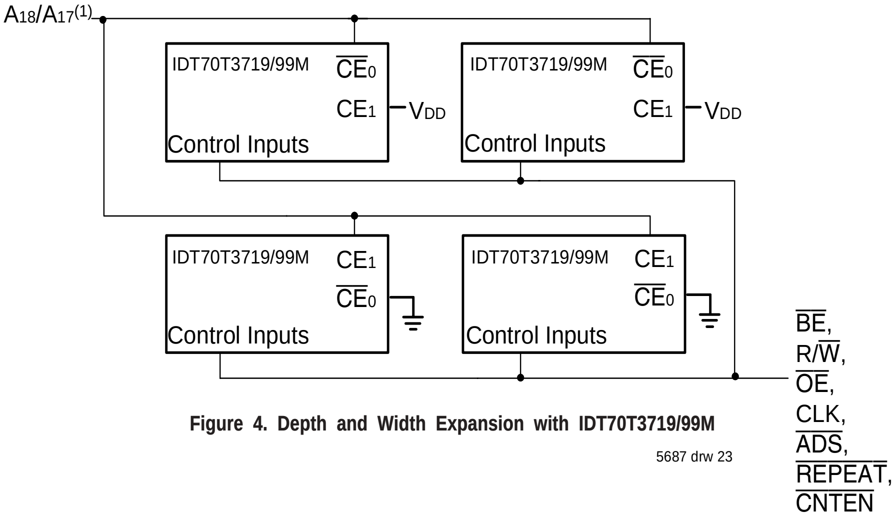


Figure 4. Depth and Width Expansion with IDT70T3719/99M

NOTE:
1. A_{18} is for IDT70T3719, A_{17} is for IDT70T3799.

JTAG Functionality and Configuration

The IDT70T3719/99M is composed of two independent memory arrays, and thus cannot be treated as a single JTAG device in the scan chain. The two arrays (A and B) each have identical characteristics and commands but must be treated as separate entities in JTAG operations. Please refer to Figure 5.

JTAG signaling must be provided serially to each array and utilize the information provided in the Identification Register Definitions, Scan Register Sizes, and System Interface Parameter tables. Specifically, commands for Array B must precede those for Array A in any JTAG operations sent to the IDT70T3719/99M. Please reference Application Note AN-411, "JTAG Testing of Multichip Modules" for specific instructions on performing JTAG testing on the IDT70T3719/99M. AN-411 is available at www.idt.com.

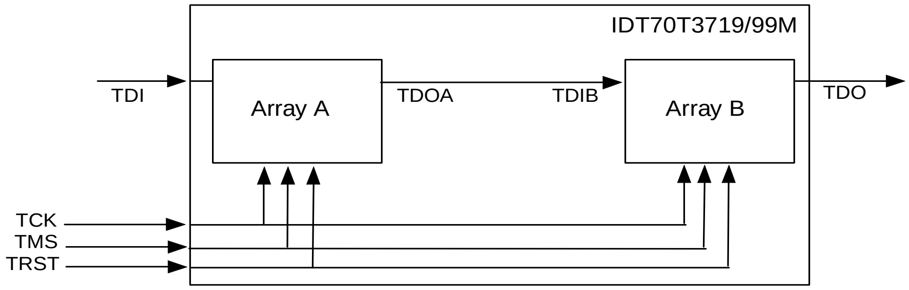


Figure 5. JTAG Configuration for IDT70T3719/99M

JTAG Timing Specifications

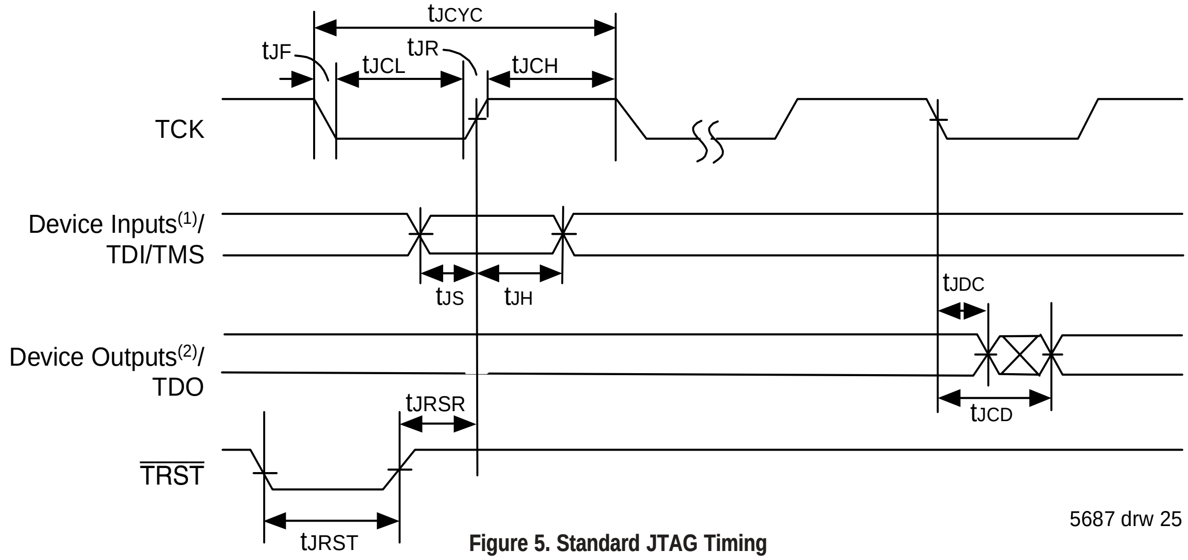


Figure 5. Standard JTAG Timing

NOTES:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics (1,2,3,4)

		70T3719/99M		
Symbol	**Parameter**	**Min.**	**Max.**	**Units**
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3(1)	ns
t_{JF}	JTAG Clock Fall Time	—	3(1)	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

5687 tbl 16

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field Array B	Value Array B	Instruction Field Array A	Value Array A	Description
Revision Number (31:28)	0x0	Revision Number (63:60)	0x0	Reserved for Version number
IDT Device ID (27:12)(1)	0x330	IDT Device ID (59:44)(1)	0x330	Defines IDT Part number
IDT JEDEC ID (11:1)	0x33	IDT JEDEC ID (43:33)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	ID Register Indicator Bit (Bit 32)	1	Indicates the presence of an ID Register

5687 tbl 17

NOTE:
1. Device ID for IDT70T3719M is 0x330. Device ID for IDT70T3799M is 0x331.

Scan Register Sizes

Register Name	Bit Size Array A	Bit Size Array B	Bit Size 70T3719M
Instruction (IR)	4	4	8
Bypass (BYR)	1	1	2
Identification (IDR)	32	32	64
Boundary Scan (BSR)	Note (3)	Note (3)	Note (3)

5687 tbl 18

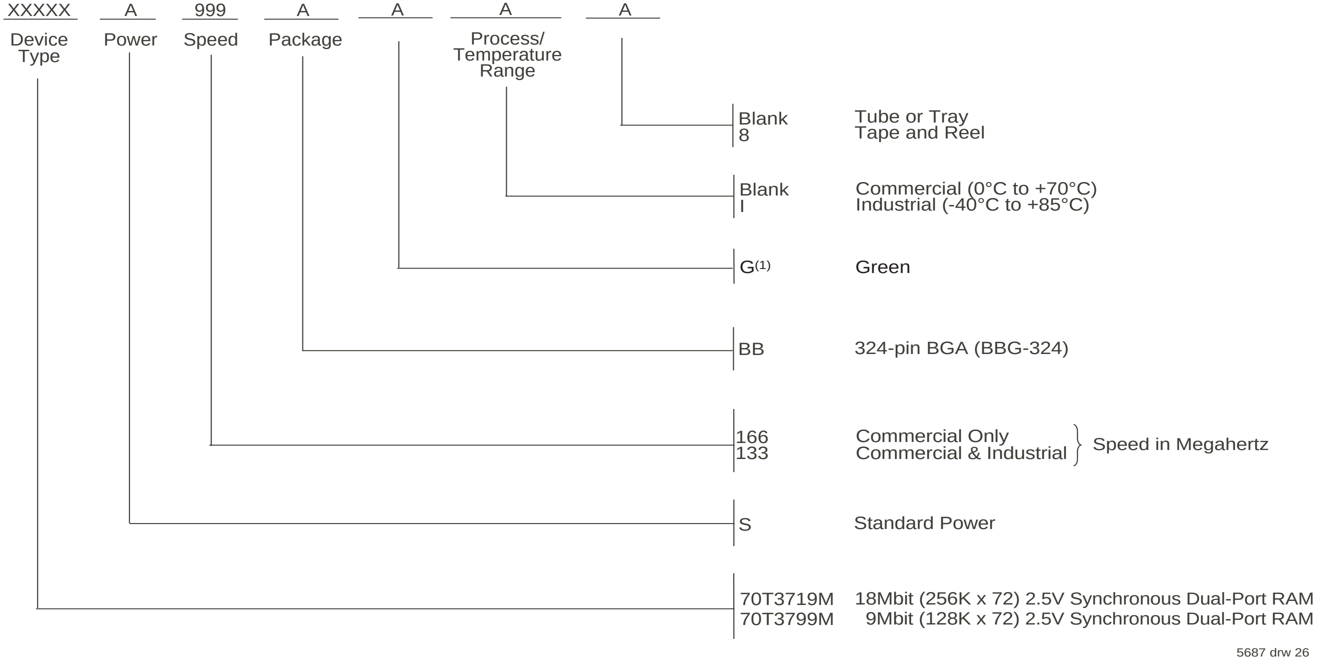
System Interface Parameters

Instruction	Code	Description
EXTEST	00000000	Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	11111111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	00100010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	01000100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers except $\overline{\text{INT}}$x and $\overline{\text{COL}}$x to a High-Z state.
CLAMP	00110011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	00010001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	01010101, 01110111, 10001000, 10011001, 10101010, 10111011, 11001100	Several combinations are reserved. Do not use codes other than those identified above.
PRIVATE	01100110,11101110, 11011101	For internal use only.

5687 tbl 19

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



NOTE:

1. Green parts available. For specific speeds, packages and powers contact your local sales office.
LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

IDT Clock Solution for IDT70T3719/99M Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specitications		Clock Specifications				IDT PLL Clock Device	IDT Non-PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
70T3719/99M	3.3/2.5	LVTTL	15pF	40%	166	75ps	5T2010	5T9010 5T905, 5T9050 5T907, 5T9070

5687 tbl 20

Datasheet Document History:

06/27/05:	Initial Datasheet	
07/11/07:	Removed Advanced status	
01/19/09:	Page 25	Removed "IDT" from orderable part number
08/06/10:	Page 3	Footnote 5 - corrected a typo in the package body and ball-pitch dimensions
07/15/14:	Page 25	Added Tape & Reel to Ordering Information
02/14/18:	Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018	

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