HIGH-SPEED 3.3V 128/64K x 36
SYNCHRONOUS DUAL-PORT STATIC RAM
WITH 3.3V OR 2.5V INTERFACE

IDT70V3599/89S

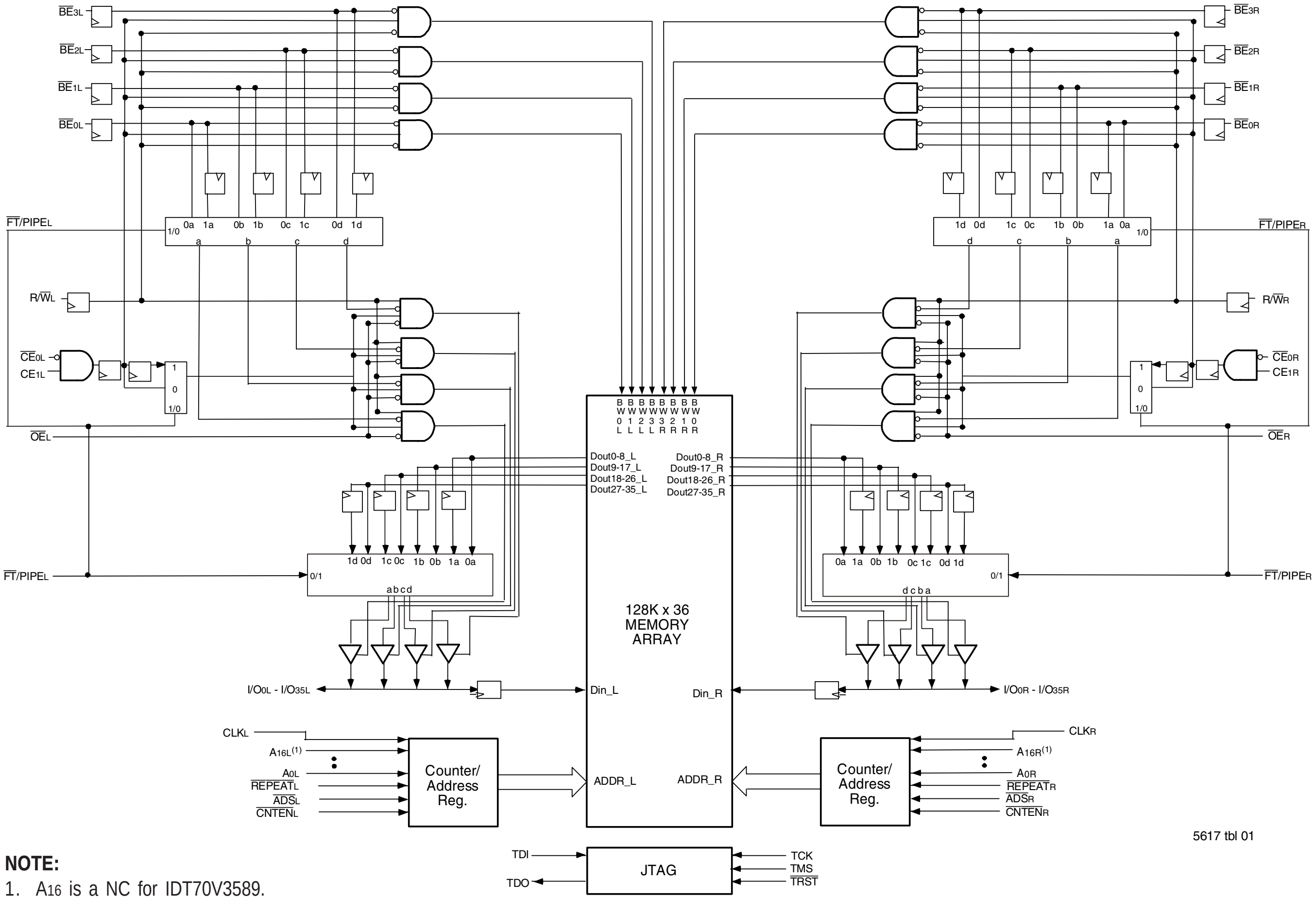
LEAD FINISH (containing SnPb) are obsolete excluding the BGA and Hermetic packages

Features:

- **True Dual-Port memory cells which allow simultaneous access of the same memory location**
- **High-speed data access**
  - *Commercial: 3.6ns (166MHz)/4.2ns (133MHz) (max.)*
  - *Industrial: 4.2ns (133MHz) (max.)*
- **Selectable Pipelined or Flow-Through output mode**
- **Counter enable and repeat features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Full synchronous operation on both ports**
  - *6ns cycle time, 166MHz operation (12Gbps bandwidth)*
  - *Fast 3.6ns clock to data out*
  - *1.7ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 166MHz*
  - *Data input, address, byte enable and control registers*
  - *Self-timed write allows fast cycle time*
- **Separate byte controls for multiplexed bus and bus matching compatibility**
- **Dual Cycle Deselect (DCD) for Pipelined Output mode**
- **LVTTL- compatible, 3.3V (±150mV) power supply for core**
- **LVTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port**
- **Industrial temperature range (-40°C to +85°C) is available at 133MHz.**
- **Available in a 208-pin Plastic Quad Flatpack (PQFP), 208-pin fine pitch Ball Grid Array (fpBGA), and 256-pin Ball Grid Array (BGA)**
- **Supports JTAG features compliant with IEEE 1149.1**
- **Green parts available, see ordering information**

Note; the information regarding recently obsoleted parts is included in this datasheet for customer convenience. Please see the Orderable Parts Table for the current, active part list.

Functional Block Diagram



NOTE:

1. A16 is a NC for IDT70V3589.

MARCH 2019

Description:

The IDT70V3599/89 is a high-speed 128/64K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3599/89 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{\text{CE}}$0 and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3599/89 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V.

Pin Configuration(1,2,3,4,5)

06/28/02

A1 IO19L	A2 IO18L	A3 VSS	A4 TDO	A5 NC	A6 A16L(1)	A7 A12L	A8 A8L	A9 $\overline{\text{BE}}$1L	A10 VDD	A11 CLKL	A12 $\overline{\text{CNTEN}}$L	A13 A4L	A14 A0L	A15 OPTL	A16 I/O17L	A17 VSS
B1 I/O20R	B2 VSS	B3 I/O18R	B4 TDI	B5 NC	B6 A13L	B7 A9L	B8 $\overline{\text{BE}}$2L	B9 $\overline{\text{CE}}$0L	B10 VSS	B11 $\overline{\text{ADS}}$L	B12 A5L	B13 A1L	B14 VSS	B15 VDDQR	B16 I/O16L	B17 I/O15R
C1 VDDQL	C2 I/O19R	C3 VDDQR	C4 PL/$\overline{\text{FT}}$L	C5 NC	C6 A14L	C7 A10L	C8 $\overline{\text{BE}}$3L	C9 CE1L	C10 VSS	C11 R/$\overline{\text{W}}$L	C12 A6L	C13 A2L	C14 VDD	C15 I/O16R	C16 I/O15L	C17 VSS
D1 I/O22L	D2 VSS	D3 I/O21L	D4 I/O20L	D5 A15L	D6 A11L	D7 A7L	D8 $\overline{\text{BE}}$0L	D9 VDD	D10 $\overline{\text{OE}}$L	D11 $\overline{\text{REPEAT}}$L	D12 A3L	D13 VDD	D14 I/O17R	D15 VDDQL	D16 I/O14L	D17 I/O14R
E1 I/O23L	E2 I/O22R	E3 VDDQR	E4 I/O21R										E14 I/O12L	E15 I/O13R	E16 VSS	E17 I/O13L
F1 VDDQL	F2 I/O23R	F3 I/O24L	F4 VSS										F14 VSS	F15 I/O12R	F16 I/O11L	F17 VDDQR
G1 I/O26L	G2 VSS	G3 I/O25L	G4 I/O24R										G14 I/O9L	G15 VDDQL	G16 I/O10L	G17 I/O11R
H1 VDD	H2 I/O26R	H3 VDDQR	H4 I/O25R										H14 VDD	H15 IO9R	H16 VSS	H17 I/O10R
J1 VDDQL	J2 VDD	J3 VSS	J4 VSS										J14 VSS	J15 VDD	J16 VSS	J17 VDDQR
K1 I/O28R	K2 VSS	K3 I/O27R	K4 VSS										K14 I/O7R	K15 VDDQL	K16 I/O8R	K17 VSS
L1 I/O29R	L2 I/O28L	L3 VDDQR	L4 I/O27L										L14 I/O6R	L15 I/O7L	L16 VSS	L17 I/O8L
M1 VDDQL	M2 I/O29L	M3 I/O30R	M4 VSS										M14 VSS	M15 I/O6L	M16 I/O5R	M17 VDDQR
N1 I/O31L	N2 VSS	N3 I/O31R	N4 I/O30L										N14 I/O3R	N15 VDDQL	N16 I/O4R	N17 I/O5L
P1 I/O32R	P2 I/O32L	P3 VDDQR	P4 I/O35R	P5 $\overline{\text{TRST}}$	P6 A16R(1)	P7 A12R	P8 A8R	P9 $\overline{\text{BE}}$1R	P10 VDD	P11 CLKR	P12 $\overline{\text{CNTEN}}$R	P13 A4R	P14 I/O2L	P15 I/O3L	P16 VSS	P17 I/O4L
R1 VSS	R2 I/O33L	R3 I/O34R	R4 TCK	R5 NC	R6 A13R	R7 A9R	R8 $\overline{\text{BE}}$2R	R9 $\overline{\text{CE}}$0R	R10 VSS	R11 $\overline{\text{ADS}}$R	R12 A5R	R13 A1R	R14 VSS	R15 VDDQL	R16 I/O1R	R17 VDDQR
T1 I/O33R	T2 I/O34L	T3 VDDQL	T4 TMS	T5 NC	T6 A14R	T7 A10R	T8 $\overline{\text{BE}}$3R	T9 CE1R	T10 VSS	T11 R/$\overline{\text{W}}$R	T12 A6R	T13 A2R	T14 VSS	T15 I/O0R	T16 VSS	T17 I/O2R
U1 VSS	U2 I/O35L	U3 PL/$\overline{\text{FT}}$R	U4 NC	U5 A15R	U6 A11R	U7 A7R	U8 $\overline{\text{BE}}$0R	U9 VDD	U10 $\overline{\text{OE}}$R	U11 $\overline{\text{REPEAT}}$R	U12 A3R	U13 A0R	U14 VDD	U15 OPTR	U16 I/O0L	U17 I/O1L

70V3599/89BF
BF-208(6)

208-Pin fpBGA
Top View(7)

5617 drw 02c

NOTES:

1. A16 is a NC for IDT70V3589.
2. All VDD pins must be connected to 3.3V power supply.
3. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
4. All VSS pins must be connected to ground supply.
5. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4,5] (con't.)

70V3599/89BC
BC-256[6]

256-Pin BGA
Top View[7]

06/28/02

A1 NC	A2 TDI	A3 NC	A4 NC	A5 A$_{14L}$	A6 A$_{11L}$	A7 A$_{8L}$	A8 $\overline{\text{BE}}_{2L}$	A9 CE$_{1L}$	A10 $\overline{\text{OE}}_{L}$	A11 $\overline{\text{CNTEN}}_{L}$	A12 A$_{5L}$	A13 A$_{2L}$	A14 A$_{0L}$	A15 NC	A16 NC
B1 I/O$_{18L}$	B2 NC	B3 TDO	B4 NC	B5 A$_{15L}$	B6 A$_{12L}$	B7 A$_{9L}$	B8 $\overline{\text{BE}}_{3L}$	B9 $\overline{\text{CE}}_{0L}$	B10 R/$\overline{\text{W}}_{L}$	B11 $\overline{\text{REPEAT}}_{L}$	B12 A$_{4L}$	B13 A$_{1L}$	B14 V$_{DD}$	B15 I/O$_{17L}$	B16 NC
C1 I/O$_{18R}$	C2 I/O$_{19L}$	C3 V$_{SS}$	C4 A$_{16L}$(1)	C5 A$_{13L}$	C6 A$_{10L}$	C7 A$_{7L}$	C8 $\overline{\text{BE}}_{1L}$	C9 $\overline{\text{BE}}_{0L}$	C10 CLK$_{L}$	C11 $\overline{\text{ADS}}_{L}$	C12 A$_{6L}$	C13 A$_{3L}$	C14 OPT$_{L}$	C15 I/O$_{17R}$	C16 I/O$_{16L}$
D1 I/O$_{20R}$	D2 I/O$_{19R}$	D3 I/O$_{20L}$	D4 PIPE/$\overline{\text{FT}}_{L}$	D5 V$_{DDQL}$	D6 V$_{DDQL}$	D7 V$_{DDQR}$	D8 V$_{DDQR}$	D9 V$_{DDQL}$	D10 V$_{DDQL}$	D11 V$_{DDQR}$	D12 V$_{DDQR}$	D13 V$_{DD}$	D14 I/O$_{15R}$	D15 I/O$_{15L}$	D16 I/O$_{16R}$
E1 I/O$_{21R}$	E2 I/O$_{21L}$	E3 I/O$_{22L}$	E4 V$_{DDQL}$	E5 V$_{DD}$	E6 V$_{DD}$	E7 V$_{SS}$	E8 V$_{SS}$	E9 V$_{SS}$	E10 V$_{SS}$	E11 V$_{DD}$	E12 V$_{DD}$	E13 V$_{DDQR}$	E14 I/O$_{13L}$	E15 I/O$_{14L}$	E16 I/O$_{14R}$
F1 I/O$_{23L}$	F2 I/O$_{22R}$	F3 I/O$_{23R}$	F4 V$_{DDQL}$	F5 V$_{DD}$	F6 V$_{SS}$	F7 V$_{SS}$	F8 V$_{SS}$	F9 V$_{SS}$	F10 V$_{SS}$	F11 V$_{SS}$	F12 V$_{DD}$	F13 V$_{DDQR}$	F14 I/O$_{12R}$	F15 I/O$_{13R}$	F16 I/O$_{12L}$
G1 I/O$_{24R}$	G2 I/O$_{24L}$	G3 I/O$_{25L}$	G4 V$_{DDQR}$	G5 V$_{SS}$	G6 V$_{SS}$	G7 V$_{SS}$	G8 V$_{SS}$	G9 V$_{SS}$	G10 V$_{SS}$	G11 V$_{SS}$	G12 V$_{SS}$	G13 V$_{DDQL}$	G14 I/O$_{10L}$	G15 I/O$_{11L}$	G16 I/O$_{11R}$
H1 I/O$_{26L}$	H2 I/O$_{25R}$	H3 I/O$_{26R}$	H4 V$_{DDQR}$	H5 V$_{SS}$	H6 V$_{SS}$	H7 V$_{SS}$	H8 V$_{SS}$	H9 V$_{SS}$	H10 V$_{SS}$	H11 V$_{SS}$	H12 V$_{SS}$	H13 V$_{DDQL}$	H14 I/O$_{9R}$	H15 IO$_{9L}$	H16 I/O$_{10R}$
J1 I/O$_{27L}$	J2 I/O$_{28R}$	J3 I/O$_{27R}$	J4 V$_{DDQL}$	J5 V$_{SS}$	J6 V$_{SS}$	J7 V$_{SS}$	J8 V$_{SS}$	J9 V$_{SS}$	J10 V$_{SS}$	J11 V$_{SS}$	J12 V$_{SS}$	J13 V$_{DDQR}$	J14 I/O$_{8R}$	J15 I/O$_{7R}$	J16 I/O$_{8L}$
K1 I/O$_{29R}$	K2 I/O$_{29L}$	K3 I/O$_{28L}$	K4 V$_{DDQL}$	K5 V$_{SS}$	K6 V$_{SS}$	K7 V$_{SS}$	K8 V$_{SS}$	K9 V$_{SS}$	K10 V$_{SS}$	K11 V$_{SS}$	K12 V$_{SS}$	K13 V$_{DDQR}$	K14 I/O$_{6R}$	K15 I/O$_{6L}$	K16 I/O$_{7L}$
L1 I/O$_{30L}$	L2 I/O$_{31R}$	L3 I/O$_{30R}$	L4 V$_{DDQR}$	L5 V$_{DD}$	L6 V$_{SS}$	L7 V$_{SS}$	L8 V$_{SS}$	L9 V$_{SS}$	L10 V$_{SS}$	L11 V$_{SS}$	L12 V$_{DD}$	L13 V$_{DDQL}$	L14 I/O$_{5L}$	L15 I/O$_{4R}$	L16 I/O$_{5R}$
M1 I/O$_{32R}$	M2 I/O$_{32L}$	M3 I/O$_{31L}$	M4 V$_{DDQR}$	M5 V$_{DD}$	M6 V$_{DD}$	M7 V$_{SS}$	M8 V$_{SS}$	M9 V$_{SS}$	M10 V$_{SS}$	M11 V$_{DD}$	M12 V$_{DD}$	M13 V$_{DDQL}$	M14 I/O$_{3R}$	M15 I/O$_{3L}$	M16 I/O$_{4L}$
N1 I/O$_{33L}$	N2 I/O$_{34R}$	N3 I/O$_{33R}$	N4 PIPE/$\overline{\text{FT}}_{R}$	N5 V$_{DDQR}$	N6 V$_{DDQR}$	N7 V$_{DDQL}$	N8 V$_{DDQL}$	N9 V$_{DDQR}$	N10 V$_{DDQR}$	N11 V$_{DDQL}$	N12 V$_{DDQL}$	N13 V$_{DD}$	N14 I/O$_{2L}$	N15 I/O$_{1R}$	N16 I/O$_{2R}$
P1 I/O$_{35R}$	P2 I/O$_{34L}$	P3 TMS	P4 A$_{16R}$(1)	P5 A$_{13R}$	P6 A$_{10R}$	P7 A$_{7R}$	P8 $\overline{\text{BE}}_{1R}$	P9 $\overline{\text{BE}}_{0R}$	P10 CLK$_{R}$	P11 $\overline{\text{ADS}}_{R}$	P12 A$_{6R}$	P13 A$_{3R}$	P14 I/O$_{0L}$	P15 I/O$_{0R}$	P16 I/O$_{1L}$
R1 I/O$_{35L}$	R2 NC	R3 $\overline{\text{TRST}}$	R4 NC	R5 A$_{15R}$	R6 A$_{12R}$	R7 A$_{9R}$	R8 $\overline{\text{BE}}_{3R}$	R9 $\overline{\text{CE}}_{0R}$	R10 R/$\overline{\text{W}}_{R}$	R11 $\overline{\text{REPEAT}}_{R}$	R12 A$_{4R}$	R13 A$_{1R}$	R14 OPT$_{R}$	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 NC	T5 A$_{14R}$	T6 A$_{11R}$	T7 A$_{8R}$	T8 $\overline{\text{BE}}_{2R}$	T9 CE$_{1R}$	T10 $\overline{\text{OE}}_{R}$	T11 $\overline{\text{CNTEN}}_{R}$	T12 A$_{5R}$	T13 A$_{2R}$	T14 A$_{0R}$	T15 NC	T16 NC

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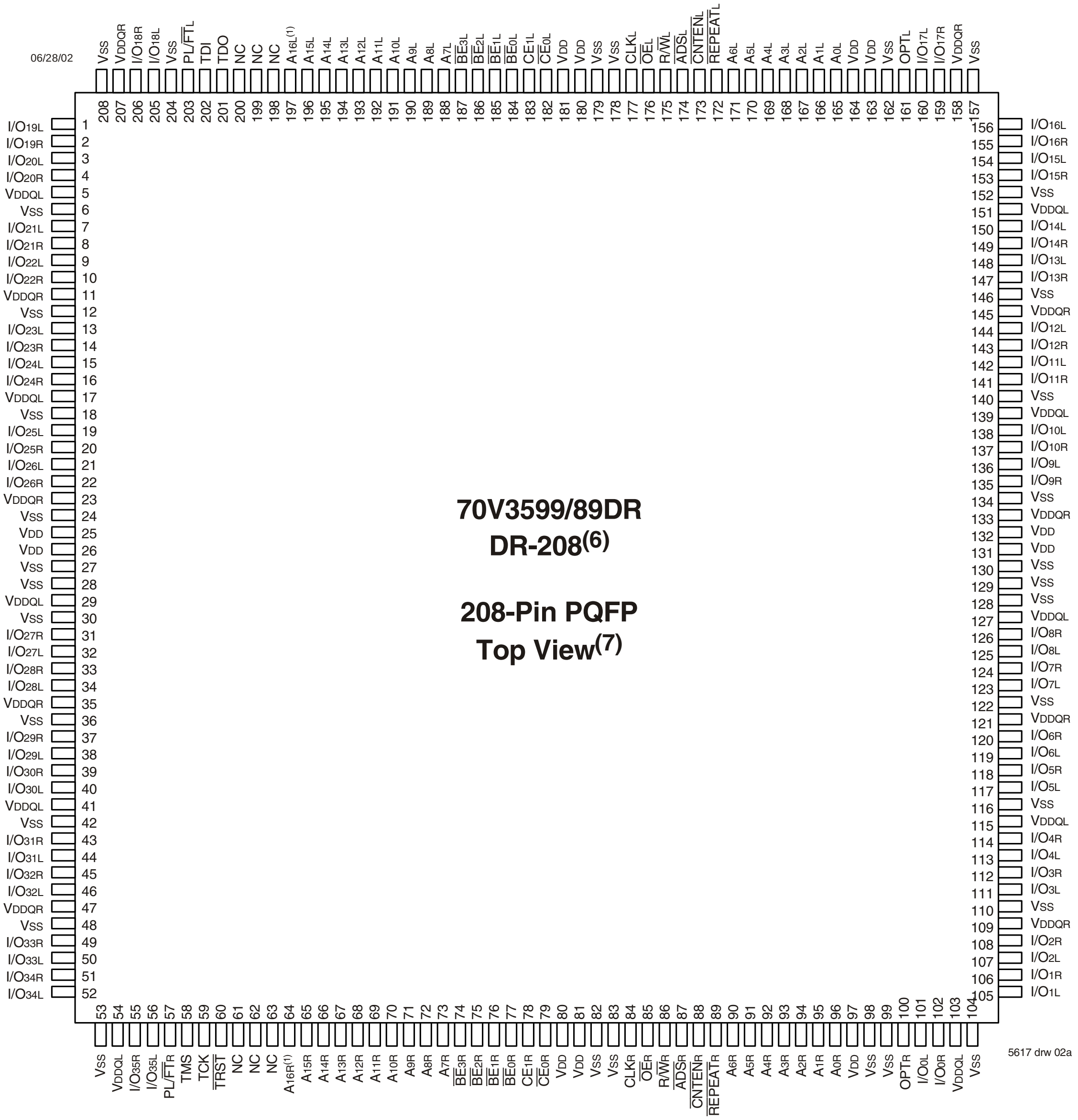
NOTES:

1. A$_{16}$ is a NC for IDT70V3589.
2. All V$_{DD}$ pins must be connected to 3.3V power supply.
3. All V$_{DDQ}$ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V$_{IH}$ (3.3V), and 2.5V if OPT pin for that port is set to V$_{IL}$ (0V).
4. All V$_{SS}$ pins must be connected to ground supply.
5. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4,5] (con't.)



NOTES:

1. A16 is a NC for IDT70V3589.
2. All VDD pins must be connected to 3.3V power supply.
3. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
4. All VSS pins must be connected to ground supply.
5. Package body is approximately 28mm x 28mm x 3.5mm.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables(5)
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{16L}(1)	A_{0R} - A_{16R}(1)	Address
I/O_{0L} - I/O_{35L}	I/O_{0R} - I/O_{35R}	Data Input/Output
CLK_L	CLK_R	Clock
$PL/\overline{FT}_L$	$PL/\overline{FT}_R$	Pipeline/Flow-Through
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat(4)
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes)(5)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)(2)
OPT_L	OPT_R	Option for selecting V_{DDQX}(2,3)
V_{DD}		Power (3.3V)(2)
V_{SS}		Ground (0V)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz)
TMS		Test Mode Select
$\overline{TRST}$		Reset (Initialize TAP Controller)

5617 tbl 01

NOTES:

1. A_{16} is a NC for IDT70V3589.
2. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
3. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to VIL (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
4. When $\overline{REPEAT}_X$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_X$.
5. Chip Enables and Byte Enables are double buffered when $PL/\overline{FT} = V_{IH}$, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control$^{(1,2,3,4)}$

$\overline{\text{OE}}$	CLK	$\overline{\text{CE}}_0$	CE$_1$	$\overline{\text{BE}}_3$	$\overline{\text{BE}}_2$	$\overline{\text{BE}}_1$	$\overline{\text{BE}}_0$	R/$\overline{\text{W}}$	Byte 3 I/O$_{27-35}$	Byte 2 I/O$_{18-26}$	Byte 1 I/O$_{9-17}$	Byte 0 I/O$_{0-8}$	MODE
X	↑	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	D$_{\text{IN}}$	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	High-Z	High-Z	D$_{\text{IN}}$	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	High-Z	D$_{\text{IN}}$	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	D$_{\text{IN}}$	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	High-Z	High-Z	D$_{\text{IN}}$	D$_{\text{IN}}$	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	D$_{\text{IN}}$	D$_{\text{IN}}$	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	D$_{\text{IN}}$	D$_{\text{IN}}$	D$_{\text{IN}}$	D$_{\text{IN}}$	Write to All Bytes
L	↑	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	D$_{\text{OUT}}$	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	High-Z	High-Z	D$_{\text{OUT}}$	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	High-Z	D$_{\text{OUT}}$	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	D$_{\text{OUT}}$	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	High-Z	High-Z	D$_{\text{OUT}}$	D$_{\text{OUT}}$	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	D$_{\text{OUT}}$	D$_{\text{OUT}}$	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	D$_{\text{OUT}}$	D$_{\text{OUT}}$	D$_{\text{OUT}}$	D$_{\text{OUT}}$	Read All Bytes
H	↑	L	H	L	L	L	L	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

5617 tbl 02

NOTES:

1. "H" = V$_{\text{IH}}$, "L" = V$_{\text{IL}}$, "X" = Don't Care.
2. $\overline{\text{ADS}}$, $\overline{\text{CNTEN}}$, $\overline{\text{REPEAT}}$ = X.
3. $\overline{\text{OE}}$ is an asynchronous input signal.
4. It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

Truth Table II—Address Counter Control$^{(1,2)}$

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{\text{ADS}}$	$\overline{\text{CNTEN}}$	$\overline{\text{REPEAT}}^{(6)}$	I/O$^{(3)}$	MODE
X	X	An	↑	X	X	L$^{(4)}$	D$_{\text{I/O}}$(0)	Counter Reset to last valid $\overline{\text{ADS}}$ load
An	X	An	↑	L$^{(4)}$	X	H	D$_{\text{I/O}}$ (n)	External Address Used
An	Ap	Ap	↑	H	H	H	D$_{\text{I/O}}$(p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L$^{(5)}$	H	D$_{\text{I/O}}$(p+1)	Counter Enabled—Internal Address generation

5617 tbl 03

NOTES:

1. "H" = V$_{\text{IH}}$, "L" = V$_{\text{IL}}$, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{\text{W}}$, $\overline{\text{CE}}_0$, CE$_1$, $\overline{\text{BE}}$n and $\overline{\text{OE}}$.
3. Outputs configured in flow-through output mode: if outputs are in pipelined mode the date out will be delayed by one cycle.
4. $\overline{\text{ADS}}$ and $\overline{\text{REPEAT}}$ are independent of all other memory control signals including $\overline{\text{CE}}_0$, CE$_1$ and $\overline{\text{BE}}$n
5. The address counter advances if $\overline{\text{CNTEN}}$ = V$_{\text{IL}}$ on the rising edge of CLK, regardless of all other memory control signals including $\overline{\text{CE}}_0$, CE$_1$, $\overline{\text{BE}}$n.
6. When $\overline{\text{REPEAT}}$ is asserted, the counter will reset to the last valid address loaded via $\overline{\text{ADS}}$. This value is not set at power-up: a known location should be loaded via $\overline{\text{ADS}}$ during initialization if desired. Any subsequent $\overline{\text{ADS}}$ access during operations will update the $\overline{\text{REPEAT}}$ address location.

Recommended Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

5617 tbl 04

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}[3]	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	50	mA

5617 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 150mV.
3. Ambient Temperature Under Bias. No AC Conditions. Chip Deselected.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage[3]	2.4	2.5	2.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address & Control Inputs)	1.7	—	V_{DDQ} + 100mV[2]	V
V_{IH}	Input High Voltage - I/O[3]	1.7	—	V_{DDQ} + 100mV[2]	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.7	V

5617 tbl 05a

NOTES:
1. Undershoot of $V_{IL} \geq$ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 100mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage[3]	3.15	3.3	3.45	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address & Control Inputs)[3]	2.0	—	V_{DDQ} + 150mV[2]	V
V_{IH}	Input High Voltage - I/O[3]	2.0	—	V_{DDQ} + 150mV[2]	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

5617 tbl 05b

NOTES:
1. Undershoot of $V_{IL} \geq$ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance(1)
(T_A = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}(3)	Output Capacitance	V_{OUT} = 3dV	10.5	pF

5617 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3599/89S		Unit
			Min.	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current(1)	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\lvert I_{LO}\rvert$	Output Leakage Current(1)	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage(2)	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage(2)	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage(2)	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage(2)	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

5617 tbl 08

NOTE:
1. At $V_{DD} \leq 2.0V$ leakages are undefined.
2. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(3) (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Condition	Version		70V3599/89S166 Com'l Only		70V3599/89S133 Com'l & Ind		Unit
					Typ.(4)	Max.	Typ.(4)	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}(1)	COM'L	S	370	500	320	400	mA
			IND	S	—	—	320	480	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}, Outputs Disabled, f = f_{MAX}(1)	COM'L	S	125	200	115	160	mA
			IND	S	—	—	115	195	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(1)	COM'L	S	250	350	220	290	mA
			IND	S	—	—	220	350	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports Outputs Disabled $\overline{CE}_L$ and $\overline{CE}_R$ $\geq$ V_{DDQ} - 0.2V, V_{IN} $\geq$ V_{DDQ} - 0.2V or V_{IN} $\leq$ 0.2V, f = 0(2)	COM'L	S	15	30	15	30	mA
			IND	S	—	—	15	40	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ $\leq$ 0.2V and $\overline{CE}_{"B"}$ $\geq$ V_{DDQ} - 0.2V(5) V_{IN} $\geq$ V_{DDQ} - 0.2V or V_{IN} $\leq$ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}(1)	COM'L	S	250	350	220	290	mA
			IND	S	—	—	220	350	

5617 tbl 09

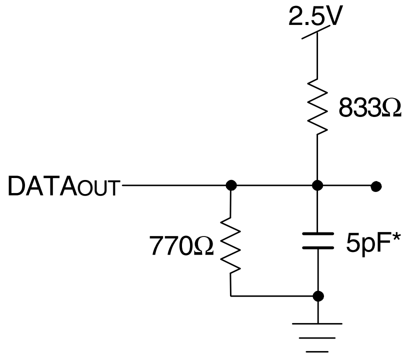
NOTES:

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. **I_{DD} DC**(f=0) = 120mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ $\leq$ 0.2V means $\overline{CE}_{0X}$ $\leq$ 0.2V and CE_{1X} $\geq$ V_{DDQ} - 0.2V
   $\overline{CE}_X$ $\geq$ V_{DDQ} - 0.2V means $\overline{CE}_{0X}$ $\geq$ V_{DDQ} - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.

AC Test Conditions (VDDQ - 3.3V/2.5V)

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

5617 tbl 10



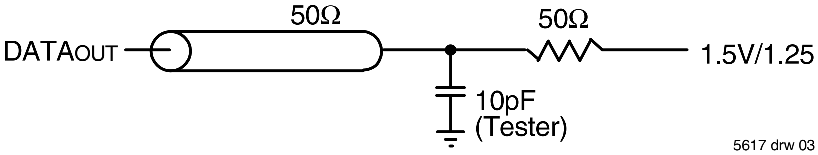


Figure 1. AC Output Test load.

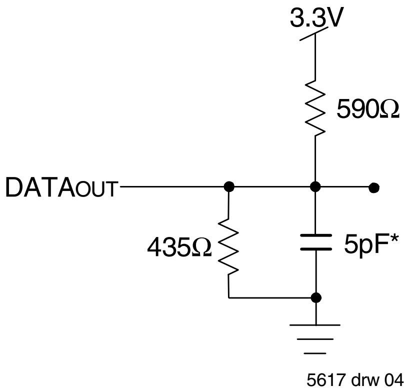


Figure 2. Output Test Load
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).
*Including scope and jig.

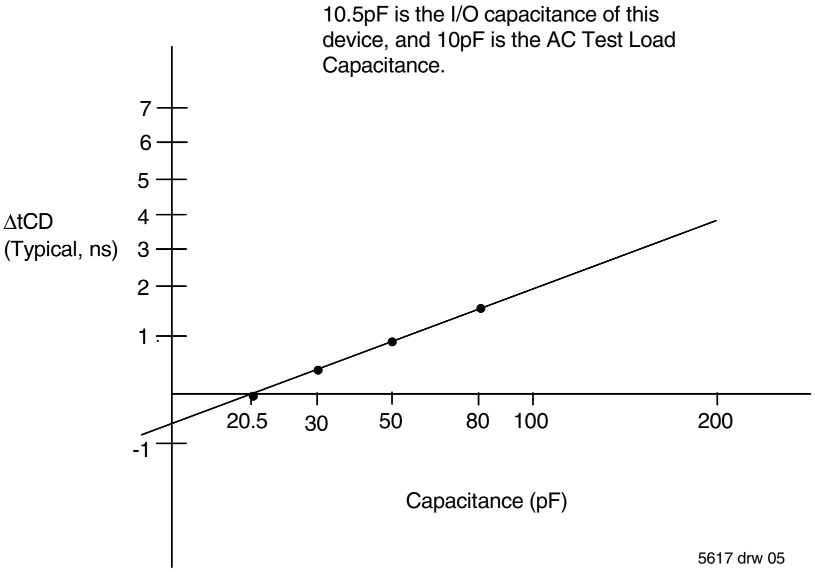


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)(2,3) (V_{DD} = 3.3V ± 150mV)

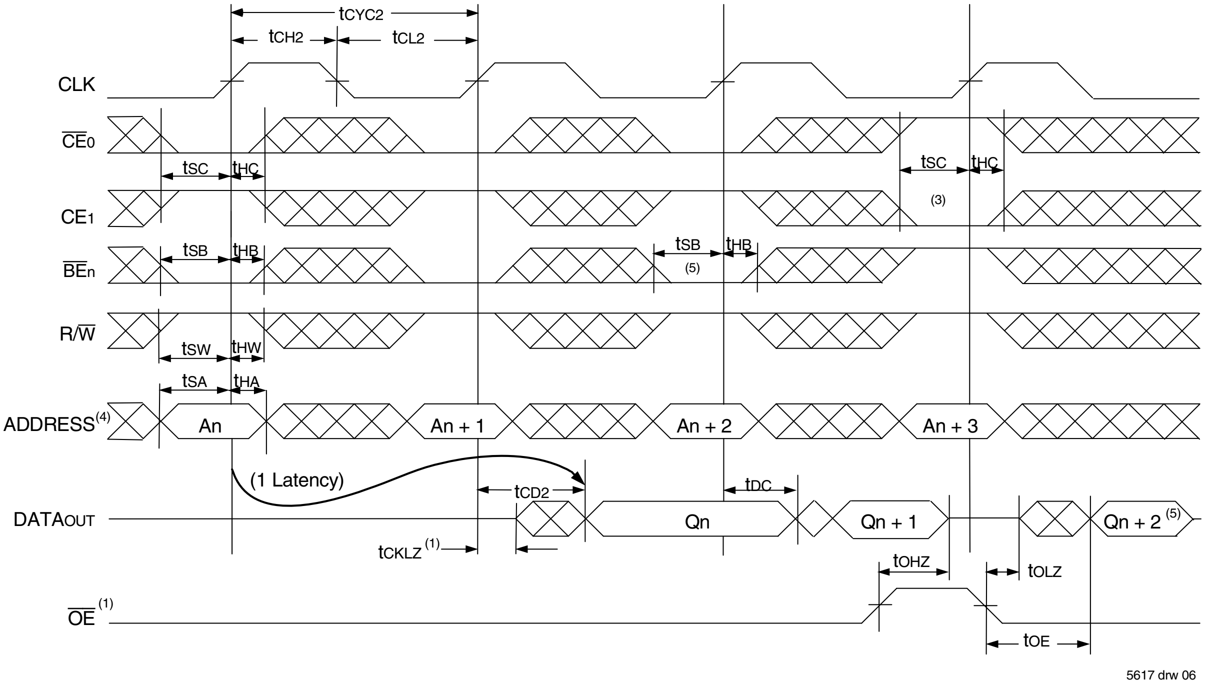
		70V3599/89S166 Com'l Only		70V3599/89S133 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{CYC1}	Clock Cycle Time (Flow-Through)(1)	20	—	25	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)(1)	6	—	7.5	—	ns
t_{CH1}	Clock High Time (Flow-Through)(1)	6	—	7	—	ns
t_{CL1}	Clock Low Time (Flow-Through)(1)	6	—	7	—	ns
t_{CH2}	Clock High Time (Pipelined)(2)	2.1	—	2.6	—	ns
t_{CL2}	Clock Low Time (Pipelined)(1)	2.1	—	2.6	—	ns
t_{SA}	Address Setup Time	1.7	—	1.8	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	ns
t_{SC}	Chip Enable Setup Time	1.7	—	1.8	—	ns
t_{HC}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{SB}	Byte Enable Setup Time	1.7	—	1.8	—	ns
t_{HB}	Byte Enable Hold Time	0.5	—	0.5	—	ns
t_{SW}	R/W Setup Time	1.7	—	1.8	—	ns
t_{HW}	R/W Hold Time	0.5	—	0.5	—	ns
t_{SD}	Input Data Setup Time	1.7	—	1.8	—	ns
t_{HD}	Input Data Hold Time	0.5	—	0.5	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	1.7	—	1.8	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	1.7	—	1.8	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	ns
t_{SRPT}	$\overline{REPEAT}$ Setup Time	1.7	—	1.8	—	ns
t_{HRPT}	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	ns
t_{OE}	Output Enable to Data Valid	—	4.0	—	4.2	ns
t_{OLZ}	Output Enable to Output Low-Z	1	—	1	—	ns
t_{OHZ}	Output Enable to Output High-Z	1	3.6	1	4.2	ns
t_{CD1}	Clock to Data Valid (Flow-Through)(1)	—	12	—	15	ns
t_{CD2}	Clock to Data Valid (Pipelined)(1)	—	3.6	—	4.2	ns
t_{DC}	Data Output Hold After Clock High	1	—	1	—	ns
t_{CKHZ}	Clock High to Output High-Z	1	3	1	3	ns
t_{CKLZ}	Clock High to Output Low-Z	1	—	1	—	ns
Port-to-Port Delay						
t_{CO}	Clock-to-Clock Offset	5	—	6	—	ns

5617 tbl 11

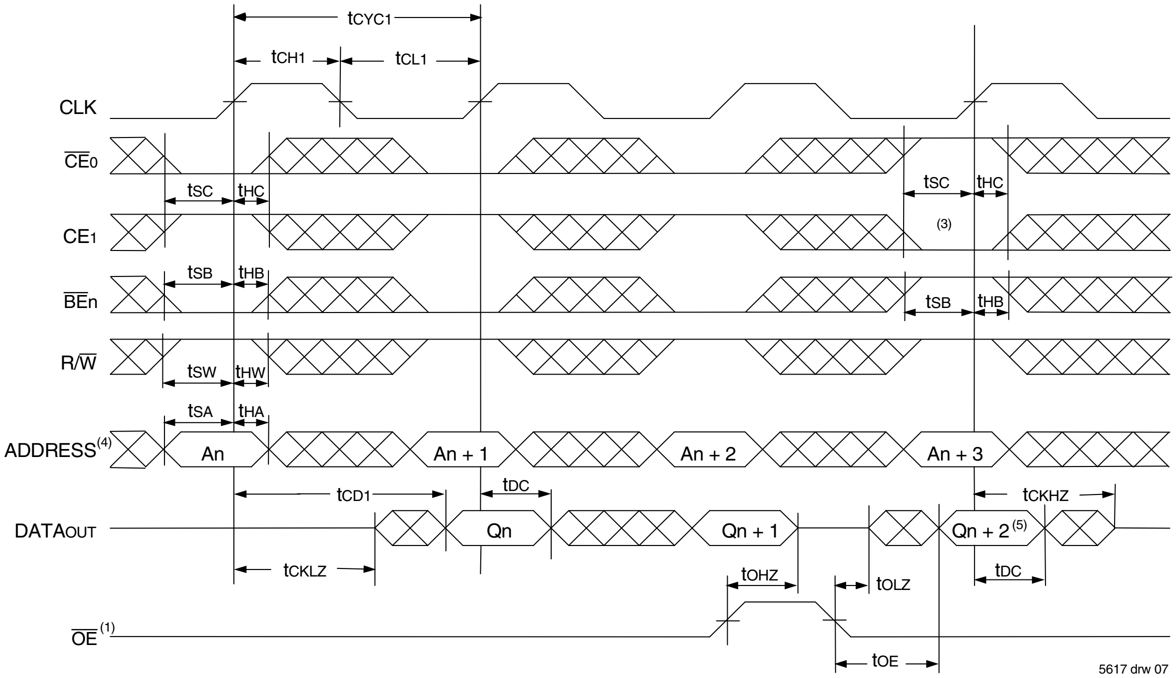
NOTES:

1. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPE$_X$ = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPE. $\overline{FT}$/PIPE should be treated as a DC signal, i.e. steady state during operation.
3. These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 5 for details on selecting the desired operating voltage levels for each port.

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{\text{FT}}$/PIPE'X' = V_{IH})$^{(2)}$



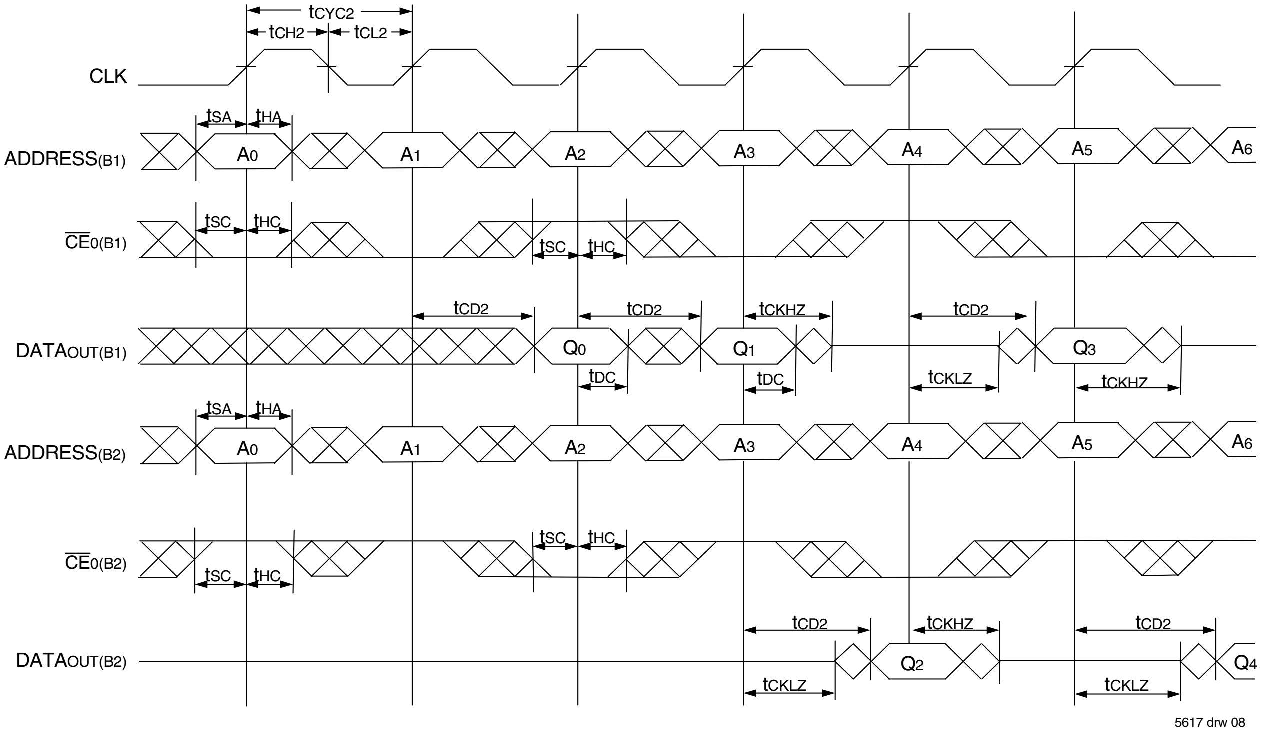
Timing Waveform of Read Cycle for Flow-through Output ($\overline{\text{FT}}$/PIPE"X" = V_{IL})$^{(2,6)}$



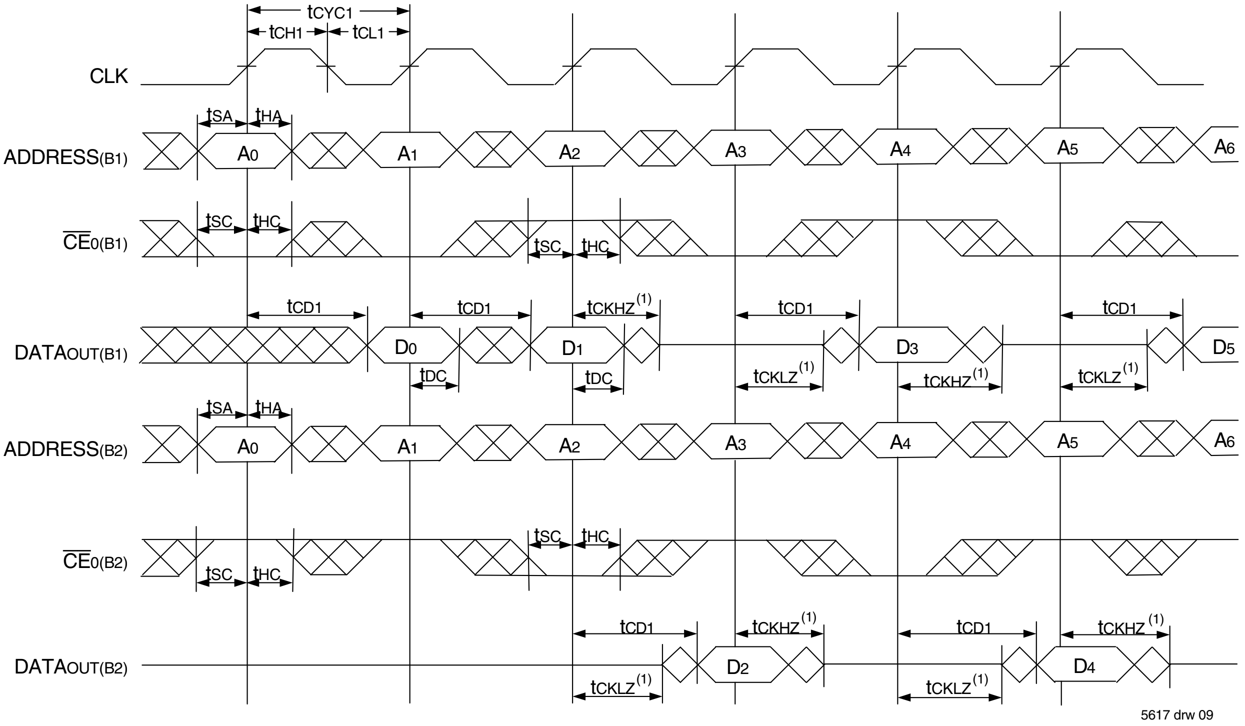
NOTES:

1. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{\text{ADS}}$ = V_{IL} and $\overline{\text{REPEAT}}$ = V_{IH}.
3. The output is disabled (High-Impedance state) by $\overline{\text{CE}}_0$ = V_{IH}, CE_1 = V_{IL}, $\overline{\text{BE}}_n$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{\text{BE}}_n$ was HIGH, then the appropriate Byte of DATA_{OUT} for Qn + 2 would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read(1,2)



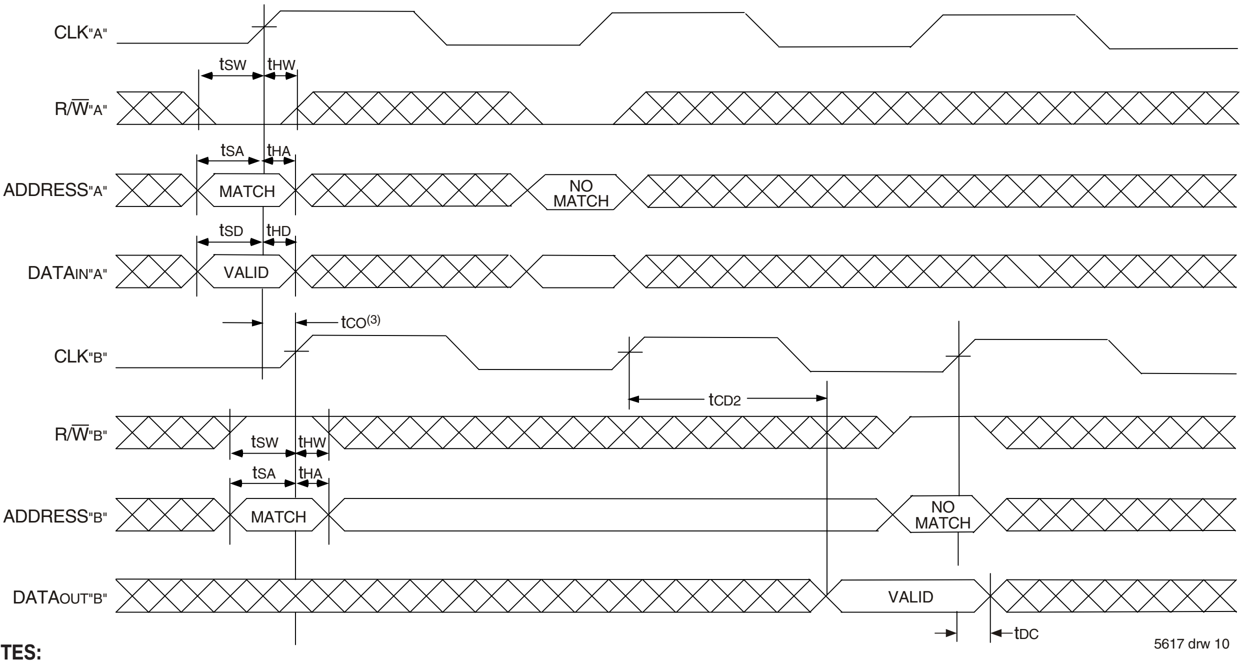
Timing Waveform of a Multi-Device Flow-Through Read(1,2)



NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3599/89 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{BE}_n$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$ and $\overline{REPEAT}$ = V_{IH}.

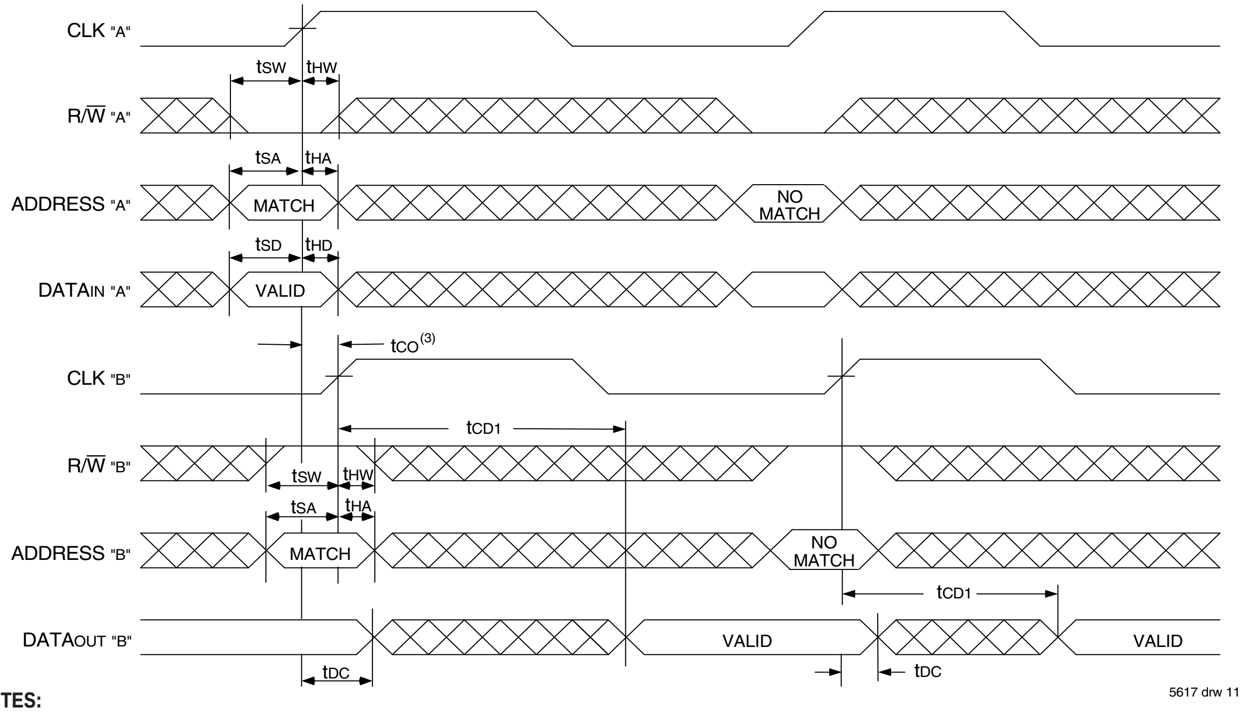
Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2,4)



NOTES:

1. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port "B", which is being read from. $\overline{OE}$ = V_{IH} for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be t_{CO} + 2 t_{CYC2} + t_{CD2}). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be t_{CO} + t_{CYC2} + t_{CD2}).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

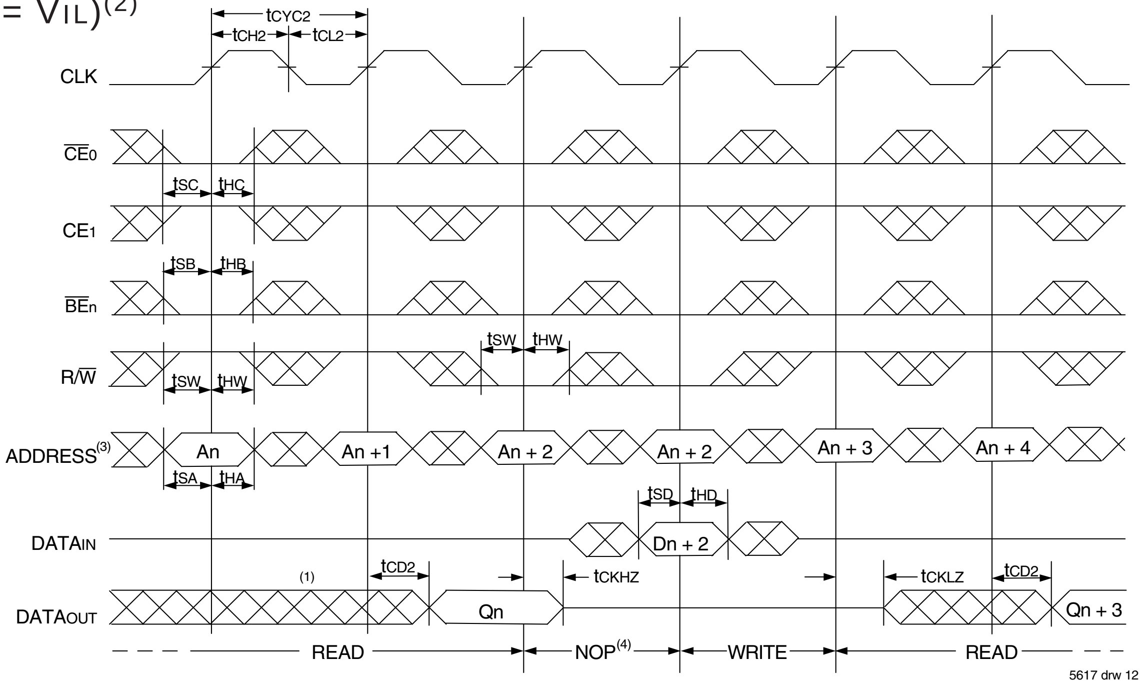
Timing Waveform with Port-to-Port Flow-Through Read(1,2,4)



NOTES:

1. $\overline{CE}_0$, $\overline{BE}$n, and $\overline{ADS}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be t_{CO} + t_{CYC} + t_{CD1}). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be t_{CO} + t_{CD1}).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

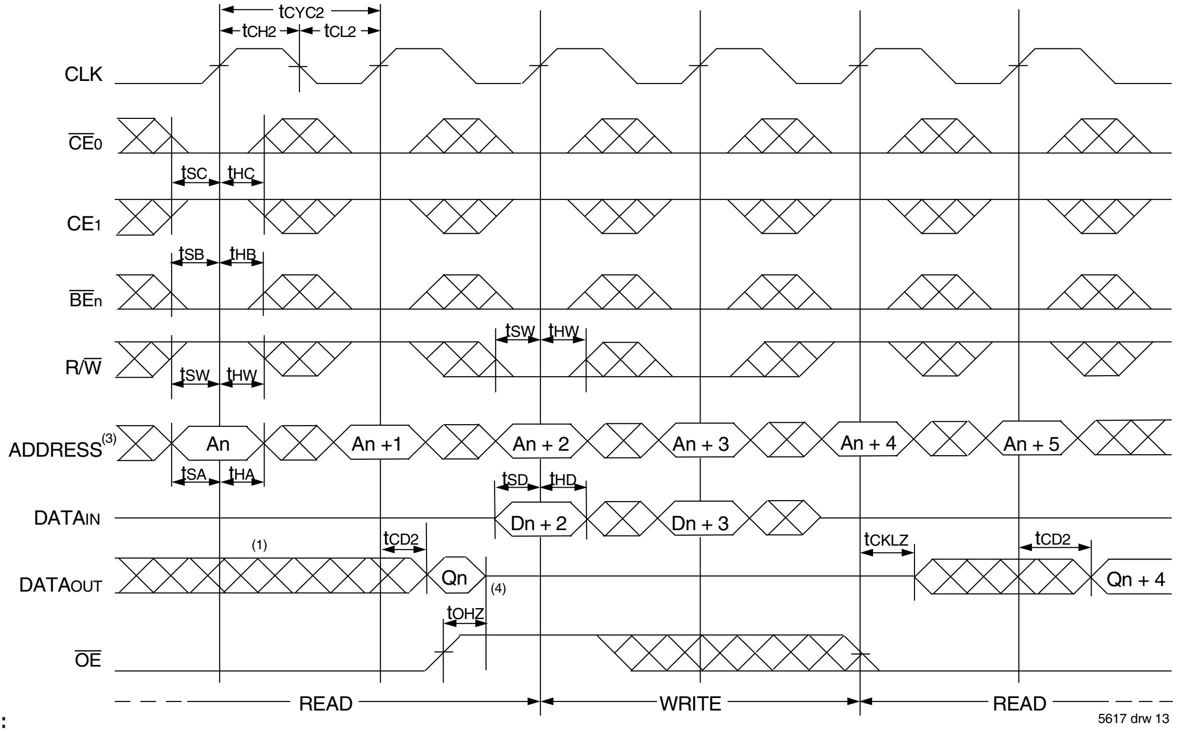
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})(2)



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

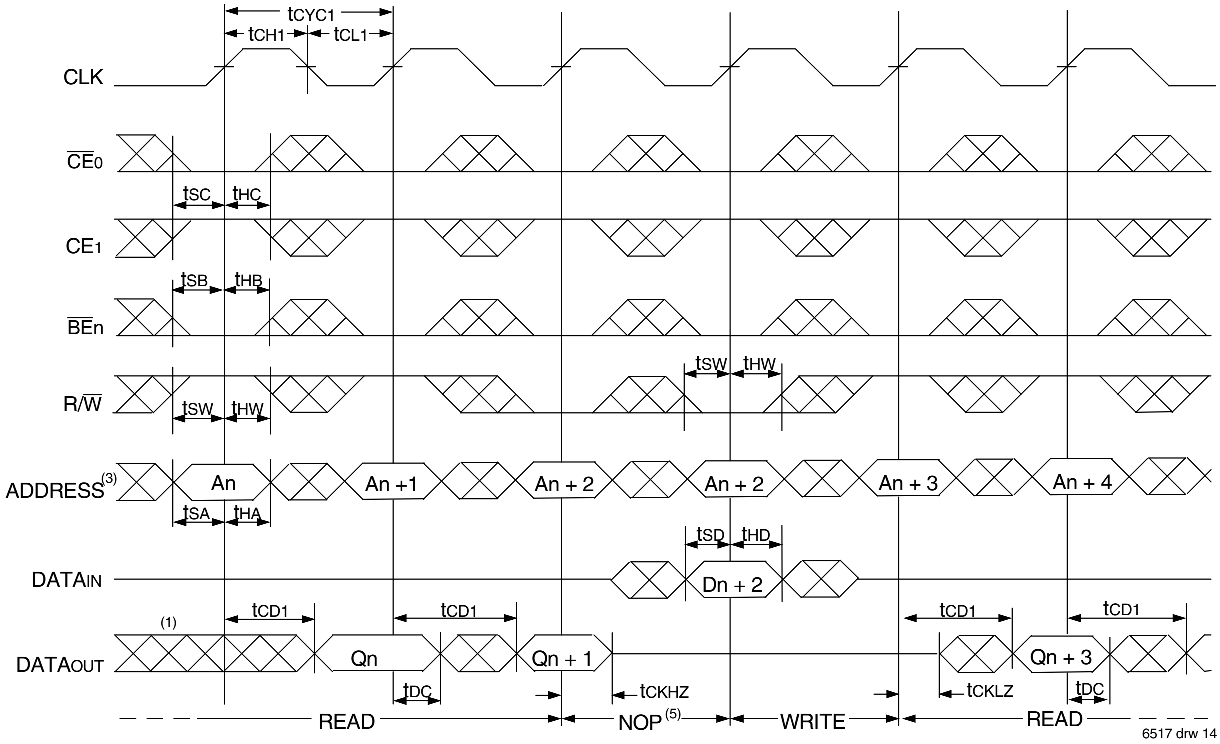
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)



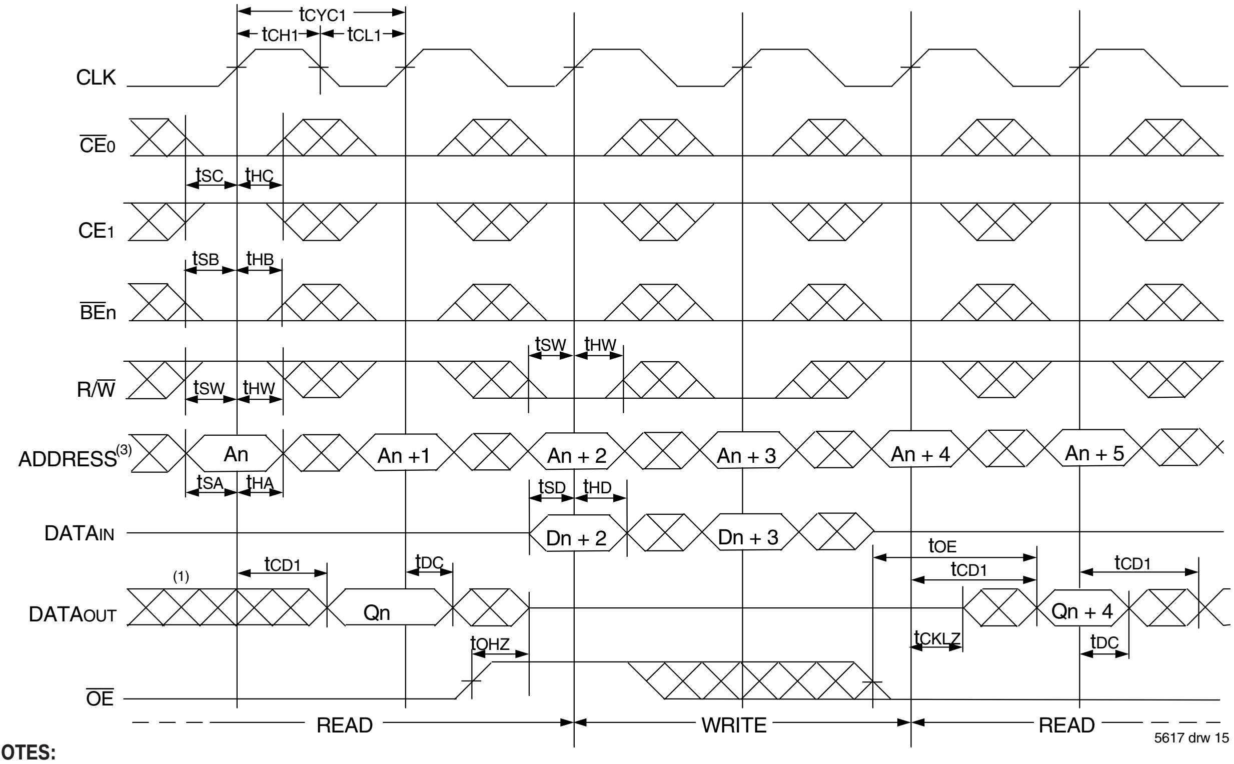
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{\text{OE}}$ = V_{IL})$^{(2)}$



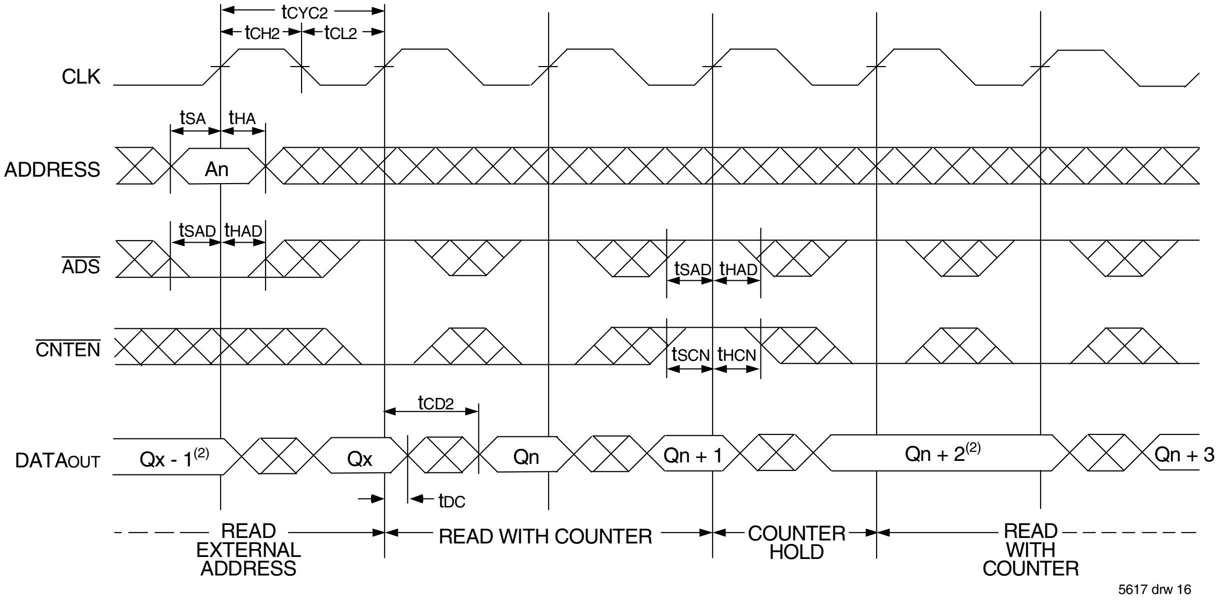
Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{\text{OE}}$ Controlled)$^{(2)}$



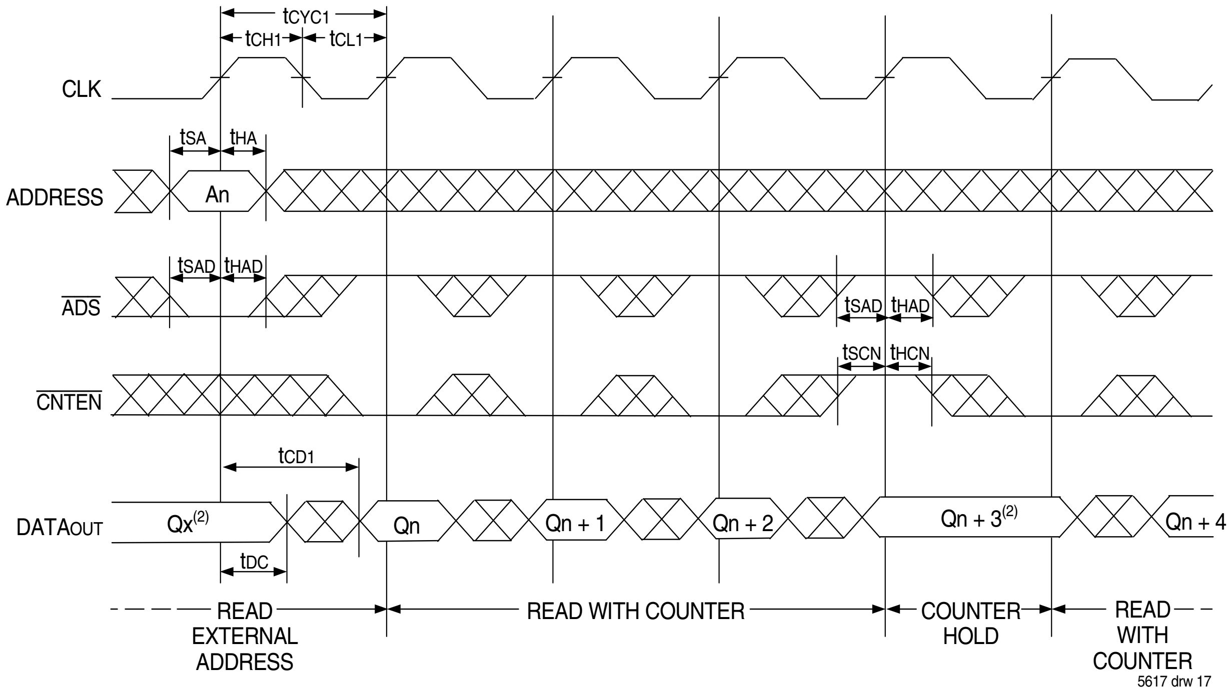
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{\text{CE}}_0$, $\overline{\text{BE}}$n, and $\overline{\text{ADS}}$ = V_{IL}; CE_1 and $\overline{\text{REPEAT}}$ = V_{IH}.
3. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance[(1)]



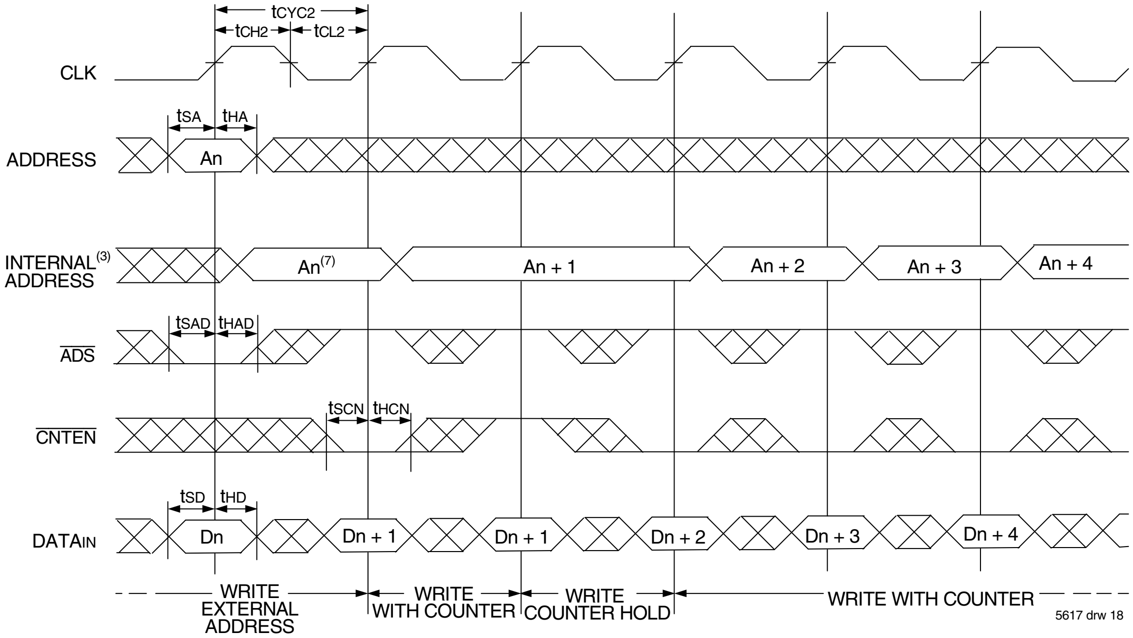
Timing Waveform of Flow-Through Read with Address Counter Advance[(1)]



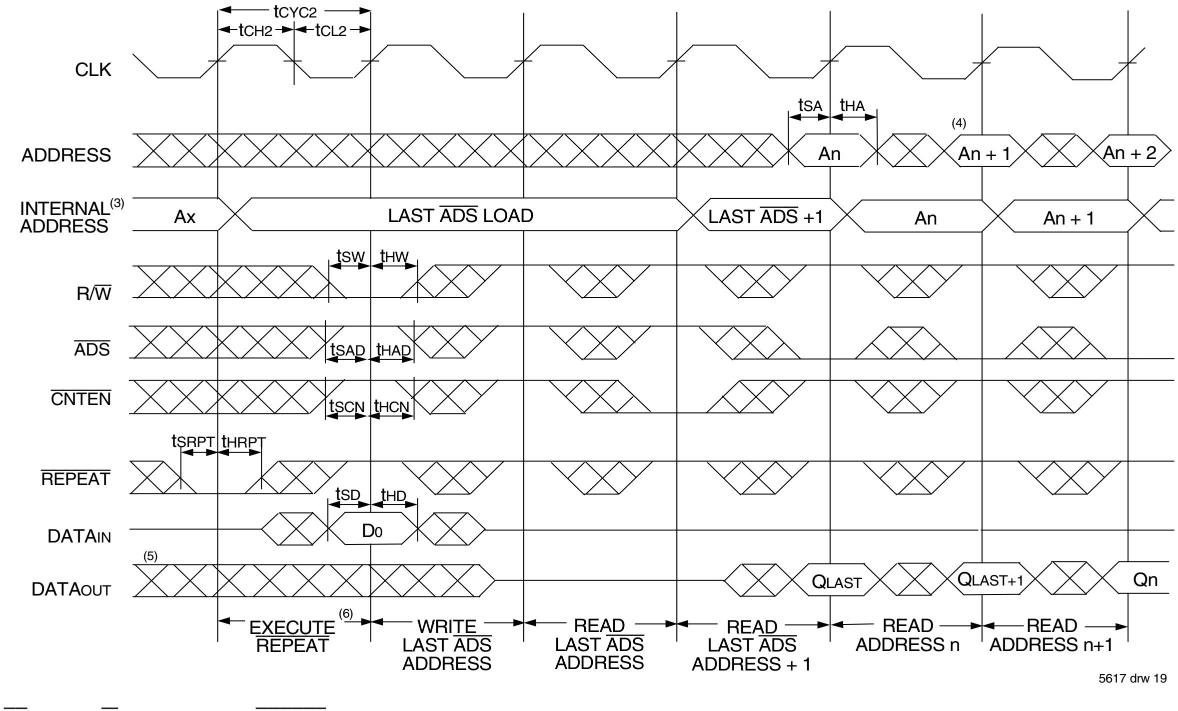
NOTES:

1. $\overline{\text{CE}}_0$, $\overline{\text{OE}}$, $\overline{\text{BE}}n = V_{IL}$; CE_1, R/$\overline{\text{W}}$, and $\overline{\text{REPEAT}} = V_{IH}$.
2. If there is no address change via $\overline{\text{ADS}} = V_{IL}$ (loading a new address) or $\overline{\text{CNTEN}} = V_{IL}$ (advancing the address), i.e. $\overline{\text{ADS}} = V_{IH}$ and $\overline{\text{CNTEN}} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)(1)



Timing Waveform of Counter Repeat(2)



NOTES:

1. $\overline{CE}_0$, $\overline{BE}_n$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{CE}_0$, $\overline{BE}_n$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during $\overline{REPEAT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{REPEAT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. Extra cycles are shown here simply for clarification. For more information on $\overline{REPEAT}$ function refer to Truth Table II.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

Functional Description

The IDT70V3599/89 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3599/89s for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V3599/89 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3599/89 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

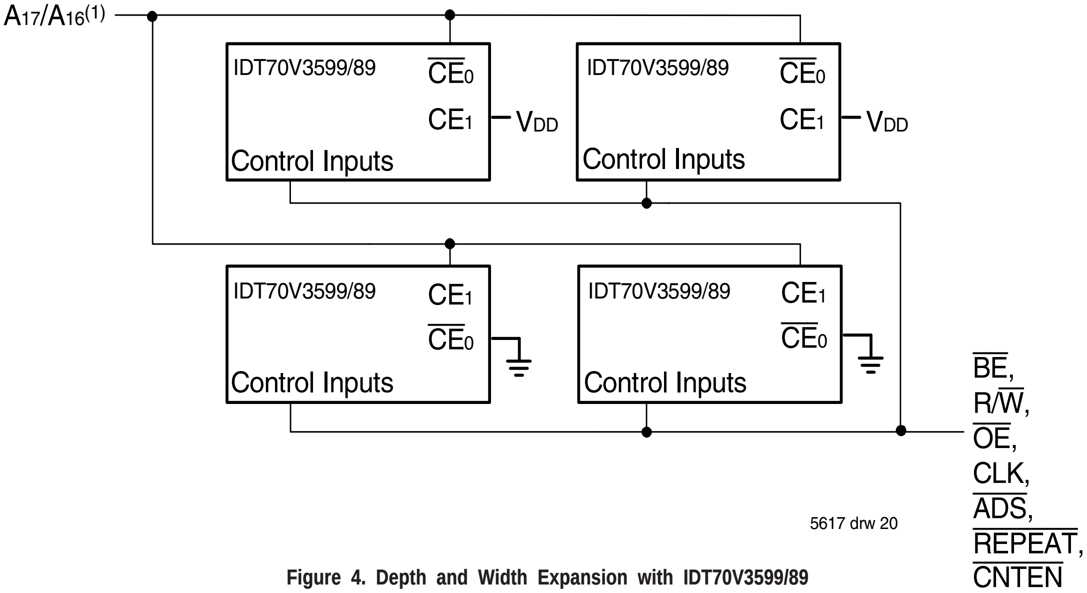


Figure 4. Depth and Width Expansion with IDT70V3599/89

NOTE:

1. A_{17} is for IDT70V3599, A_{16} is for IDT70V3589.

JTAG Timing Specifications

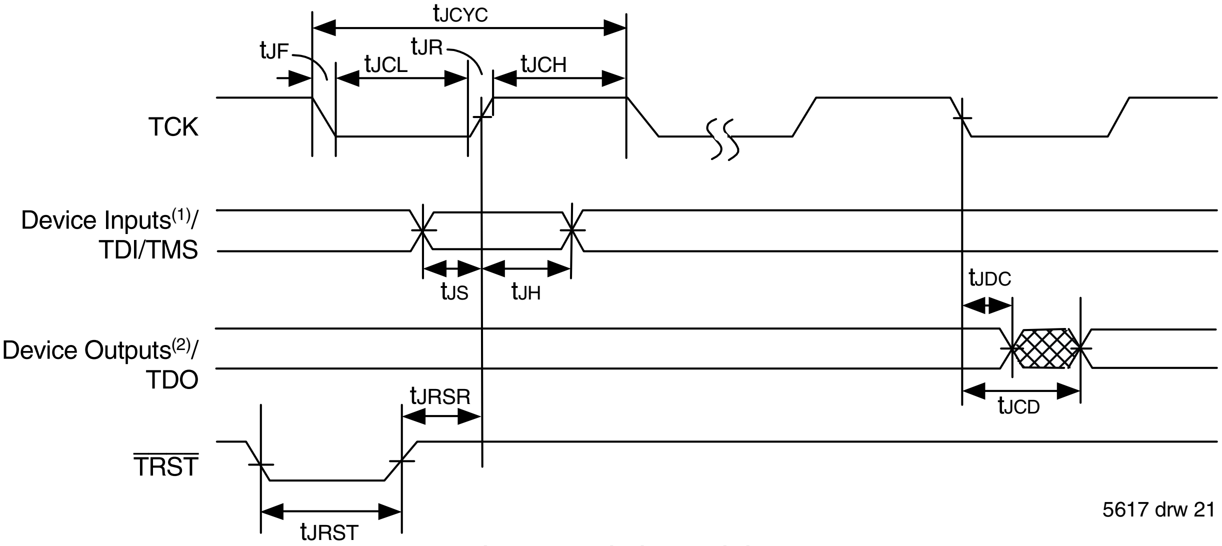


Figure 5. Standard JTAG Timing

NOTES:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics(1,2,3,4)

Symbol	Parameter	70V3599/89		
		Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3(1)	ns
t_{JF}	JTAG Clock Fall Time	—	3(1)	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

5617 tbl 12

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x0312(1)	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5617 tbl 13

NOTE:

1. Device ID for IDT70V3589 is 0x0313.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5617 tbl 14

System Interface Parameters

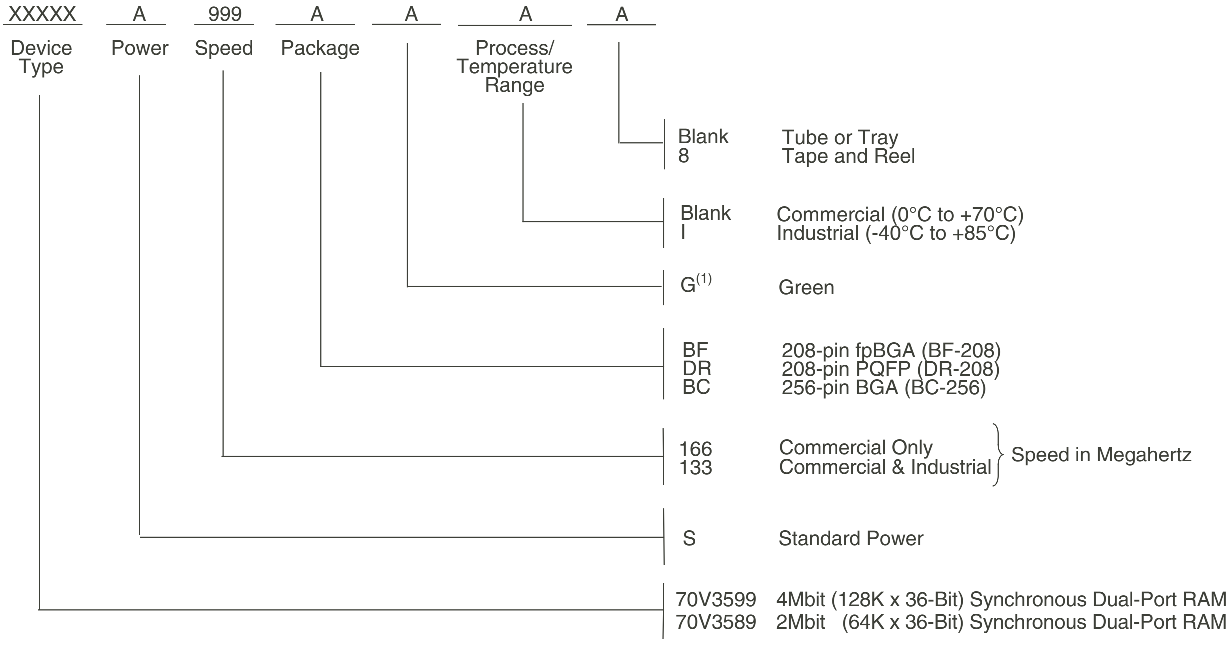
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0011	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

5617 tbl 15

NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



5617 drw 22

NOTE:

1. Green parts available. For specific speeds, packages and powers contact your local sales office.
   LEAD FINISH (containing SnPb) are obsolete excluding BGA and Hermetic packages.
   Note; the information regarding recently obsoleted parts is included in this datasheet for customer convenience. Please see the Orderable Parts Table for the current, active part list.

ORDERABLE PART INFORMATION

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
133	70V3599S133BC	BC256	CABGA	C
	70V3599S133BC8	BC256	CABGA	C
	70V3599S133BCGI	BCG256	CABGA	I
	70V3599S133BCI	BC256	CABGA	I
	70V3599S133BCI8	BC256	CABGA	I
	70V3599S133BF	BF208	CABGA	C
	70V3599S133BF8	BF208	CABGA	C
	70V3599S133BFGI	BFG208	CABGA	I
	70V3599S133BFGI8	BFG208	CABGA	I
	70V3599S133BFI	BF208	CABGA	I
	70V3599S133BFI8	BF208	CABGA	I
	70V3599S133DRGI	DRG208	PQFP	I
166	70V3599S166BC	BC256	CABGA	C
	70V3599S166BC8	BC256	CABGA	C
	70V3599S166BCG	BCG256	CABGA	C
	70V3599S166BF	BF208	CABGA	C
	70V3599S166BF8	BF208	CABGA	C
	70V3599S166BFG	BFG208	CABGA	C
	70V3599S166BFG8	BFG208	CABGA	C
	70V3599S166DRG	DRG208	PQFP	C

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
133	70V3589S133BC	BC256	CABGA	C
	70V3589S133BC8	BC256	CABGA	C
	70V3589S133BCI	BC256	CABGA	I
	70V3589S133BCI8	BC256	CABGA	I
	70V3589S133BF	BF208	CABGA	C
	70V3589S133BF8	BF208	CABGA	C
	70V3589S133BFI	BF208	CABGA	I
	70V3589S133BFI8	BF208	CABGA	I
	70V3589S133DRG	DRG208	PQFP	C
	70V3589S133DRGI	DRG208	PQFP	I
166	70V3589S166BC	BC256	CABGA	C
	70V3589S166BC8	BC256	CABGA	C
	70V3589S166BCG	BCG256	CABGA	C
	70V3589S166BF	BF208	CABGA	C
	70V3589S166BF8	BF208	CABGA	C
	70V3589S166BFG	BFG208	CABGA	C
	70V3589S166BFG8	BFG208	CABGA	C
	70V3589S166DRG	DRG208	PQFP	C

IDT Clock Solution for IDT70V3599/89 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specitications		Clock Specifications				IDT PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance	
70V3599/89	3.3/2.5	LVTTL	8pF	40%	166	75ps	IDT5V2528

5617 tbl16a

Datasheet Document History:

06/02/00:		Initial Public Offering
07/12/00:		Added mux to functional block diagram
07/30/01:	Page 20	Changed maximum value for JTAG AC Electrical Characteristics for t_{JCD} from 20ns to 25ns
	Page 9	Added Industrial Temperature DC Parameters
11/20/01:	Pages 2, 3 & 4	Added date revision for pin configurations
	Page 11	Changed t_{OE} value in AC Electrical Characteristics, please refer to Errata #SMEN-01-05
	Pages 1 & 22	Replaced TM logo with ® logo
	Page 10	Changed AC Test Conditions Input Rise/Fall Times
07/01/02:		Consolidated multiple devices into one datasheet
	Pages 1 & 5	Added DCD capability for Pipelined Outputs
	Page 7	Clarified T_{BIAS} and added T_{JN}
	Page 9	Changed DC Electrical Parameters
	Page 11	Removed Clock Rise & Fall Time from AC Electrical Characteristics Table
		Removed Preliminary status
05/19/03:	Page 11	Added Byte Enable SetupTime & Byte Enable Hold Time to AC Elecctrical Characteristics Table
	Page 22	Added IDT Clock Solution Table
01/10/06:	Page 1	Added green availability to features
	Page 5	Changed footnote 2 for Truth Table I from $\overline{\text{ADS}}$, $\overline{\text{CNTEN}}$, $\overline{\text{REPEAT}}$ = V_{IH} to $\overline{\text{ADS}}$, $\overline{\text{CNTEN}}$, $\overline{\text{REPEAT}}$ = X
	Page 22	Added green indicator to ordering information
07/25/08:	Page 9	Corrected a typo in the DC Chars table
01/19/09:	Page 22	Removed "IDT" from orderable part number
07/26/10:	Page 11	In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range values located in the table, the commercial TA header note has been removed
	Pages 13-16	In order to correct the footnotes of timing diagrams, $\overline{\text{CNTEN}}$ has been removed to reconcile the footnotes with the $\overline{\text{CNTEN}}$ logic definition found in Truth Table II - Address Counter Control
10/14/14:	Page 22	Added Tape & Reel to Ordering Information
06/21/18:		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
03/07/19:	Pages 1, 22	Added orderable part information table. Updated EOL note to obsolete status.

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