Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256SA70

FEATURES:

- 32K x 8 CMOS static RAM
- Equal access and cycle times
  -- Commercial: 70ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin 30 mil Plastic SOJ, 28-pin 300 mil Plastic Dip, 28-pin 300 mil TSOP Type I, and 28-pin 600 mil Plastic Dip.

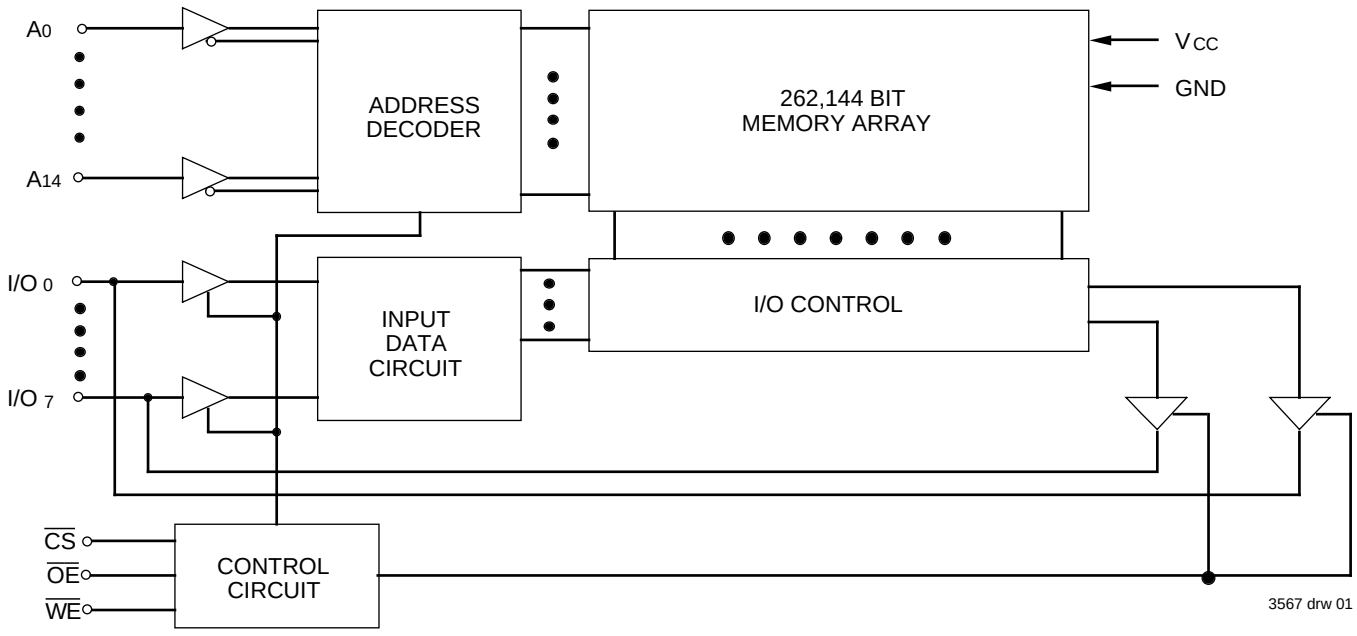
DESCRIPTION:

The IDT71256SA is a 262,144-bit medium-speed Static RAM organized as 32K x 8. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for your memory needs.

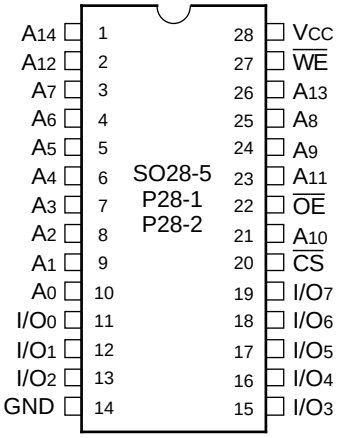
All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71256SA is packaged in a 28-pin 300 mil Plastic SOJ, 28-pin 300 mil Plastic Dip, 28-pin 300 mil TSOP Type I and 28-pin 600 mil Plastic Dip.

FUNCTIONAL BLOCK DIAGRAM

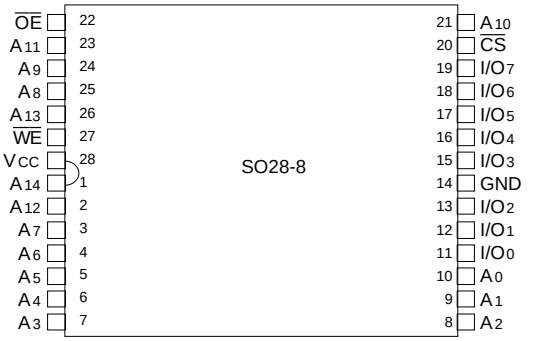


PIN CONFIGURATION



3567 drw 02

SOJ/DIP
TOP VIEW



3567 drw 03

TSOP
TOP VIEW

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3567 tbl 01
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3567 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	11	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	11	pF

NOTE: 3567 tbl 03
1. This parameter is guaranteed by device characterization, but not production tested.

TRUTH TABLE[1,2]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected — Standby (I_{SB})
V_{HC}[3]	X	X	High-Z	Deselected — Standby (I_{SB1})

NOTES: 3567 tbl 04
1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} –0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71256SA		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3567 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC}–0.2V)

Symbol	Parameter	71256SA70 Com'l.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	130	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	20	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{CC} = Max., f = 0(2) $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	15	mA

NOTES: 3567 tbl 06

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing .

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3567 tbl 07

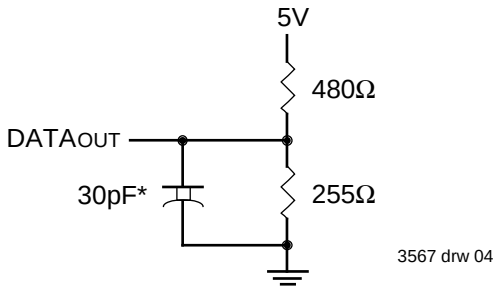


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Figure 1. AC Test Load

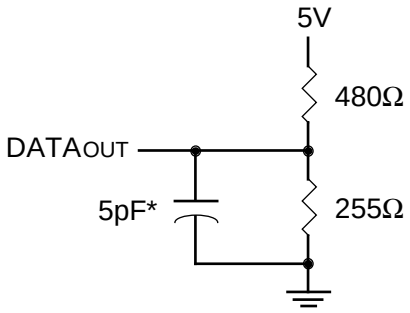

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Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Including jig and scope capacitance.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, CommercialTemperature Range Only)

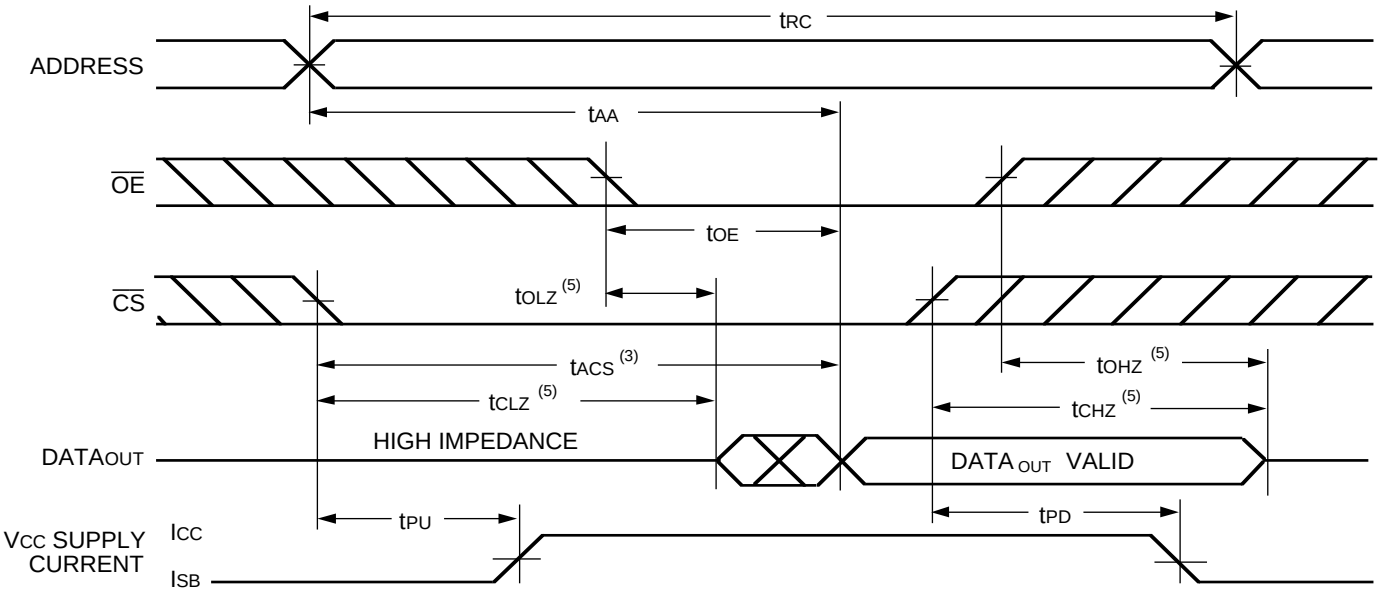
Symbol	Parameter	71256SA70 Min.	71256SA70 Max.	Unit
Read Cycle				
t_{RC}	Read Cycle Time	70	—	ns
t_{AA}	Address Access Time	—	70	ns
t_{ACS}	Chip Select Access Time	—	70	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	4	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High-Z	0	11	ns
t_{OE}	Output Enable to Output Valid	—	11	ns
t_{OLZ}(2)	Output Enable to Output in Low-Z	0	—	ns
t_{OHZ}(2)	Output Disable to Output in High-Z	0	10	ns
t_{OH}	Output Hold from Address Change	3	—	ns
t_{PU}(2)	Chip Select to Power Up Time	0	—	ns
t_{PD}(2)	Chip Deselect to Power Down Time	—	25	ns
Write Cycle				
t_{WC}	Write Cycle Time	70	—	ns
t_{AW}	Address Valid to End of Write	20	—	ns
t_{CW}	Chip Select to End of Write	20	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{WP}	Write Pulse Width	20	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{DW}	Data Valid to End of Write	13	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{OW}(2)	Output Active from End of Write	4	—	ns
t_{WHZ}(2)	Write Enable to Output in High-Z	0	11	ns

NOTES:

3567 tbl 08

1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



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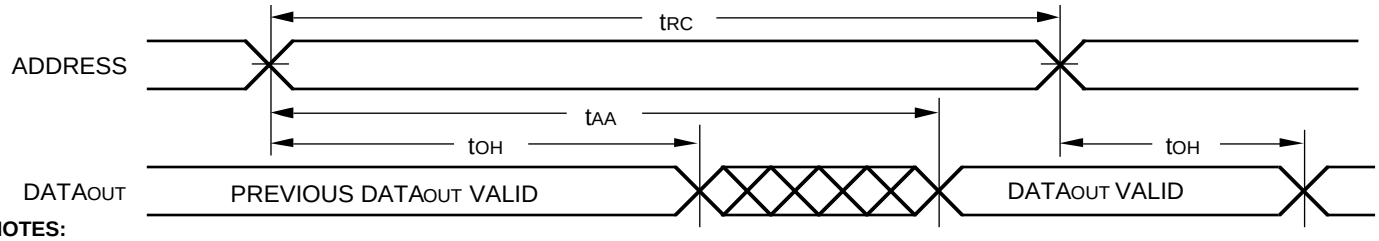
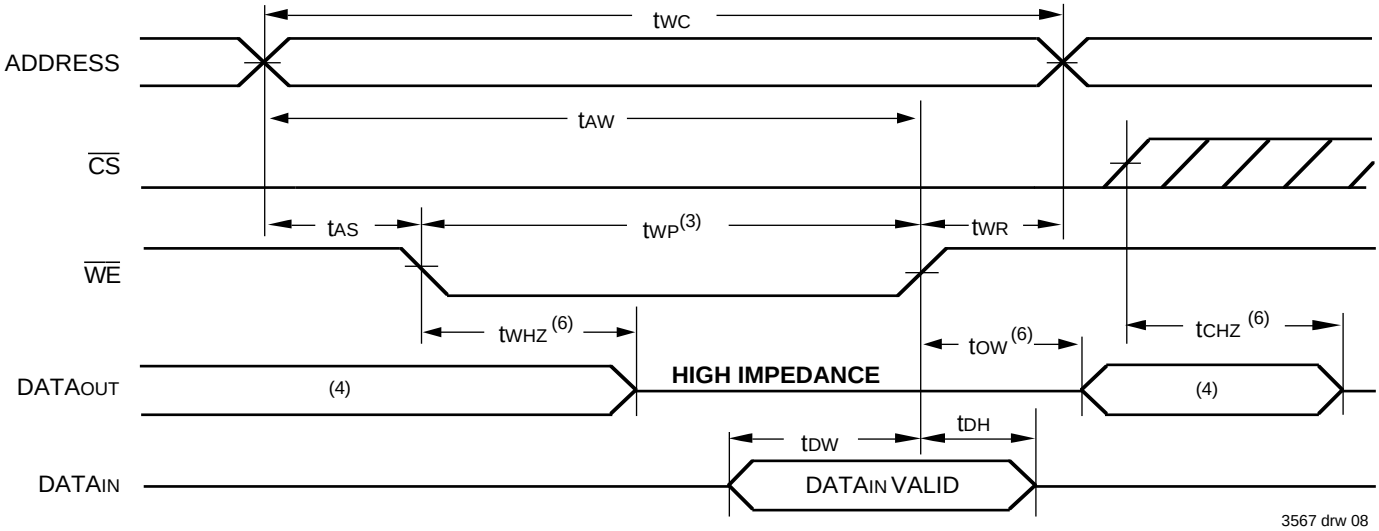
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



3567 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



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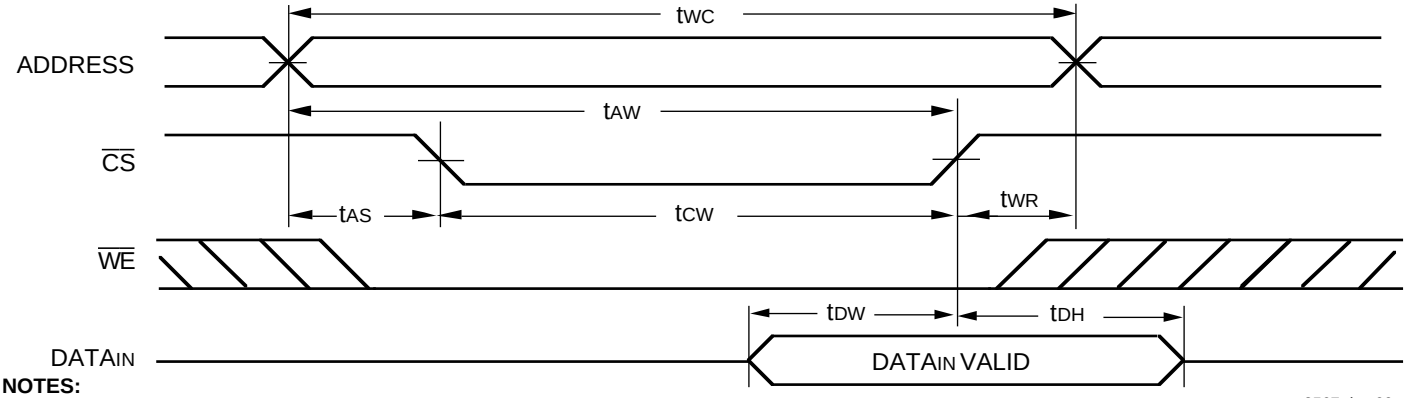
TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



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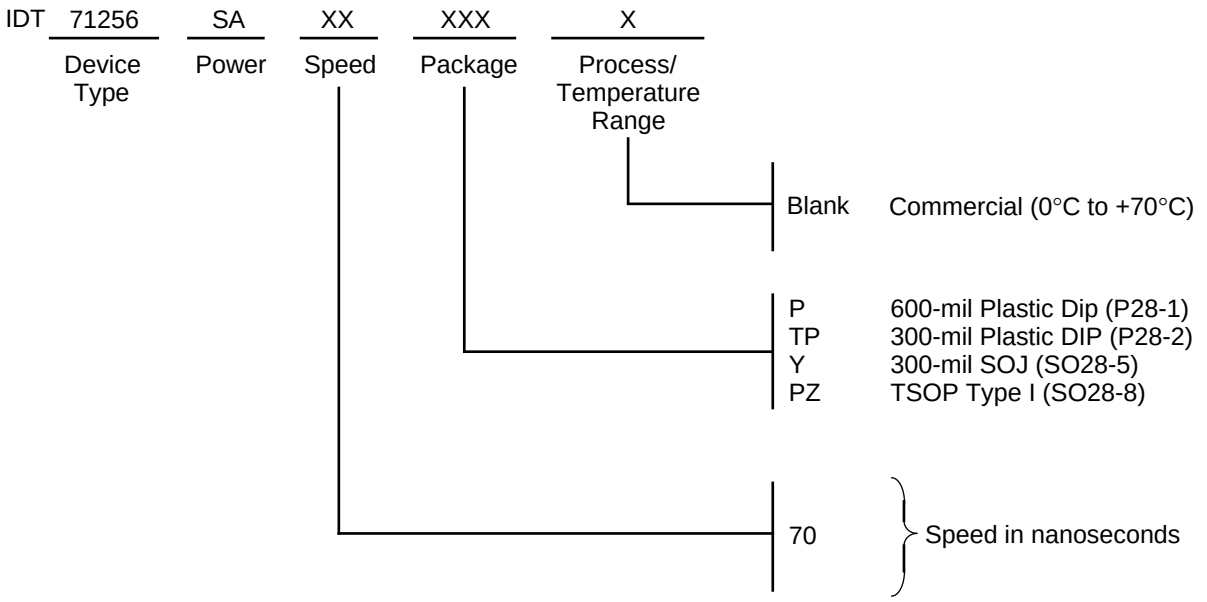
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



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