Integrated Device Technology, Inc.

CMOS STATIC RAMS 256K (256K x 1-BIT)

ADVANCE INFORMATION
IDT71257S
IDT71257L

FEATURES:

- High-speed (equal access and cycle times)
  - —Military — 45/55/70/85ns max.
  - —Commercial — 35/45/55/70ns max.
- Low-power operation
  - —IDT 71257S
    Active: 400mW (typ.)
    Standby: 400μW (typ.)
  - —IDT 71257L
    Active: 350mW (typ.)
    Standby: 100μW (typ.)
- Battery backup operation — 2V data retention (L version only)
- High-density industry standard 24-pin, 300 mil DIP
- Produced with advanced CEMOS™ technology
- Separate data input and output
- Single 5V (±10%) power supply
- Inputs/outputs TTL-compatible
- Three state outputs
- Static operation — no clocks or refresh required
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71257, a 262,144-bit high-speed static RAM organized as 256K x 1, is fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 45ns are available, with typical power consumption of only 400mW. The IDT71257 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 80μW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT71257 is packaged in a 24-pin, 300 mil DIP providing excellent board-level packing densities.

The IDT71257 military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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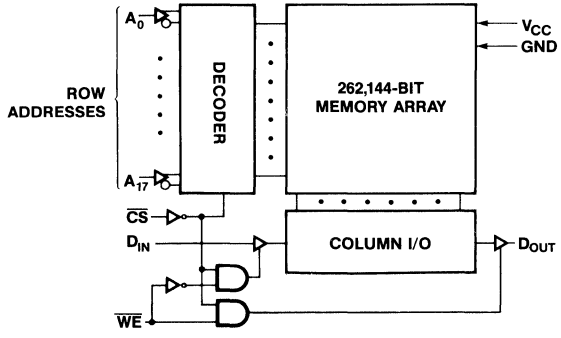
FUNCTIONAL BLOCK DIAGRAM



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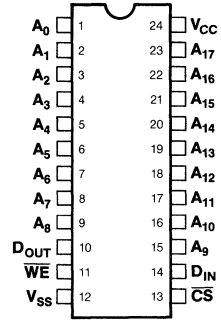
PIN CONFIGURATION



DIP
TOP VIEW

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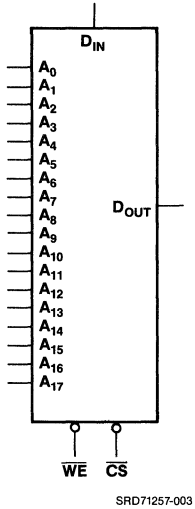
PIN NAMES

A_{0-17}	Address Inputs
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

LOGIC SYMBOL



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