Integrated Device Technology, Inc

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 512 x 9-BIT & 1024 x 9-BIT

IDT7201SA/LA
IDT7202SA/LA

FEATURES:

- First-In, First-Out dual port memory
- 512 x 9 organization (IDT7201A)
- 1024 x 9 organization (IDT7202A)
- Low power consumption
- Ultra high speed — 45ns cycle time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT7201A pin and functionally compatible with Mostek MK4501 but with half-full flag capability
- IDT7202A allows for deep word structure (1024) without expansion
- Half-full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance 1.2 micron CEMOS™ II technology
- Available in Plastic DIP, CERDIP and LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7201A/7202A is a dual port memory that utilizes a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 45ns (22MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also featues a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A half-full flag is available in the single device mode and width expansion modes.

The IDT7201A/7202A is fabricated using the high speed CEMOS II, 1.2 micron technology and is available in DIPs and LCCs screened to MIL-STD-883, Method 5004. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 1024 x 9 organization of the IDT7202A allows a 1024 deep word structure without the need for expansion.

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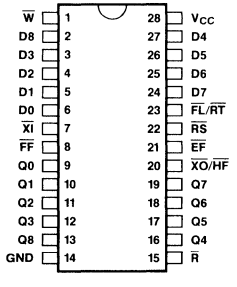
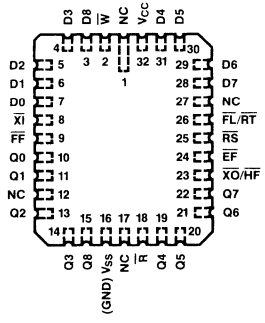
PIN CONFIGURATIONS

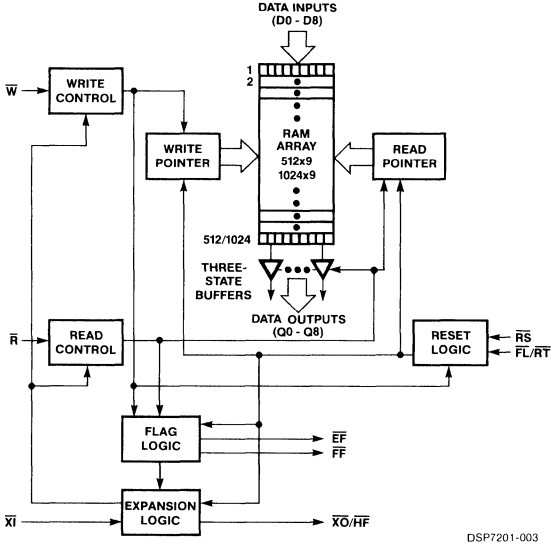


DIP
TOP VIEW



PLCC & LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V	—
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V	—
GND	Supply Voltage	0	0	0	V	—
V_{IH}	Input High Voltage Commercial	2.0	—	—	V	—
V_{IH}	Input High Voltage Military	2.2	—	—	V	—
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V	1

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7201SA/LA IDT7202SA/LA COMMERCIAL T_A = 35ns			IDT7201SA/LA IDT7202SA/LA MILITARY T_A = 40ns			IDT7201SA/LA IDT7202SA/LA COMMERCIAL T_A = 50, 65, 80, 120ns			IDT7201SA/LA IDT7202SA/LA MILITARY T_A = 50, 65, 80, 120ns			UNIT	NOTES
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{LI}	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	-1	—	1	-10	—	10	µA	1
I_{LO}	Output Leakage Current	-10	—	10	-10	—	10	-10	—	10	-10	—	10	µA	2
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	—	100	—	—	120	—	50	80	—	70	100	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	—	—	15	—	—	20	—	5	8	—	8	15	mA	3
$I_{CC3}(L)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	500	—	—	900	—	—	500	—	—	900	µA	3
$I_{CC3}(S)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	5	—	—	9	—	—	5	—	—	9	mA	3

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS

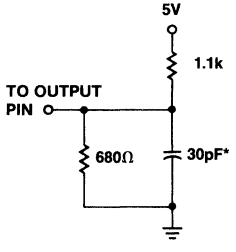
(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	COM'L		MILITARY		MILITARY AND COMMERCIAL								UNITS
		7201A/2A-35		7201A/2A-40		7201A/2A-50		7201A/2A-65		7201A/2A-80		7201A/2A-120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	35	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3, 4]	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	20	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Setup Time	18	—	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
$t_{HFH,FFH}$	Reset to Half & Full Flag High	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WEF}	Write High to Empty Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	45	—	50	—	65	—	80	—	100	—	140	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



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*Includes jig and scope capacitances.

Figure 1. Output Load.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

NOTE:

Generating $\overline{R}/\overline{W}$ Signals — When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important to not have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 5ns can affect the read or write pointer and cause it to increment.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0-D8)
Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2; i.e., t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change until t_{RSR} after the rising edge of $\overline{RS}$. HALF-FULL FLAG ($\overline{HF}$) will be reset to high after master RESET ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)
A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF-FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF-FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)
A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$, so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)
This is a dual purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded. (See Operating Modes.) In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the EXPANSION IN ($\overline{XI}$).

The IDT7201A/2A can be made to retransmit data when the RETRANSMIT ENABLE CONTROL ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 512/1024 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion Mode and will affect HALF-FULL FLAG ($\overline{HF}$) depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)
This input is a dual purpose pin. EXPANSION IN ($\overline{XI}$) is grounded to indicate an operation in the single device mode. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

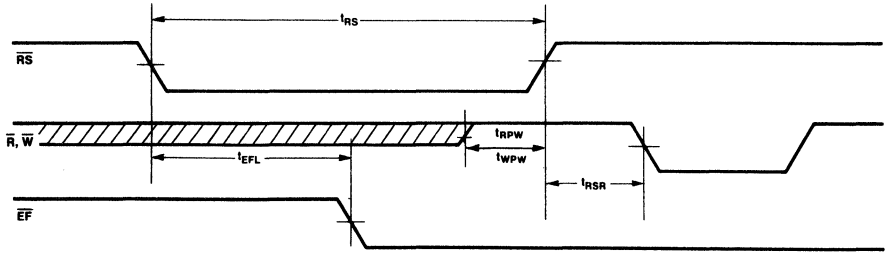
OUTPUTS:

FULL FLAG ($\overline{FF}$)
The FULL FLAT ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. if the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 512 writes for the IDT7201A and 1024 writes for the IDT7202A.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)
This is a dual purpose output. In the single device mode, when EXPANSION IN ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF-FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF-FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.



NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. W and R = V_{IH} around the rising edge of RS.

Figure 2. Reset

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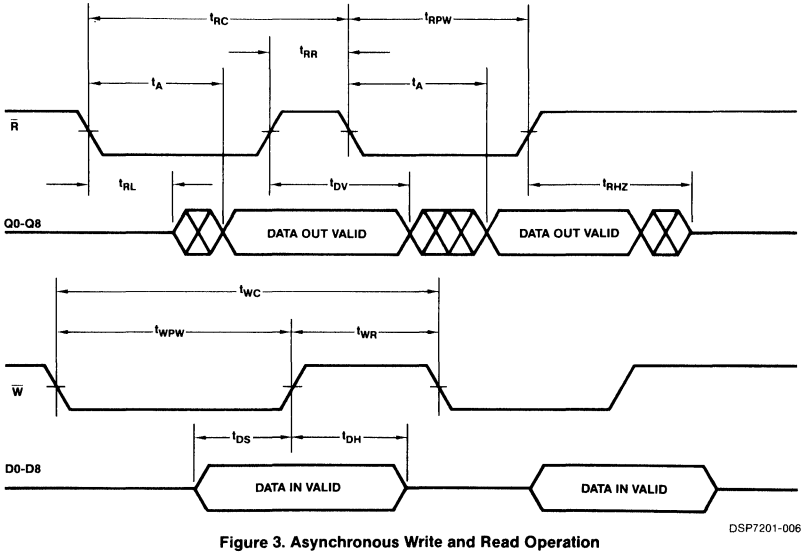


Figure 3. Asynchronous Write and Read Operation

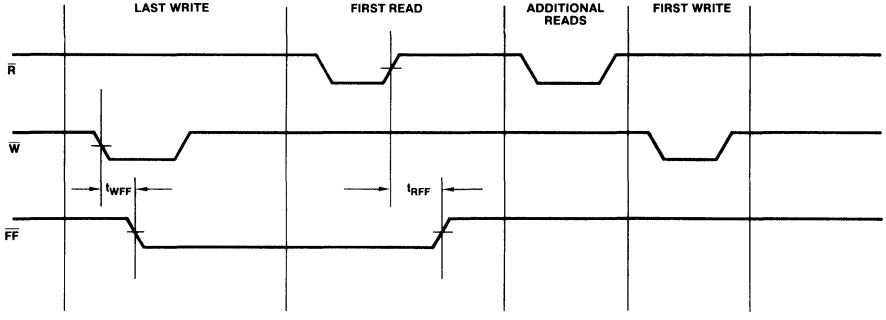


Figure 4. Full Flag From Last Write to First Read

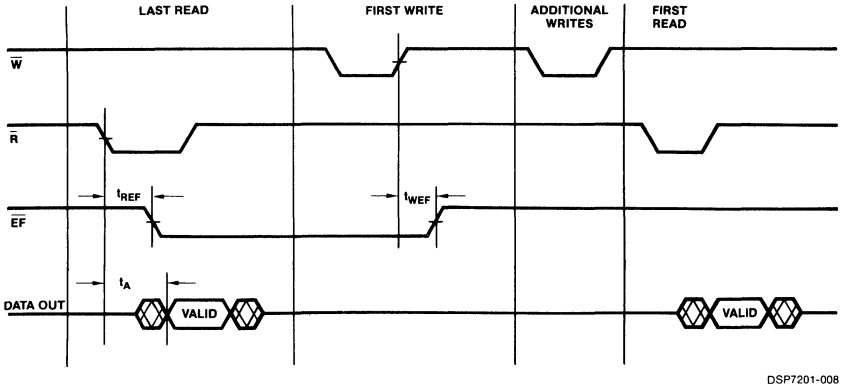
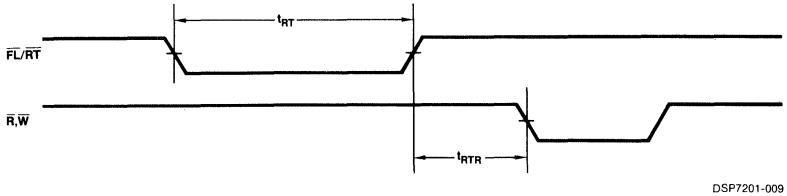


Figure 5. Empty Flag From Last Read to First Write

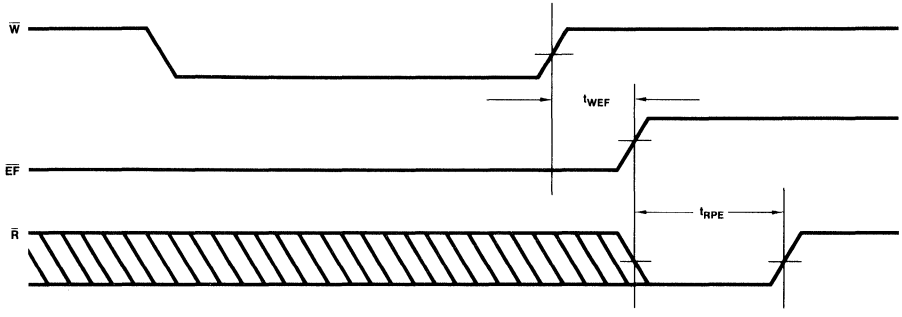


NOTES:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

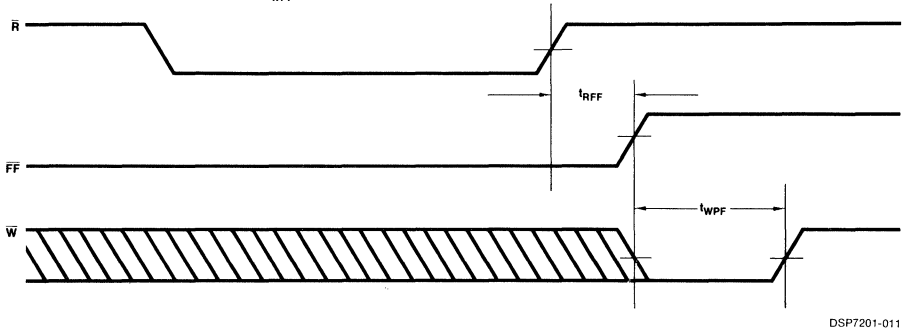


NOTE:

1. ($t_{RPE} = t_{RPW}$).

Figure 7. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:

1. ($t_{WPF} = t_{WPW}$).

Figure 8. Full Flag Timing

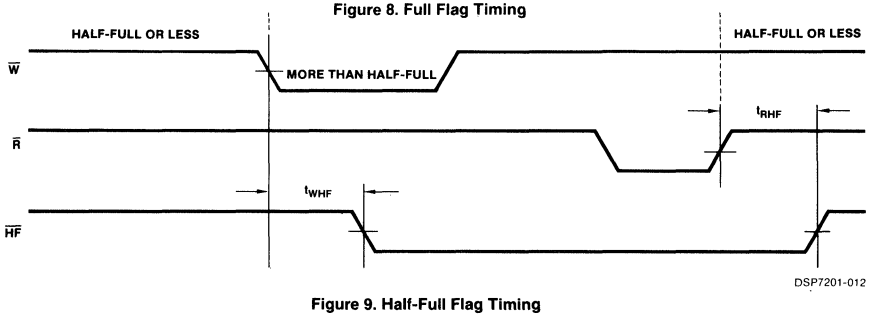


Figure 9. Half-Full Flag Timing

DATA OUTPUTS (Q0-Q8)
Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.

OPERATING MODES:

SINGLE DEVICE MODE
A single IDT7201A/2A may be used when the application requirements are for 512/1024 words or less. The IDT7201A/2A is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded. (See Figure 10.) In this mode the HALF-FULL FLAG ($\overline{HF}$), which is an active low output, is shared with EXPANSION OUT ($\overline{XO}$).

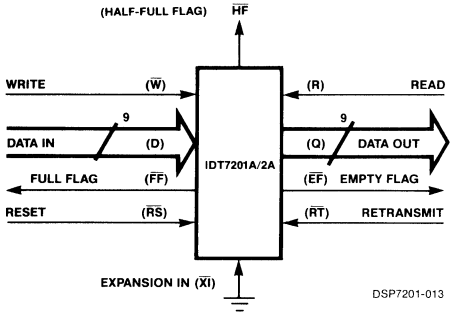
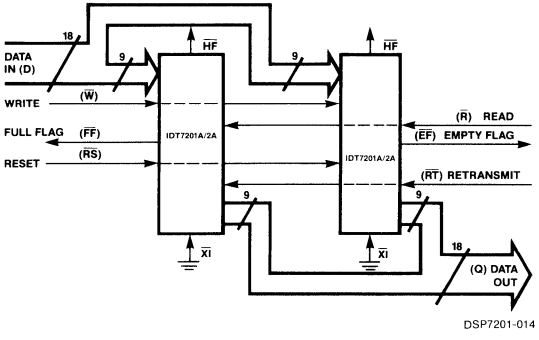


Figure 10. Block Diagram of Single 512x9/1024x9 FIFO



NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 11. Block Diagram of 512x18/1024x18 FIFO Memory Used in Width Expansion Mode

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 11 demonstrates an 18-bit word width by using two IDT7201A/2As. Any word width can be attained by adding additional IDT7201A/2As.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7201A/2A can easily be adapted to applications when the requirements are for greater than 512/1024 words. Figure 12 demonstrates Depth Expansion using three IDT7201A/2As. Any depth can be attained by adding additional IDT7201A/2As. The IDT7201A/2A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 12.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 12.
5. The RETRANSMIT ($\overline{RT}$) function and HALF-FULL FLAG ($\overline{HF}$) are not available in the Depth Expansion Mode.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 13.)

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7201A/2As as is shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 15), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ}ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would de-assert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 16), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

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TRUTH TABLES

TABLE I — RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output. $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

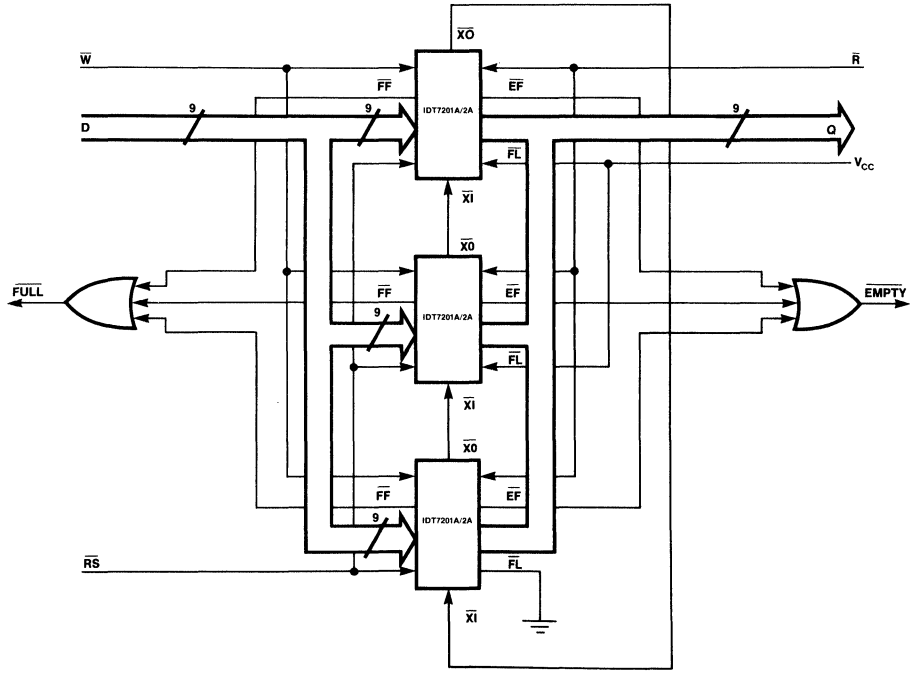

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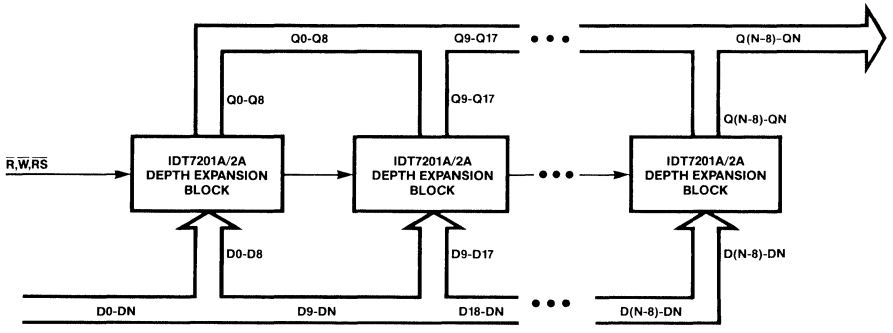
Figure 12. Block Diagram of 1536x9/3072x9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 12.
2. For Flag detection see WIDTH EXPANSION Section and Figure 11.

Figure 13. Compound FIFO Expansion

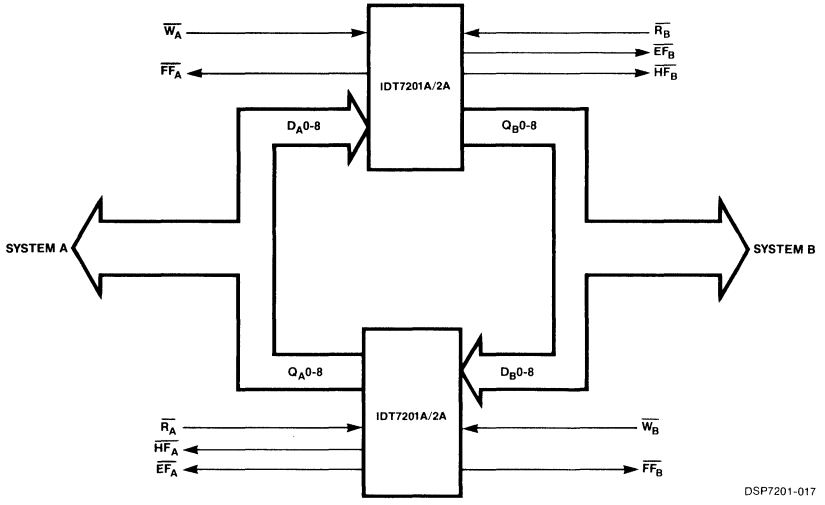


Figure 14. Bidirectional FIFO Mode

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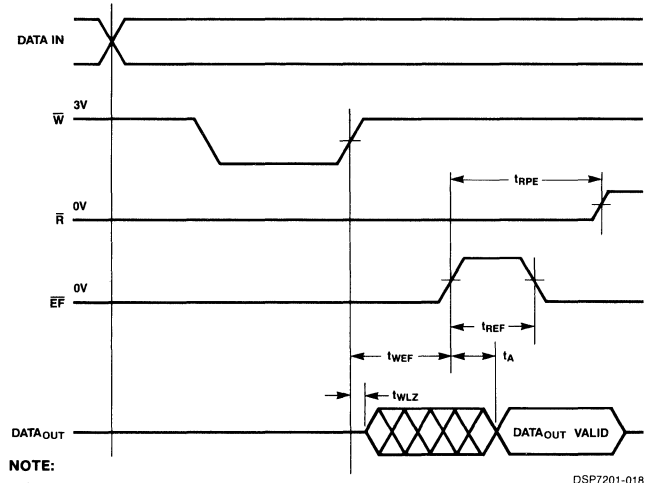
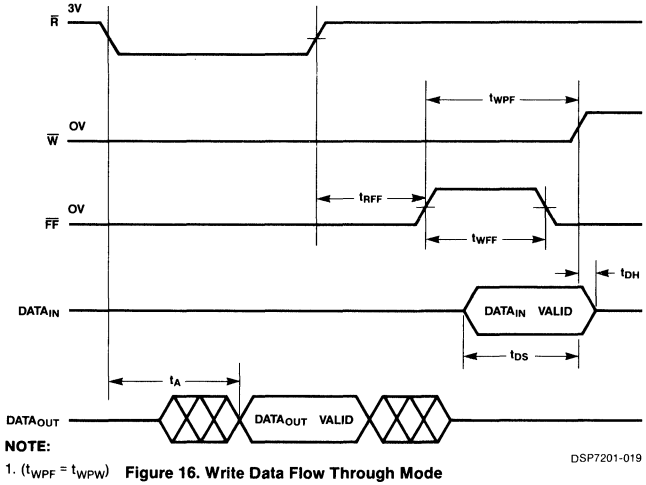


NOTE:
1. ($t_{RPE} = t_{RPW}$)

Figure 15. Read Data Flow Through Mode



NOTE:
1. ($t_{WPF} = t_{WPW}$)

Figure 16. Write Data Flow Through Mode