Integrated Device Technology, Inc.

64-BIT IEEE FLOATING POINT MULTIPLIER AND ALU

ADVANCE INFORMATION
IDT72064
IDT72065

FEATURES:

- Pin and functionally compatible with Weitek 1064/1065
- Low-power (750mW typical per device) operation
- Single 5 volt supply — no need for two supplies
- Advanced CEMOS™ II 1.5 micron technology
- Fully conforms to the requirements of IEEE Standard 754, version 10.0 for full 32-bit and 64-bit multiply and arithmetic operations.
- Very high-speed operation
  - —10 megaflops (100ns) pipelined ALU operation (add/subtract/convert/compare)
  - —5 megaflops (200ns) pipelined 32-bit (single precision) multiplications
  - —2.5 megaflops (400ns) pipelined 64-bit (double precision) multiplications
- Full floating point function arithmetic logic unit including:
  - —Add
  - —Subtract
  - —Absolute Value
  - —Compare
  - —Conversion to and from two's complement integer
- Flexible system design
  - —Three 32-bit ports allow two data inputs and one result output every 50ns
  - —One, two, or three port architectures supported
  - —Single phase, edge-triggered clock interface, with fully registered TTL or CMOS compatible inputs and outputs
- Standard 144-pin grid array package

DESCRIPTION:

The IDT72064 floating-point multiplier and the IDT72065 floating-point ALU provide high-speed 32-bit and 64-bit floating-point processing capability.

The IDT72064/065 are fabricated using IDT's advanced CEMOS II 1.5 micron technology and are capable of a total multiply latency (time required from the input of the operand until the result can be used by another device) of 500ns for single precision and 700ns for double precision multiplications. This ultra-high speed performance is achieved by combining both state-of-the-art CEMOS technology and advanced circuit design techniques.

For signal processing applications, where higher throughput speeds are required, operations including the function specification can be pipelined. For single precision multiplications, new operands can be loaded and a product unloaded every 200ns while double precision multiplies can be accomplished at a 400ns rate. The IDT72065 ALU executes all operations at a 100ns pipelined throughput. All operations including the function specification are pipelined so there is no penalty for interleaving various functions. The on-chip pipeline is automatically advanced using internal timers, so explicit pipeline flushing is not required.

This flexible two-chip set operates in full conformance with the requirements of IEEE standard 754 revision 10.0. It performs operations on single (32-bit) and double (64-bit) precision operands as well as conversion to 32-bit two's complement integers. The IDT72064/065 accommodates all rounding modes, infinity and reserved operand representations, and the treatment of exceptions, such as overflow, underflow, invalid and inexact operations. Exact conformance to the standards ensures complete software portability between prototype development and final application. A "FAST" mode eliminates the time penalty for denormalized numbers by substituting zero for a denormalized number.

The flexible input/output architecture of these devices allows them to be used in systems with one, two, or three 32-bit buses, or one 64-bit bus. Fully registered inputs and outputs, separately controlled, are loaded on each positive-going transition of the clock.

A 6-bit function control determines the arithmetic function to be performed while a 4-bit status output flags arithmetic exceptions and conditions. Both the function inputs and status outputs propagate along with the data to ease system design timing.

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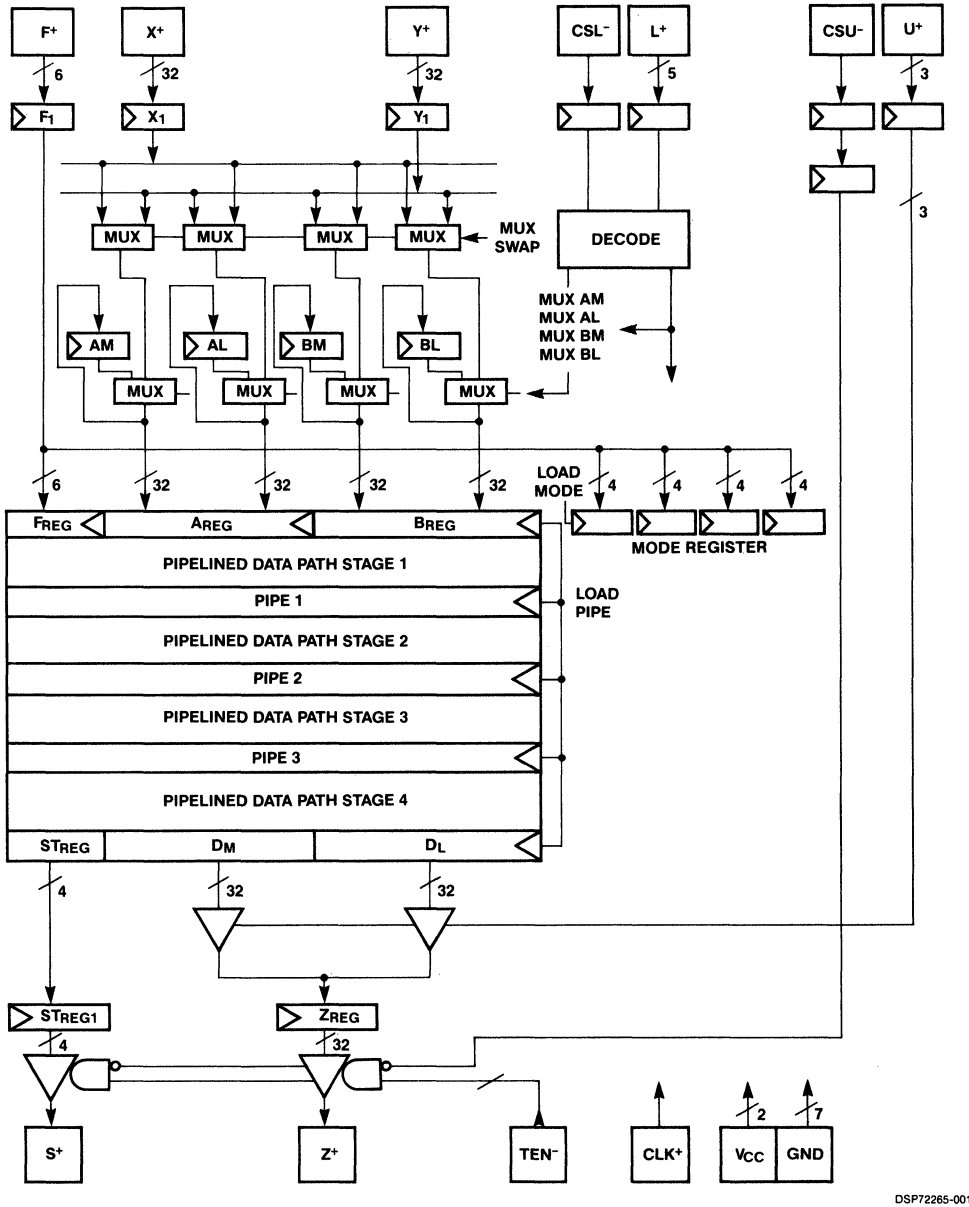
FUNCTIONAL BLOCK DIAGRAM
IDT72065 FLOATING POINT ALU



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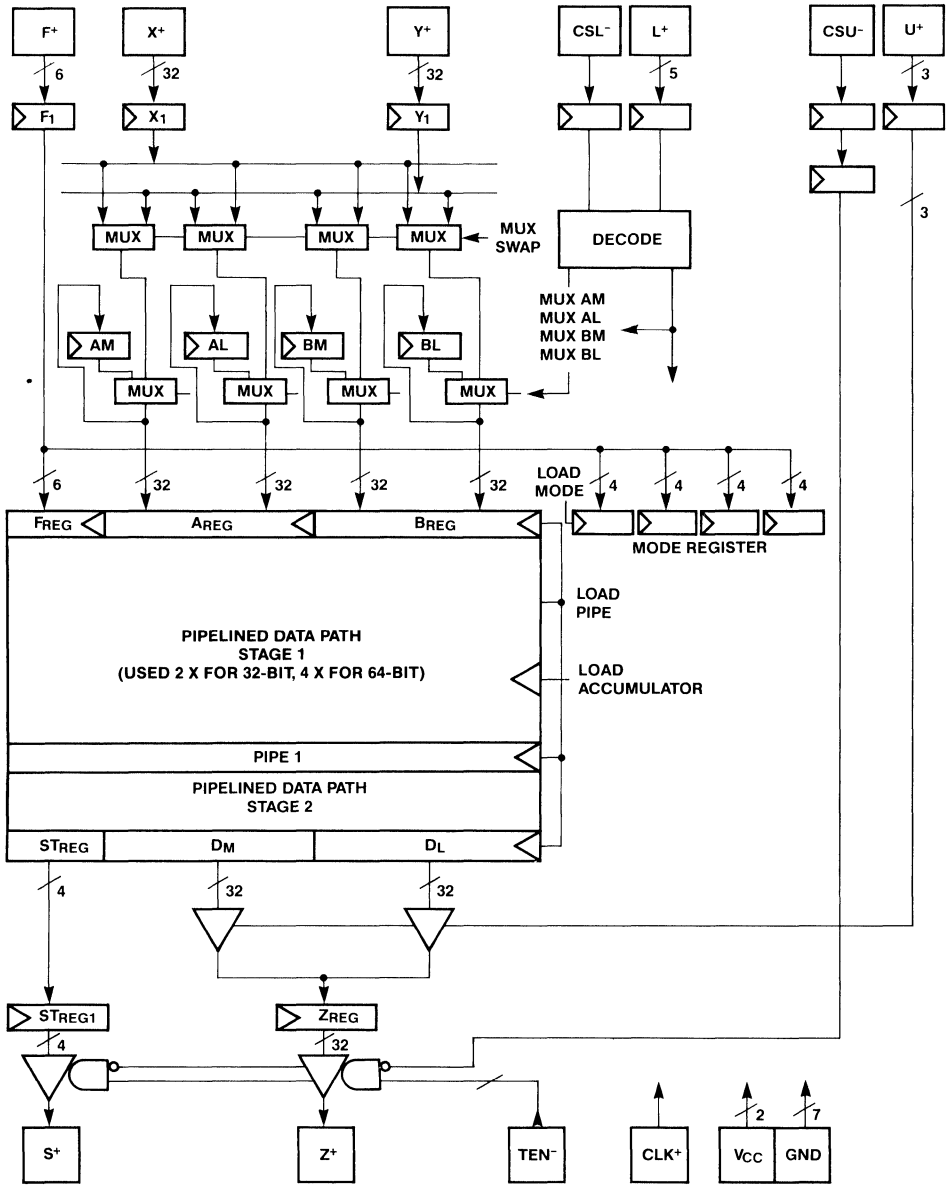
FUNCTIONAL BLOCK DIAGRAM
IDT72065 FLOATING POINT MULTIPLIER



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PIN CONFIGURATION

GND	Z_{31}	Z_{14}	Z_{13}	Z_{27}	Z_{10}	Z_{25}	Z_{24}	Z_7	Z_{22}	Z_{20}	Z_{19}	Z_3	Z_1	GND
S_3	NC	V_{CC}	Z_{15}	Z_{29}	Z_{12}	Z_{11}	Z_9	Z_6	Z_{21}	Z_4	Z_{18}	Z_{17}	V_{CC}	Y_0
GND	S_2	NC	NC	Z_{30}	Z_{28}	Z_{26}	Z_8	Z_{23}	Z_5	Z_2	Z_{16}	Z_0	GND	Y_{17}
TEN	S_0	NC										NC	Y_{16}	Y_{18}
U_2	CSU	S_1										Y_1	Y_2	Y_4
NC	U_0	U_1										Y_3	Y_{19}	Y_{21}
NC	CLK	NC										Y_5	Y_{20}	Y_6
F_5	F_4	V_{SS}										Y_{23}	Y_{22}	Y_7
F_3	F_0	F_1										Y_8	Y_{25}	Y_{24}
F_2	NC	L_4										Y_{26}	Y_{10}	Y_9
NC	L_2	L_0										Y_{29}	Y_{27}	Y_{11}
L_3	NC	NC										Y_{15}	Y_{13}	Y_{12}
L_1	GND	X_{31}	X_{15}	X_{29}	X_{26}	X_8	X_{23}	X_5	X_3	X_1	NC	Y_{31}	Y_{14}	Y_{28}
CSL	NC	X_{14}	X_{13}	X_{27}	X_{10}	X_{25}	X_{22}	X_{20}	X_{19}	X_2	X_{16}	NC	NC	Y_{30}
GND	X_{30}	X_{28}	X_{12}	X_{11}	X_9	X_{24}	X_7	X_6	X_{21}	X_4	X_{18}	X_{17}	X_0	V_{SS}

144-PIN PGA
(PIN GRID ARRAY)
TOP VIEW

DSP72265-003