Integrated Device Technology, Inc.

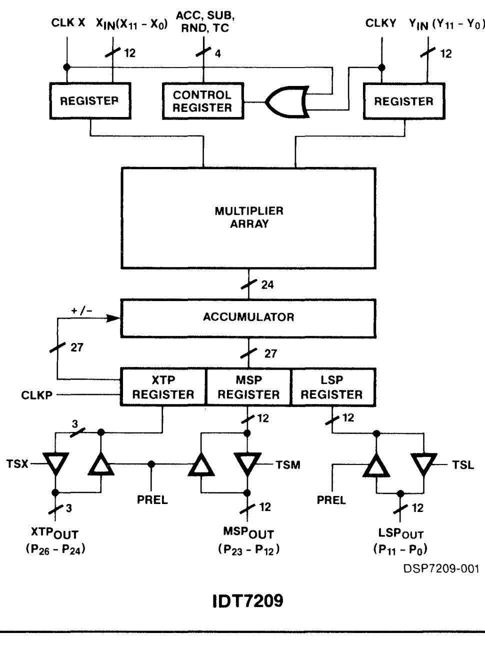
12 x 12 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7209L

FEATURES:

- 12 x 12 parallel multiplier/accumulator with selectable accumulation and subtraction
- High-speed — 30ns maximum multiply/accumulate time
- Selectable accumulation, subtraction, rounding and preloading with 27-bit result
- Pin and functionally compatible with the TRW TDC1009J
- Performs subtraction and double precision addition and multiplication
- Produced using advanced CEMOS™ high-performance technology
- Low-power consumption (less than 150mW typical) — less than 1/10 the power of compatible bipolar
- Inputs and outputs directly TTL-compatible
- Single 5V supply
- Available in DIP, SHRINK-DIP, plastic DIP or LCC
- Military product available 100% screened to MIL-STD-883, Class B

FUNCTIONAL BLOCK DIAGRAM



IDT7209

DESCRIPTION:

The IDT7209 is a high-speed, low-power 12 x 12 parallel multiplier/accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using IDT's CEMOS silicon gate technology, this device offers a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/10 the power dissipation and exceptional speed (30ns maximum) performance.

A pin and functional replacement for TRW's TDC1009J, the IDT7209 operates from a single 5 volt supply and is compatible with standard TTL logic levels. The architecture of the IDT7209 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flops, a preload capability which enables input data to be preloaded into the output registers, individual three-state output ports for the extended product (XTP) and most significant product (MSP), and a least significant product (LSP) output.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the two's complement input (TC) as either two's complement or an unsigned magnitude, yielding a full-precision 24-bit result that may be accumulated to a full 27-bit result. The three output registers—extended product (XTP), most significant product (MSP) and least significant product (LSP)—are controlled by the respective TSX, TSM and TSL input lines.

The accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from subsequent results. When the subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the extended product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The ROUND (RND) control rounds up the most significant product (MSP) and the 3-bit extended product (XTP) outputs. When preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see PRELOAD truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

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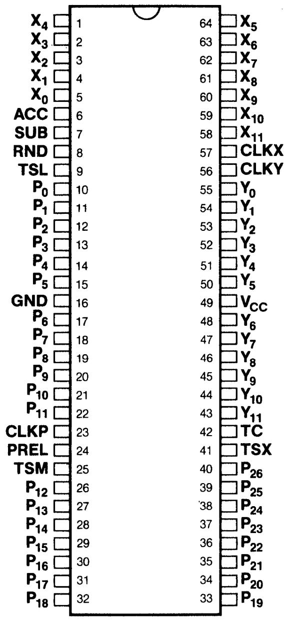
PIN CONFIGURATIONS



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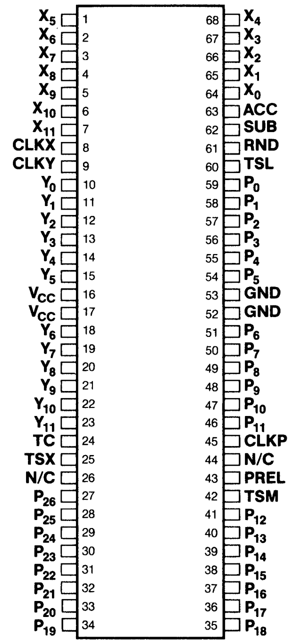
**DIP
TOP VIEW**



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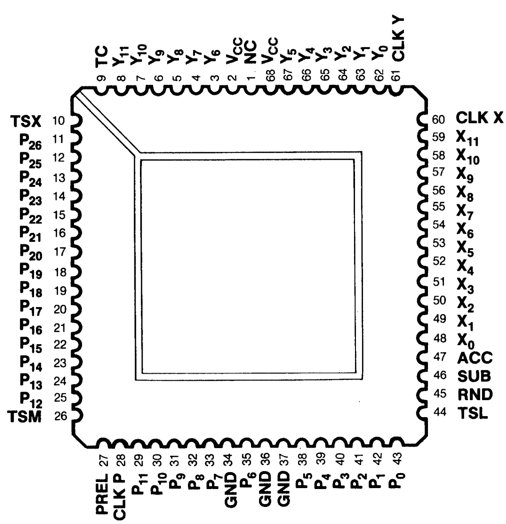
**SHRINK-DIP
TOP VIEW**



DSP7209-003

**LCC
TOP VIEW**

ABSOLUTE MAXIMUM RATING[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.6	1.6	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C) for Commercial clocked multiply times of 30,45,55,65ns or Military, 40,55,65,75ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	10	—	—	20	µA
I_{CC}[2]	Operating Power Supply Current	Outputs Open Measured at 10MHz[2]	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	—	4	20	—	4	25	mA
I_{CC}/f[2,3]	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	6	—	—	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80 + 6(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 100 + 8(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C) for Commercial clocked multiply times of 100,135ns or Military, 120,170ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}[2]	Operating Power Supply Current	Outputs Open Measured at 10MHz[2]	—	30	60	—	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	—	0.1	1.0	—	0.1	2.0	mA
I_{CC}/f[2,3]	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	5	—	—	7	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 60 + 5(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 80 + 7(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

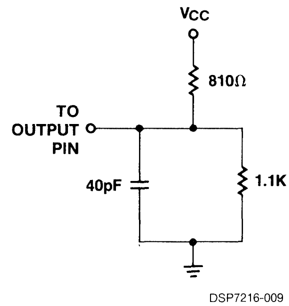


Figure 1. AC Output Test Load

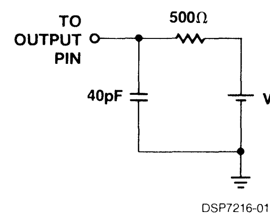


Figure 2. Output Three State Delay Load (V_X = 0V or 2.6V)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7209L-30 MIN.	IDT7209L-30 MAX.	IDT7209L-45 MIN.	IDT7209L-45 MAX.	IDT7209L-65 MIN.	IDT7209L-65 MAX.	IDT7209L-100 MIN.	IDT7209L-100 MAX.	IDT7209L-135 MIN.	IDT7209L-135 MAX.	UNITS	TEST LOAD FIG.
t_{MA}	Multiply-Accumulate Time	—	30	—	45	—	65	—	100	—	135	ns	1
t_D	Output Delay	—	25	—	25	—	35	—	35	—	40	ns	1
t_{ENA}	3-State Output Enable Delay(1)	—	25	—	25	—	30	—	35	—	40	ns	2
t_{DIS}	3-State Output Disable Delay(1)	—	25	—	25	—	30	—	35	—	40	ns	2
t_S	Input Register Setup Time	12	—	15	—	25	—	25	—	25	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	10	—	15	—	25	—	25	—	25	—	ns	—

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = 0°C to +125°C)

SYMBOL	PARAMETER	IDT7209L-40 MIN.	IDT7209L-40 MAX.	IDT7209L-55 MIN.	IDT7209L-55 MAX.	IDT7209L-75 MIN.	IDT7209L-75 MAX.	IDT7209L-120 MIN.	IDT7209L-120 MAX.	IDT7209L-170 MIN.	IDT7209L-170 MAX.	UNITS	TEST LOAD FIG.
t_{MA}	Multiply-Accumulate Time	—	40	—	55	—	75	—	120	—	170	ns	1
t_D	Output Delay	—	25	—	30	—	35	—	40	—	45	ns	1
t_{ENA}	3-State Output Enable Delay(1)	—	25	—	30	—	35	—	40	—	45	ns	2
t_{DIS}	3-State Output Disable Delay(1)	—	25	—	30	—	35	—	40	—	45	ns	2
t_S	Input Register Setup Time	15	—	20	—	25	—	30	—	30	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	15	—	20	—	30	—	30	—	30	—	ns	—

NOTE:
1. Transition is measured ±500mV from steady state with loading specified in Fig. 2.

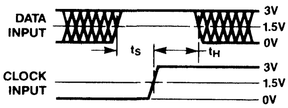


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Figure 3. Set Up and Hold Time

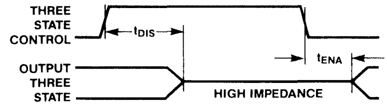

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Figure 4. Three State Control Timing Diagram

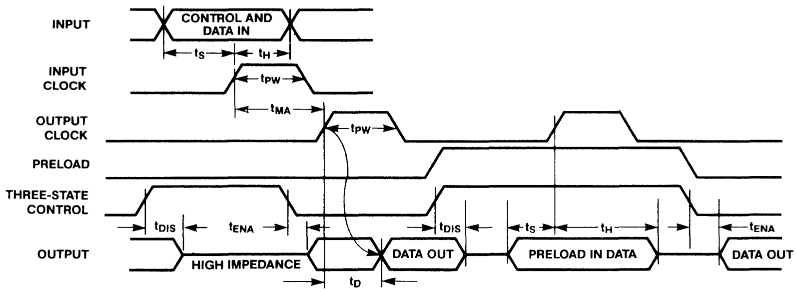

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Figure 5. Timing Diagram

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{11}-X_0)

Multiplicand Data Inputs

Y_{IN} (Y_{11}-Y_0)

Multiplier Data Inputs

INPUT CLOCKS:

CLKX, CLKY

Input data is loaded on the rising edge of these clocks.

CONTROLS:

ACC (Accumulate)

When ACC is high, the contents of the XTP, MSP and LSP registers are added to or subtracted from the multiplier output. When ACC is low, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)

When the ACC and SUB signals are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is high and SUB is low, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is low, SUB acts as a "don't care" input.

TC (Two's Complement)

When the TC Control is HIGH, it makes both the X and Y input, two's complement inputs. When the TC Control is LOW, it makes both inputs, X and Y, unsigned magnitude inputs.

RND (Round)

A high level at this input adds a "1" to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload)

When the PREL input is high, the output is driven to a high impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising of CLKP. The PREL, TSM TSL and TSX inputs must all be valid over the same period that the preload input is valid.

TSX, TSL, TSM (Three State Output Controls)

The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are high and are enabled when TSX, TSM and TSL are low.

OUTPUT CLOCK:

CLKP

Output data is loaded into the output register on the rising edge of this clock.

OUTPUTS:

XTP (P_{26}-P_{24})

Extended Product Output (3-bits)

MSP (P_{23}-P_{12})

Most Significant Product

LSP (P_{11}-P_{0})

Least Significant Product

NOTES ON TWO'S COMPLEMENT FORMATS:

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the 2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.

2. When in the non-accumulating mode, the first four bits (P_{26} through P_{23}) will all indicate the sign of the product. Additionally, the P_{22} term will also indicate the sign except for one exceptional case when multiplying -1×-1. With the additional bits that are available in this multiplier, the -1×-1 is valid operation that yields a +1 product.

3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 27-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES:
Hi Z = Output buffers at high impedance (output disabled).
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance, or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

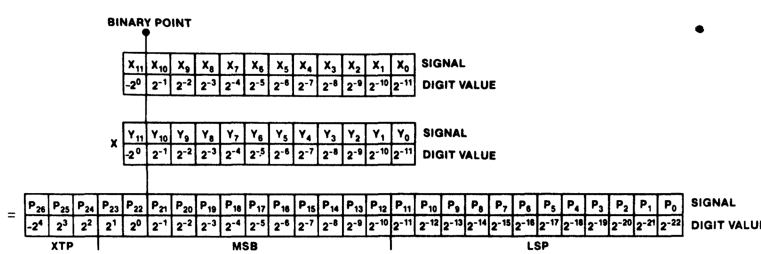

Figure 6. Fractional Two's Complement Notation

BINARY POINT

X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	DIGIT VALUE

x

Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	DIGIT VALUE

=

P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}
XTP			MSP												LSP											

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Figure 7. Fractional Unsigned Magnitude Notation

BINARY POINT

X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

x

Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

=

P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
-2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE
XTP			MSP												LSP												

DSP7209-011

Figure 8. Integer Two's Complement Notation

BINARY POINT

X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	SIGNAL
2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

x

Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	SIGNAL
2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE

=

P_{26}	P_{25}	P_{24}	P_{23}	P_{22}	P_{21}	P_{20}	P_{19}	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	P_{12}	P_{11}	P_{10}	P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	SIGNAL
2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DIGIT VALUE
XTP			MSP												LSP												

DSP7209-012

Figure 9. Integer Unsigned Magnitude Notation

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