Integrated Device Technology, Inc.

12 x 12 BIT PARALLEL CMOS MULTIPLIER

IDT7212L
IDT7213L

FEATURES:

- 12 x 12 parallel multiplier with double precision product
- High-speed — 30ns maximum clock to multiply time
- Low-power consumption — 150mW typical, less than 1/10th the power of compatible bipolar parts
- Produced with advanced CEMOS™ high-performance technology
- IDT7212L is pin and functionally compatible with TRW MPY012H
- IDT7213L requires only a single clock with register enables
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL-compatible
- Three-state output
- Available in DIP, SHRINK-DIP, plastic DIP, LCC or Flatpack
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7212/IDT7213 are high-speed, low power 12 x 12 multipliers ideal for fast, real-time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, high-reliability technology, CEMOS, has achieved speeds (30ns max.) exceeding bipolar at 1/10th the power consumption.

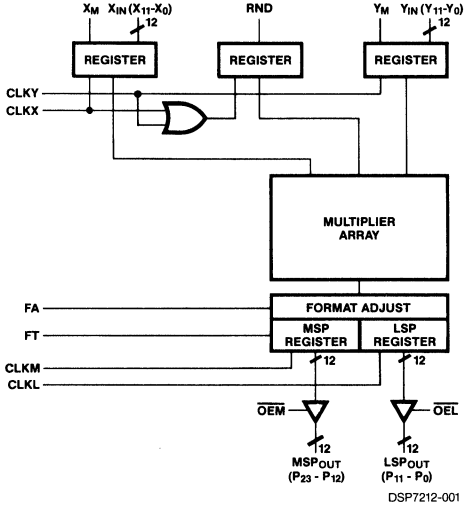
The IDT7212/IDT7213 are ideal for applications requiring high-speed multiplications such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition, and in any system requirement where multiplication speeds of a mini/micro computer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge triggered D-type flip-flop. With the IDT7212, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7213 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

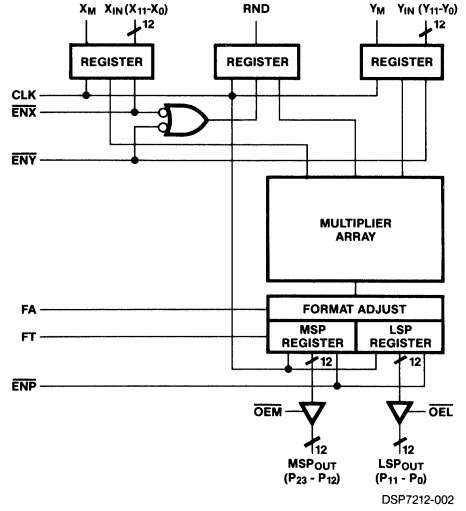
The IDT7212/IDT7213 offer additional flexibility with the FA control. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP.

The IDT7212/IDT7213 Multipliers are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAMS



IDT7212



IDT7213

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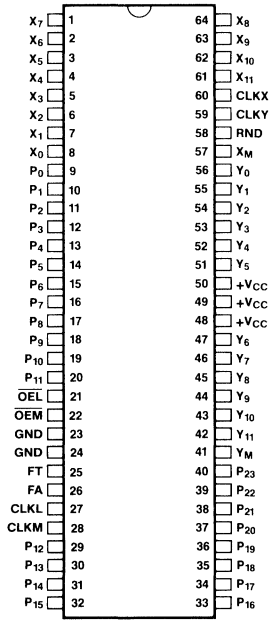
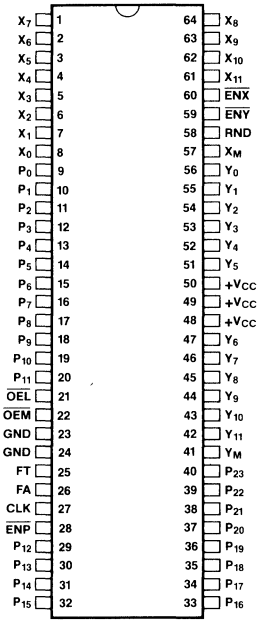
PIN CONFIGURATIONS

IDT7212
64-PIN DIP



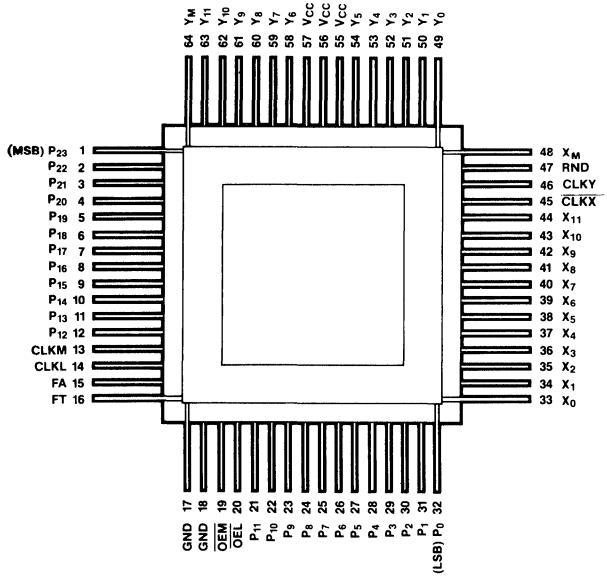
TOP VIEW DSP7212-003

IDT7213
64-PIN DIP



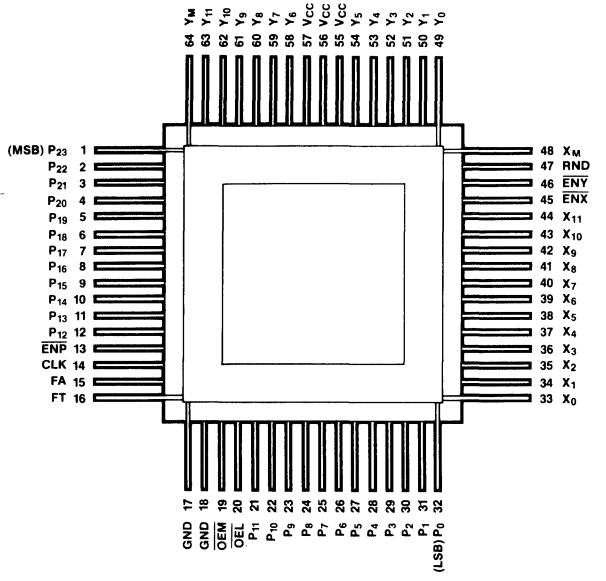
TOP VIEW DSP7212-004

IDT7212
64-LEAD FLATPACK



TOP VIEW DSP7212-005

IDT7213
64-LEAD FLATPACK



TOP VIEW DSP7212-007

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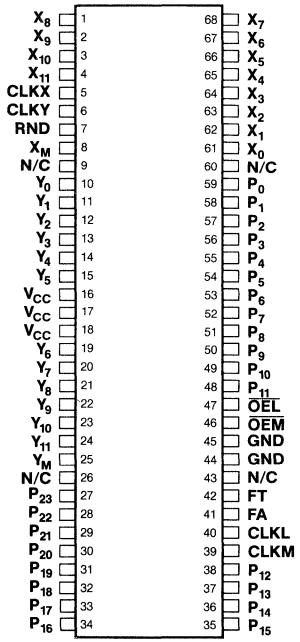
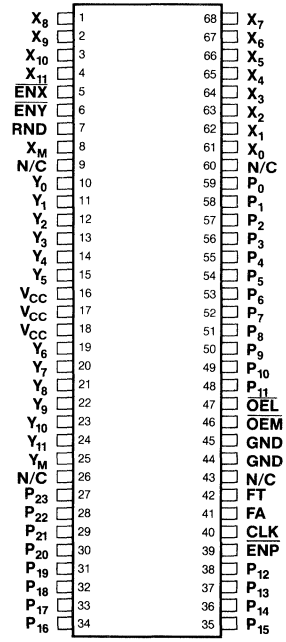
IDT7212
68-PIN SHRINK-DIP



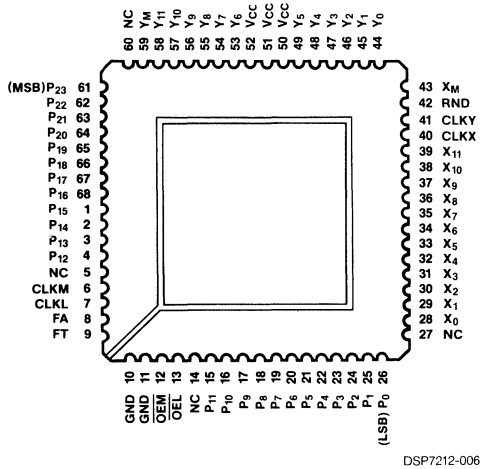
TOP VIEW

IDT7213
68-PIN SHRINK-DIP



TOP VIEW

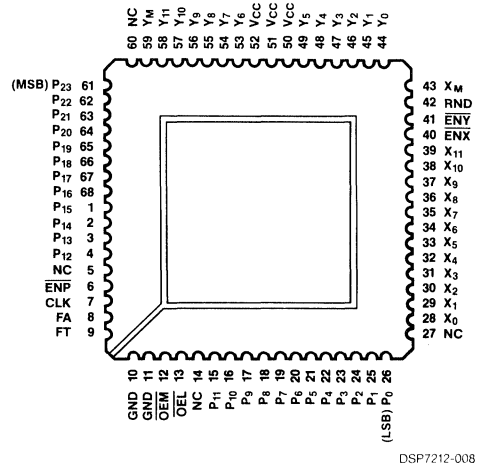
IDT7212
68-PIN LCC



DSP7212-006

TOP VIEW

IDT7213
68-PIN LCC



DSP7212-008

TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.4	1.4	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C , Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)
for Commercial clocked multiply times of 30,45,70ns or Military, 40,55,90ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	10	—	—	20	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	30	65	—	30	85	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	—	4	20	—	4	25	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	6	—	—	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 65 + 6(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 85 + 8(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C , Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)
for Commercial clocked multiply times of 115ns or Military, 140ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	25	55	—	25	75	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	—	0.1	1.0	—	0.1	2.0	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	5	—	—	7	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 55 + 5(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 75 + 7(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7212L30 IDT7213L30 MIN.	MAX.	IDT7212L45 IDT7213L45 MIN.	MAX.	IDT7212L70 IDT7213L70 MIN.	MAX.	IDT7212L115 IDT7213L115 MIN.	MAX.	UNITS	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	50	—	65	—	105	—	155	ns	1
t_{MC}	Clocked Multiply Time	—	30	—	45	—	70	—	115	ns	1
t_S	X, Y, RND Set-Up Time	15	—	20	—	20	—	25	—	ns	1
t_H	X, Y, RND Hold Time	3	—	3	—	2	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	15	—	20	—	20	—	25	—	ns	1
t_{PWL}	Clock Pulse Width Low	15	—	20	—	20	—	25	—	ns	1
t_{PDP}	Output Clock to P	—	25	—	25	—	30	—	40	ns	1
t_{ENA}	3 State Enable Time(2)	—	25	—	30	—	35	—	40	ns	2
t_{DIS}	3 State Disable Time(2)	—	25	—	25	—	30	—	35	ns	2
t_S	Clock Enable Setput Time (IDT7213 only)	15	—	20	—	25	—	25	—	ns	1
t_H	Clock Enable Hold Time (IDT7213 only)	3	—	3	—	3	—	0	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML(1) (IDT7212 only)	0	—	0	—	0	—	0	—	ns	1

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7212L40 IDT7213L40 MIN.	MAX.	IDT7212L55 IDT7213L55 MIN.	MAX.	IDT7212L90 IDT7213L90 MIN.	MAX.	IDT7212L140 IDT7213L140 MIN.	MAX.	UNITS	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	60	—	75	—	130	—	185	ns	1
t_{MC}	Clocked Multiply Time	—	40	—	55	—	90	—	140	ns	1
t_S	X, Y, RND Set-Up Time	20	—	20	—	25	—	30	—	ns	1
t_H	X, Y, RND Hold Time	3	—	3	—	2	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	20	—	25	—	30	—	30	—	ns	1
t_{PWL}	Clock Pulse Width Low	20	—	25	—	30	—	30	—	ns	1
t_{PDP}	Output Clock to P	—	25	—	30	—	35	—	45	ns	1
t_{ENA}	3 State Enable Time(2)	—	25	—	30	—	40	—	45	ns	2
t_{DIS}	3 State Disable Time(2)	—	25	—	25	—	40	—	45	ns	2
t_S	Clock Enable Setput Time (IDT7213 only)	20	—	25	—	30	—	30	—	ns	1
t_H	Clock Enable Hold Time (IDT7213 only)	3	—	3	—	2	—	0	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML(1) (IDT7212 only)	0	—	0	—	0	—	0	—	ns	1

NOTES:

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage with loading specified in Fig. 2.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is sampled and not 100% tested.

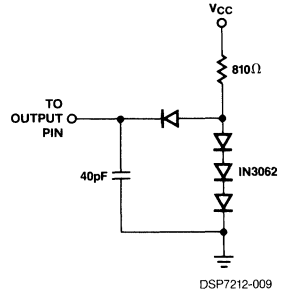


Figure 1. AC Output Test Load

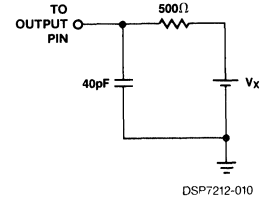
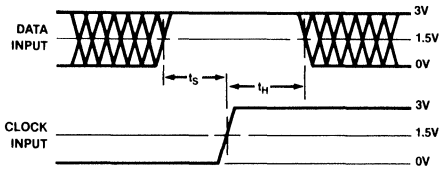


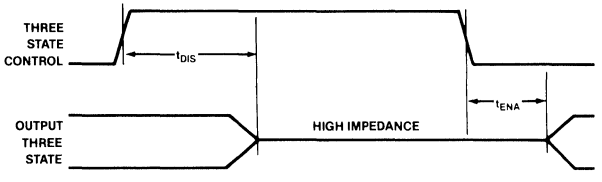
Figure 2. Output Three State Delay Load (V_X = 0V or 2.6V)



NOTE:
Diagram shown for HIGH data only. Output transition may be opposite sense.

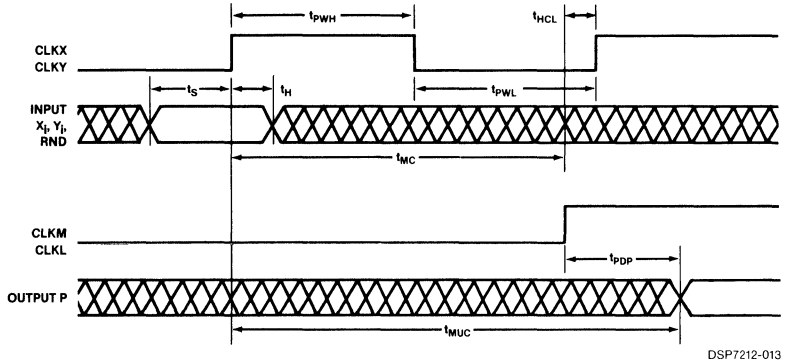
DSP7212-011

Figure 3. Set-Up And Hold Time



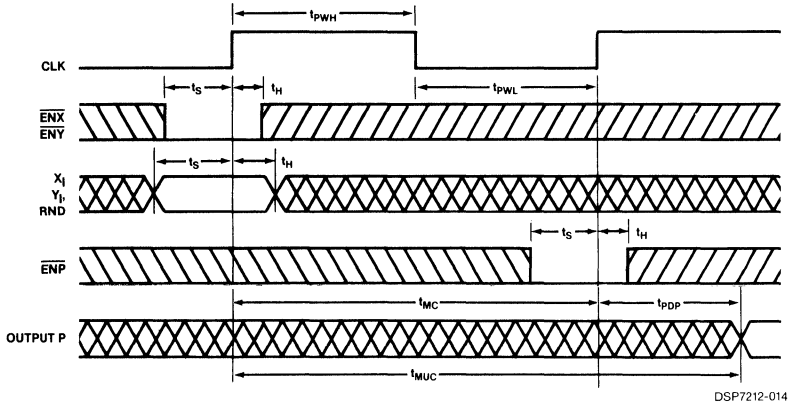
DSP7212-012

Figure 4. Three-State Control Timing Diagram



DSP7212-013

Figure 5. IDT7212 Timing Diagram



DSP7212-014

Figure 6. IDT7213 Timing Diagram

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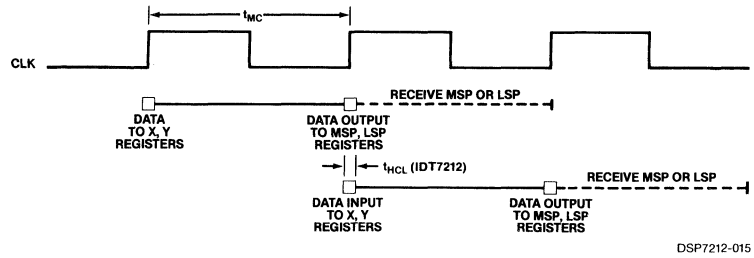


Figure 7. Simplified Timing Diagram-Typical Application

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{11} through X_0)
Twelve Multiplicand Data Inputs

Y_{IN} (Y_{11} through Y_0)
Twelve Multiplier Data Inputs

INPUT CLOCKS (IDT7212 ONLY):

CLKX
The rising edge of this clock loads the X_{11} - X_0 data input register along with the two's complement and round registers.

CLKY
The rising edge of this clock loads the Y_{11} - Y_0 data input register along with the two's complement and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7213 ONLY):

CLK
The rising edge of this clock loads all registers.

$\overline{ENX}$
Register enable for the X_{11} - X_0 data input register along with the two's complement and round registers.

$\overline{ENY}$
Register enable for the Y_{11} - Y_0 data input register along with the two's complement and round registers.

$\overline{ENP}$
Register enable for the Most Significant Product (MSP) and Least Significant Product (LSP).

CONTROLS:

X_M, Y_M (TCX, TCY)[1]
Mode control inputs for each data word. A low input designates unsigned data input with a high input used for two's complement.

NOTE:
1. TRW MPY012H/K pin designation

FA (RS)[1]
When the format adjust control is HIGH, a full 24-bit product is selected. When this control is LOW, a left-shifted 23-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications. (See Multiplier Input/Output Formats.)

FT
When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are bypassed.

$\overline{OEL}$
Three-state enable for LSP output.

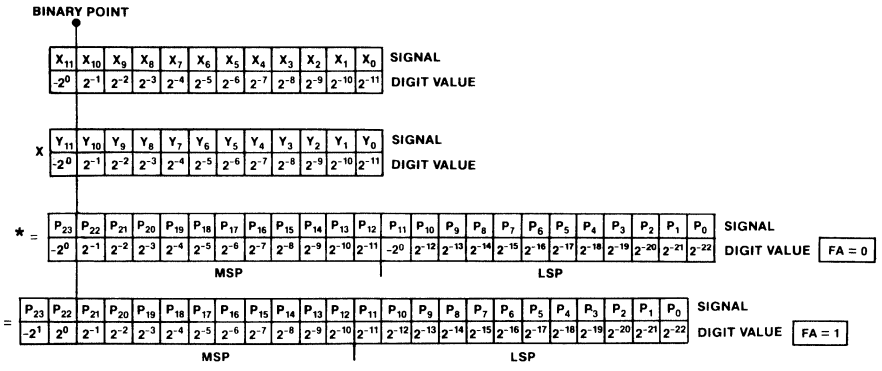
$\overline{OEP}$
Three-state enable for MSP output.

RND
Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the Format Adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the P_{10}. If FA is HIGH when RND is HIGH, a one will be added to the P_{11}. In either case, the LSP output will reflect this addition when RND is HIGH. Note also the rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

OUTPUTS:

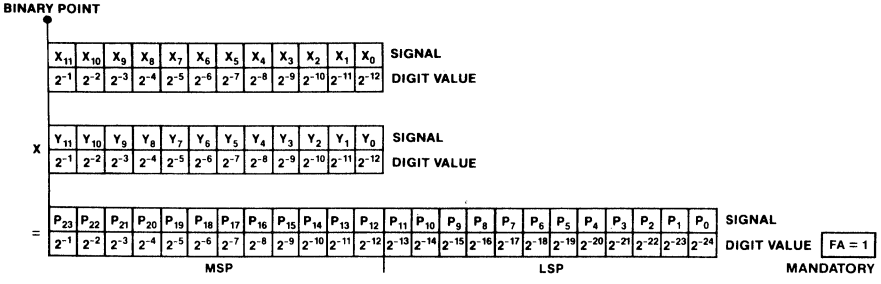
MSP (P_{23} through P_{12})
Most Significant Product Output

LSP (P_{11} through P_0)
Least Significant Product Output



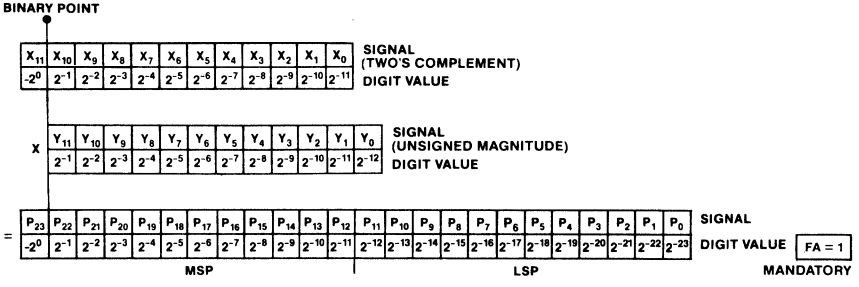
DSP7212-016

Figure 8. Fractional Two's Complement Notation



DSP7212-017

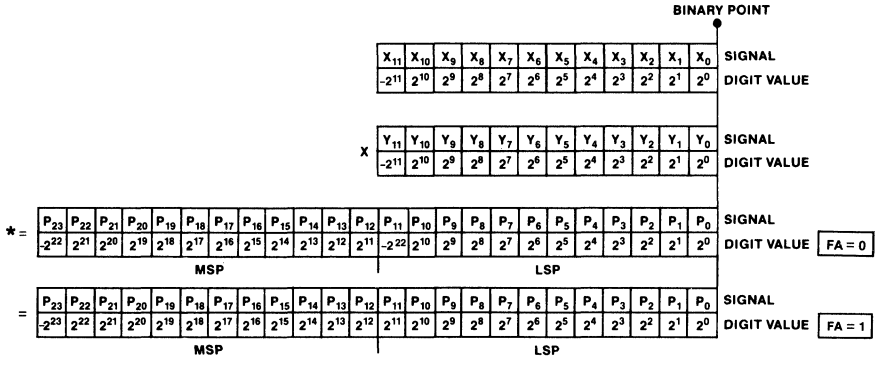
Figure 9. Fractional Unsigned Magnitude Notation



DSP7212-018

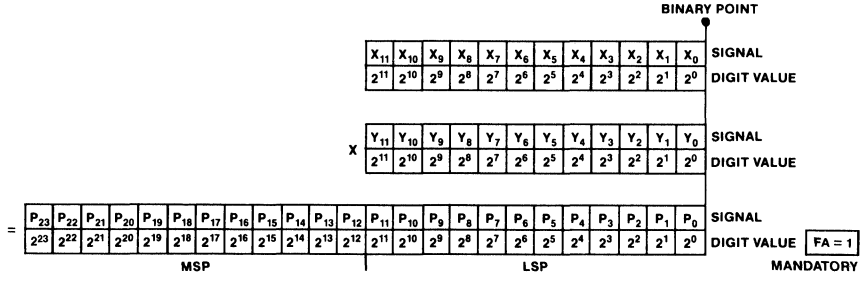
Figure 10. Fractional Mixed Mode Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 10000 . . . 0 with 1000 . . . 00 yielding an erroneous product of -1 in the fraction case and -2^{22} in the integer case.



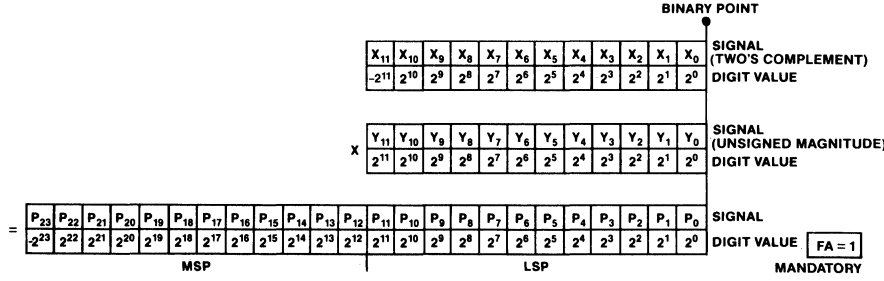
DSP7212-019

Figure 11. Integer Two's Complement Notation



DSP7212-020

Figure 12. Integer Unsigned Magnitude Notation



DSP7212-021

Figure 13. Integer Mixed Mode Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 10000 . . . 0 with 1000 . . . 00 yielding an erroneous product of -1 in the fraction case and -2^{22} in the integer case.